

## Parallel Optical Link Transmitter:

**PAROLI® 2 Tx AC, 1.25 Gbit/s**

**V23832-T2531-M101**

## Parallel Optical Link Receiver:

**PAROLI® 2 Rx AC, 1.25 Gbit/s**

**V23832-R511-M101**

### Design Benefits

- Relieve system bandwidth bottle necks
- Simplifies system design
- Enables system upgrades in field
- Low power consumption at increased board density
- Flat package for height critical application

### Features

- Infineon's highly reliable 850 nm VCSEL technology
- Power supply 3.3 V
- Transmitter with multistandard electrical interface
- Receiver with Infineon's adjustable CML output
- 12 electrical data channels
- Asynchronous, AC-coupled optical link
- 12 optical data channels
- Internal power monitoring for constant power budget
- Transmission data rate of up to 1250 Mbit/s per channel, total link data rate up to 15 Gbit/s
- PIN diode array technology
- Optimized for 62.5 µm multimode graded index fiber
- MT based optical port (MPO connector)
- Plug-in module with ultra low profile
- IEC Class 1M laser eye safety compliant
- OIF<sup>1)</sup> compliant
- GBE mask compliant modules available
- EMI-shielding for front panel access
- Standard link length compliant
- Unused transmitter channels can be switched off
- DC or AC coupling of input data
- Telcordia compliant



<sup>1)</sup> OIF-VSR4-01.0 Implementation Agreement (VSR OC-192/STM-64).

### Optical Port

- Designed for the industry standard 12 fiber MT Connector (MPO)
- Alignment pins fixed in module port
- Integrated mechanical keying
- Module is provided with a dust cover

### Features of MT Connector (MPO)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule
- MT compatible fiber spacing (250  $\mu\text{m}$ ) and alignment pin spacing (4600  $\mu\text{m}$ )
- Push-pull mechanism
- Ferrule bearing spring loaded

### Features of the PAROLI 2 Electrical Connector

- Pluggable version using BGA socket
- 100 pin positions (10x10)
- 4 mm stack height in mated conditions
- Plug and receptacle are provided with protective cap
- Standard BGA process for socket assembly
- Contact area plating made out of gold over nickel
- Module side: FCI-MEG-Array<sup>®</sup> -Plug (part no. 84512-202)
- PCB side: FCI-MEG-Array<sup>®</sup> -Receptacle (part no. 84513-201)

### Applications

- Switches, routers, transport equipment
- Mass storage devices
- Access network
- Rack-to-rack/board-to-board interconnect
- Optical backplane interconnect

Pin Configuration

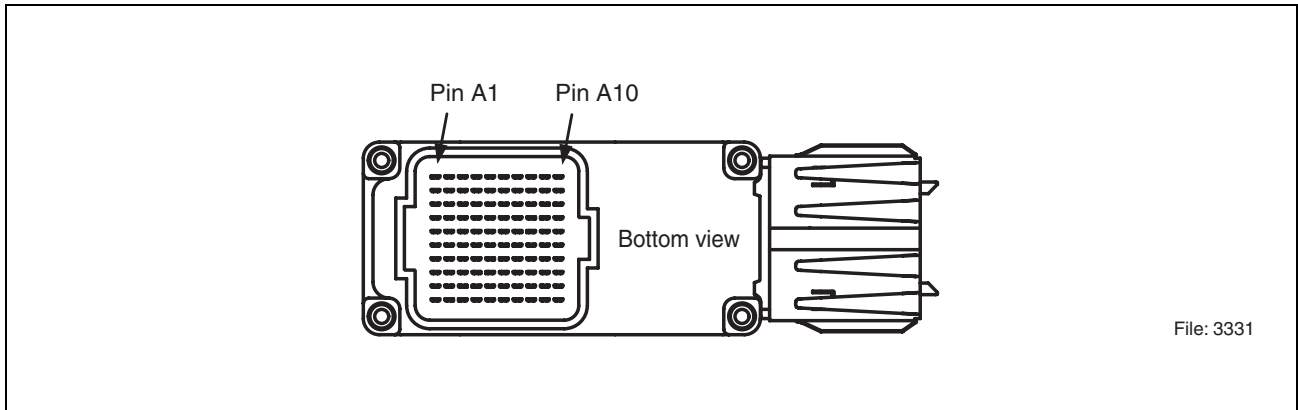


Figure 1 Pin Information Transmitter

Numbering Conventions Transmitter (bottom view)

|    | J               | I               | H               | G               | F               | E               | D               | C               | B               | A               |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 1  | V <sub>EE</sub> | DI05N           | DI05P           | DI06N           | DI06P           | DI07N           | DI07P           | DI08N           | DI08P           | V <sub>EE</sub> |
| 2  | DI04P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI09N           |
| 3  | DI04N           | V <sub>EE</sub> | Reserved        | Reserved        | t.b.l.o.        | t.b.l.o.        | Reserved        | Reserved        | V <sub>EE</sub> | DI09P           |
| 4  | DI01P           | V <sub>EE</sub> | Reserved        | Reserved        | t.b.l.o.        | t.b.l.o.        | Reserved        | Reserved        | V <sub>EE</sub> | DI12N           |
| 5  | DI01N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | t.b.l.o.        | t.b.l.o.        | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI12P           |
| 6  | DI02P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | t.b.l.o.        | -LE             | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI11N           |
| 7  | DI02N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | LCU             | LE              | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI11P           |
| 8  | DI03P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>IN</sub> | -RESET          | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI10N           |
| 9  | DI03N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DI10P           |
| 10 | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CC</sub> | V <sub>CC</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> |

This edge towards MPO connector

**Pin Description Transmitter**

| Symbol   | Level/Logic    | Description   |
|----------|----------------|---|
| $V_{CC}$ |                | Power supply voltage of laser driver  |
| $V_{IN}$ |                | CML: $V_{IN}$ = Reference supply (e.g. $V_{CC}$ )<br>LVDS, LVPECL: $V_{IN}$ = $V_{EE}$  |
| $V_{EE}$ |                | Ground  |
| LCU      | LVC MOS<br>Out | Laser Controller Up.<br>High = normal operation.<br>Low = laser fault or RESETlow.  |
| DlxxN    | Signal In      | Data Input #xx, inverted  |
| DlxxP    | Signal In      | Data Input #xx, non-inverted  |
| -RESET   | LVC MOS In     | High = laser diode array is active.<br>Low = switches laser diode array off.<br>This input has an internal pull-down to ensure laser eye safety switch off in case of unconnected RESETinput. |
| LE       | LVC MOS In     | Laser ENABLE. High active.<br>High = laser array is on if LE is also active.<br>Low = laser array is off. This input has an internal pull-up, therefore can be left open.                     |
| -LE      | LVC MOS In     | Laser ENABLE. Low active.<br>Low = laser array is on if LE is also active. This input has an internal pull-down, therefore can be left open.  |
| t.b.l.o. |                | to be left open   |
| Reserved |                | Reserved for future use   |

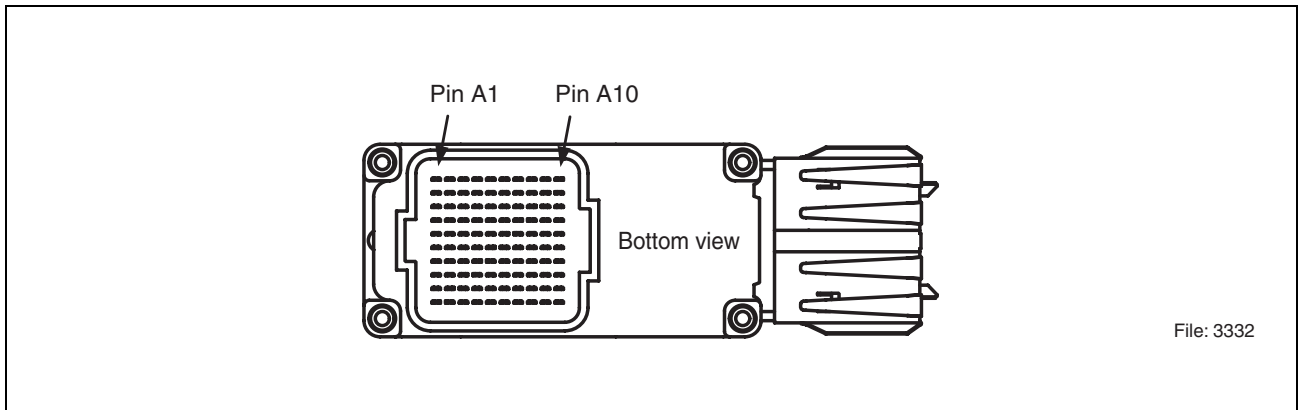


Figure 2 Pin Information Receiver

Numbering Conventions Receiver (bottom view)

|    | J               | I               | H               | G               | F                | E                | D               | C               | B               | A               |
|----|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|
| 1  | V <sub>EE</sub> | DO05P           | DO05N           | DO06P           | DO06N            | DO07P            | DO07N           | DO08P           | DO08N           | V <sub>EE</sub> |
| 2  | DO04N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub>  | V <sub>EE</sub>  | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO09P           |
| 3  | DO04P           | V <sub>EE</sub> | Reserved        | Reserved        | t.b.l.o.         | t.b.l.o.         | Reserved        | Reserved        | V <sub>EE</sub> | DO09N           |
| 4  | DO01N           | V <sub>EE</sub> | Reserved        | Reserved        | OEN              | ENSD             | Reserved        | Reserved        | V <sub>EE</sub> | DO12P           |
| 5  | DO01P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | SD01             | -SD12            | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO12N           |
| 6  | DO02N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | Reserved         | REFR             | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO11P           |
| 7  | DO02P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CCO</sub> | V <sub>CCO</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO11N           |
| 8  | DO03N           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CCO</sub> | V <sub>CCO</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO10P           |
| 9  | DO03P           | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CC</sub>  | V <sub>CC</sub>  | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | DO10N           |
| 10 | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>CC</sub>  | V <sub>CC</sub>  | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> | V <sub>EE</sub> |

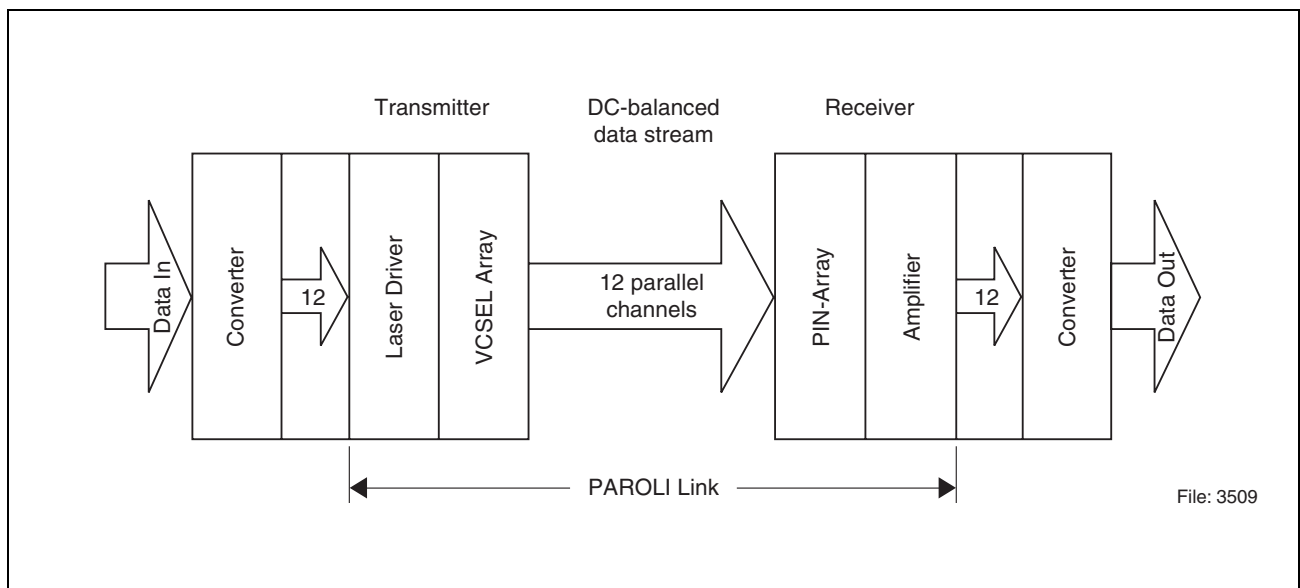
This edge towards MPO connector

**Pin Description Receiver**

| Symbol    | Level/Logic               | Description  |
|-----------|---------------------------|--|
| $V_{CC}$  |                           | Power supply voltage of pre amplifier and analog circuitry   |
| $V_{CCO}$ |                           | Power supply voltage of output stages  |
| REFR      |                           | Adjustment of output current by connecting external resistor to $V_{EE}$   |
| $V_{EE}$  |                           | Ground   |
| OEN       | LVC MOS In                | Output Enable High = normal operation.<br>Low = sets all Data Outputs to low.<br>This input has an internal pull-up which pulls to high level when this input is left open.              |
| ENSD      | LVC MOS In                | High = SD1 and –SD12 function enabled.<br>Low = SD1 and –SD12 are set to permanent active.<br>This input has an internal pull-up which pulls to high level when this input is left open. |
| SD1       | LVC MOS Out               | Signal Detect on fiber #1.<br>High = signal of sufficient AC power is present on fiber #1.<br>Low = signal on fiber #1 is insufficient.  |
| –SD12     | LVC MOS Out<br>low active | Signal Detect on fiber #12.<br>Low = signal of sufficient AC power is present on fiber #12.<br>High = signal on fiber #12 is insufficient.   |
| DOxxP     | CML Out                   | Data Output #xx, non-inverted  |
| DOxxN     | CML Out                   | Data Output #xx, inverted  |
| t.b.l.o.  |                           | to be left open  |
| Reserved  |                           | Reserved for future use  |

### Description

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI link consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module. The transmitter supports LVDS, CML and LVPECL differential signals. Two different receiver modules are available. Module V23832-R521-M101 is for LVDS electrical output only. This specification (V23832-R511-M101) describes a receiver for Infineon's adjustable CML output.



**Figure 3 Example of a PAROLI Link**

### Transmitter V23832-T2531-M101

The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible; LVPECL and CML is also supported because of the wide common input range). The electrical interface (LVDS, LVPECL or CML) is selected by the supply inputs  $V_{IN}$ . The data rate is up to 1250 Mbit/s for each channel. The transmitter module's min. data rate of 500 Mbit/s is specified for the CID<sup>1)</sup> worst case pattern (disparity 72) or any pattern with a lower disparity. The transmitter features active feedback of optical output power and extinction ratio, which guarantees a constant power budget.

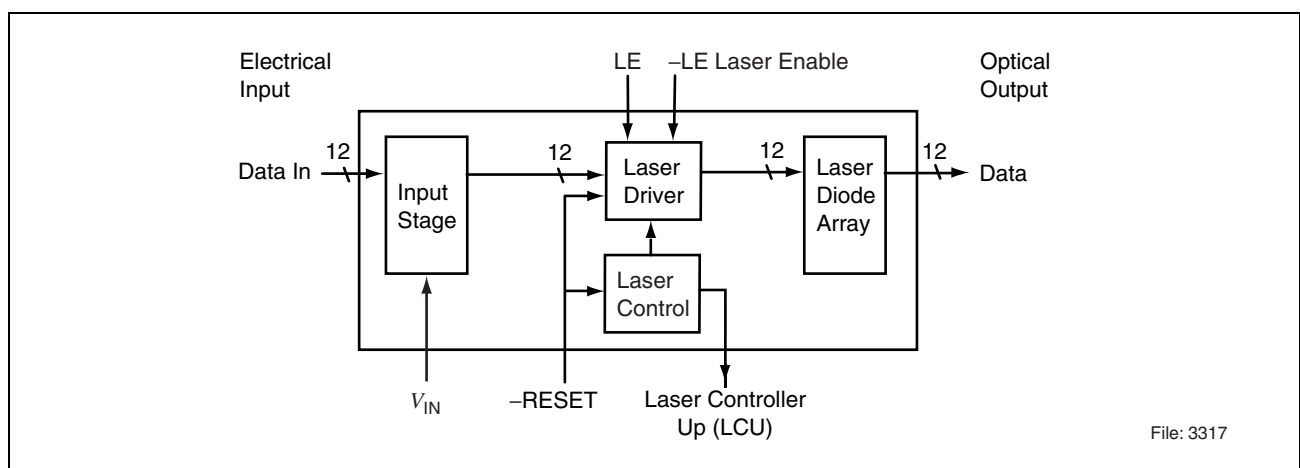
Unused channels can be forced to a quiescent state by applying e.g. a constant high level to the input stage of these channels. The integrated alerter circuit (see “**Laser Eye Safety Design Considerations**” on Page 12) will switch off the corresponding transmitter output, which results also in a reduced power consumption. Unused transmitter input channels can also be left open. The integrated swing detection circuit will assure a quiescent output state for these channels.

A logic low level at  $-\text{RESET}$  switches all laser outputs off. During power-up  $-\text{RESET}$  must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3.135 V level.

The Laser Controller Up (LCU) output is low if a laser fault is detected or  $-\text{RESET}$  is forced to low.

All non data signals have LVCMOS levels.

Transmission delay of the PAROLI system is  $\leq 1$  ns for the transmitter,  $\leq 1$  ns for the receiver and approximately 5 ns per meter for the fiber optic cable.



**Figure 4 Transmitter Block Diagram**

<sup>1)</sup> Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.



### Receiver V23832-R511-M101

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, trans impedance amplifiers, and gain amplifiers. The differential data outputs are Infineon's adjustable CML signals. A separate module (V23832-R521-M101) with LVDS output is also available. The output differential voltage (swing) is adjusted by an external resistor connected to the REFR module input, the output average is adjustable by external pull-up resistors.

The data rate is up to 1250 Mbit/s for each channel. The receiver module's min. data rate of 500 Mbit/s is specified for the CID<sup>1)</sup> worst case pattern (disparity 72) or any pattern with a lower disparity.

Additional Signal Detect outputs (SD1 active high / -SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at Output Enable sets all data outputs to logic low. SD outputs will not be effected.

All non data signals have LVCMOS levels. Transmission delay of the PAROLI system is  $\leq 1$  ns for the transmitter,  $\leq 1$  ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

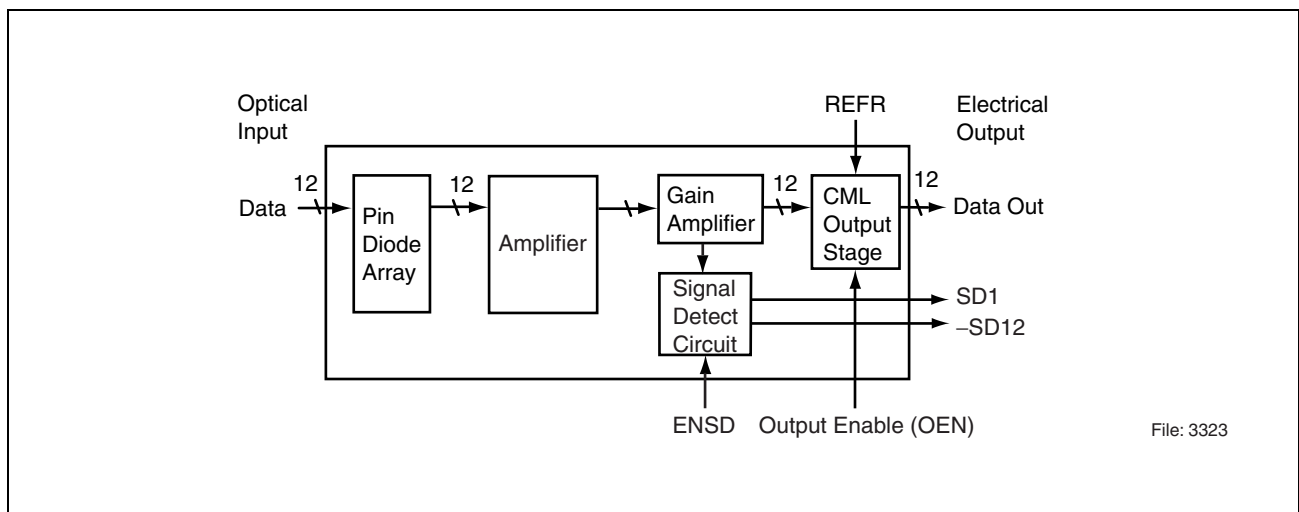


Figure 5 Receiver Block Diagram

<sup>1)</sup> Consecutive Identical Digit (CID) immunity test pattern for STM-N signals, ITU-T recommendation G.957 sec. II.

## Regulatory Compliance

The following table shows industry standard test methods and results obtained from the indicated test methods. (The overall system design will affect the electromagnetic interference (EMI), electrostatic discharge (ESD) and immunity).

| Feature   | Standard   | Comments   |
|---|--|--|
| ESD:<br>Electrostatic Discharge to the Electrical Pins (HBM)                | JEDEC Human Body Model (HBM) Test Method<br>EIA/JESD22-A114-B (MIL-STD 883D method 3015.7) | Class 1C   |
| Immunity:<br>Against Electrostatic Discharge (ESD) to the Module Receptacle | EN 61000-4-2<br>IEC 61000-4-2  | Discharges ranging from $\pm 2$ kV to $\pm 15$ kV on the front end/face-plate/receptacle cause no damage to module (under recommended mounting conditions).  |
| Immunity:<br>Against Radio Frequency Electromagnetic Field                  | EN 61000-4-3<br>IEC 61000-4-3  | With a field strength of 3 V/m, noise frequency ranges from 10 MHz to 2 GHz <sup>1)</sup> . No effect on module performance between the specification limits.  |
| Emission:<br>Electromagnetic Interference (EMI)                             | FCC 47 CFR Part 15, Class B<br>EN 55022 Class B<br>CISPR 22                                | Noise frequency range: 30 MHz to 18 GHz;<br>Radiated Emission does not exceed specified limits when measured inside a shielding enclosure with recommended cutout dimensions. Typically pass with > 11 dB margin to the limit (under recommended mounting conditions). |

<sup>1)</sup> This test covers high frequency bands of mobile phones.

## EMI Recommendations

EMI behavior of each PAROLI module revision is evaluated and measured - in order to ensure a good and sufficient EMI performance of all PAROLI modules. As the total EMI performance will also depend on system design and to avoid electromagnetic radiation exceeding the required limits set by the standards, please take note of the following recommendations.

## Description

When Gigabit switching components are found on a PCB (e.g. multiplexer, serializer-deserializer, clock data recovery, etc.), any opening of the chassis may leak radiation; this may also occur at chassis slots other than that of the device itself. Thus every mechanical opening or aperture should be as small as feasible and its length carefully considered.

On the board itself, every data connection should be an impedance matched line (e.g. micro strip, strip line or coplanar strip line). Data (D) and Data-not (Dn) should be routed symmetrically. Vias should be avoided. Where internal termination inside an IC or a PAROLI module is not present, a line terminating resistor must be provided.

The decision of how best to establish a ground depends on many boundary conditions. This decision may turn out to be critical for achieving lowest EMI performance. At RF frequencies the ground plane will always carry some amount of RF noise. Thus the ground and  $V_{CC}$  planes are often major radiators inside an enclosure.

As a general rule, for small systems such as PCI cards placed inside poorly shielded enclosures, the common ground scheme has often proven to be most effective in reducing RF emissions. In a common ground scheme, the PCI card becomes more equipotential with the chassis ground. As a result, the overall radiation will decrease. In a common ground scheme, it is strongly recommended to provide a proper contact between signal ground and chassis ground at every location where possible. This concept is designed to avoid hotspots which are places of highest radiation, caused when only a few connections between chassis and signal grounds exist. Compensation currents would concentrate at these connections, causing radiation.

However, as signal ground may be the main cause for parasitic radiation, connecting chassis ground and signal ground at the wrong place may result in enhanced RF emissions. For example, connecting chassis ground and signal ground at a front panel/bezel/chassis by means of a fiber optic module may result in a large amount of radiation especially where combined with an inadequate number of grounding points between signal ground and chassis ground. Thus the fiber optic module becomes a single contact point increasing radiation emissions. Even a capacitive coupling between signal ground and chassis ground may be harmful if it is too close to an opening or an aperture. For a number of systems, enforcing a strict separation of signal ground from chassis ground may be advantageous, providing the housing does not present any slots or other discontinuities. This separate ground concept seems to be more suitable in huge systems.

The return path of RF current must also be considered. Thus a split ground plane between Tx and Rx paths may result in severe EMI problems.

The bezel opening for a transceiver should be sized so that all contact springs of the transceiver cage make good electrical contact with the face plate.

Please consider that the PCB may behave like a dielectric waveguide. With a dielectric constant of 4, the wavelength of the harmonics inside the PCB will be half of that in free space. Thus even the smallest PCBs may have unexpected resonances.

## Laser Eye Safety

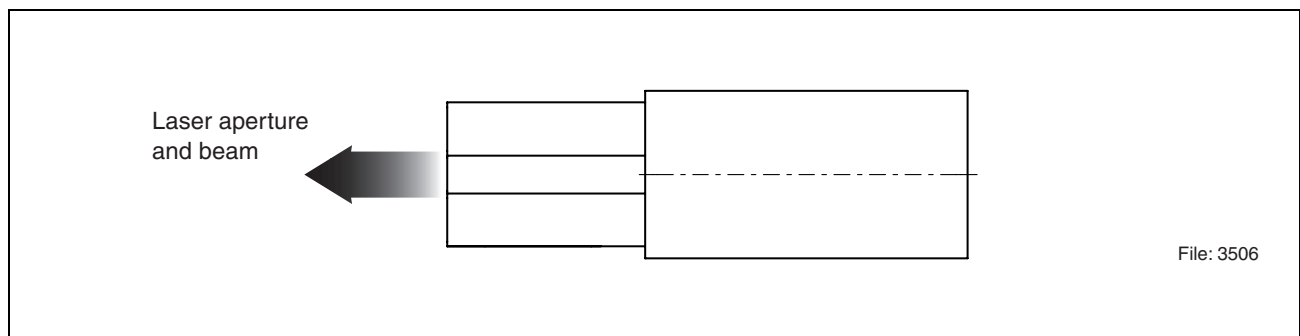
The transmitter of the AC coupled Parallel Optical Link (PAROLI) is an IEC 60825-1 Amend. 2 Class 1M laser product. It complies with FDA performance standards (21 CFR 1040.10 and 1040.11) for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The PAROLI module must be operated under the specified operating conditions (supply voltage can be adjusted between 3.0 V and 3.6 V) under any circumstances to ensure laser eye safety.

### Class 1M Laser Product

**Attention: Invisible laser radiation. Do not view directly with optical instruments.**

*Note: Any modification of the module will be considered an act of “manufacturing”, and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).*



**Figure 6 Laser Emission**

## Laser Eye Safety Design Considerations

To ensure laser eye safety for all input data patterns each channel is controlled internally and will be switched off if the laser eye safety limits are exceeded. A channel alerter switches the respective data channel output off if the input duty cycle permanently exceeds 57% (switching range 57 % min. - 65 % max.). The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.

The minimum alerter response time is 1  $\mu$ s with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1  $\mu$ s, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.

All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

**Laser Eye Safety Measurement Conditions**

| Laser Data                                   | Symbol           | Values  |      |      | Unit     | Condition                             |
|--|------------------|---------|------|------|----------|---------------------------------------|
|  |                  | min.    | typ. | max. |          |                                       |
| Center wavelength                            | $\lambda_c$      | 830     | 850  | 860  | nm       | $T_{case}$ 0...80°C                   |
| Array size                                   |                  |         | 12   |      | channels |                                       |
| Divergence angle/<br>Numerical<br>Aperture   | $\Theta/NA$      | 44/0.22 |      |      | °/rad    | $\Theta$ full /<br>NA half angle      |
| IEC class 1M<br>Accessible<br>Emission Limit | AEL              |         |      | 6.36 | dBm      | 7 mm aperture<br>@ 100 mm<br>distance |
| Applying penalties<br>(safety margin)        | $\Delta P_{opt}$ |         |      | 4.2  | dB       |                                       |
| Test limit                                   |                  |         |      | 2.16 | dBm      |                                       |

## Technical Data

### Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Performance between absolute maximum ratings and recommended operating conditions is not guaranteed.

| Parameter   | Symbol          | Limit Values |              | Unit |
|---|-----------------|--------------|--------------|------|
|   |                 | min.         | max.         |      |
| Supply Voltage  | $V_{CC}-V_{EE}$ | -0.3         | 4.5          | V    |
| Data/Control Input Levels <sup>1)</sup>   | $V_{IN}$        | -0.5         | $V_{CC}+0.5$ | V    |
| Data Input Differential Voltage <sup>2)</sup>   | $ V_{ID} $      |              | 2.0          | V    |
| Operating Case Temperature <sup>3)</sup>  | $T_{case}$      | 0            | 90           | °C   |
| Storage Ambient Temperature   | $T_{stg}$       | -40          | 100          | °C   |
| Relative Humidity (non condensing)  |                 | 5            | 95           | %    |
| ESD Resistance<br>(all pins to $V_{EE}$ , human body model) <sup>4)</sup><br>(see table “Regulatory Compliance” on Page 10) |                 |              | 1            | kV   |

<sup>1)</sup> At Data and LVCMOS inputs.

<sup>2)</sup>  $|V_{ID}| = |(\text{input voltage of non-inverted input minus input voltage of inverted input})|$ .

<sup>3)</sup> Measured at case temperature reference point (see **Figure 18** on **Page 31**).

<sup>4)</sup> To avoid electrostatic damage, handling cautions similar to those used for MOS devices must be observed.

**Recommended Operating Conditions<sup>1)</sup>**

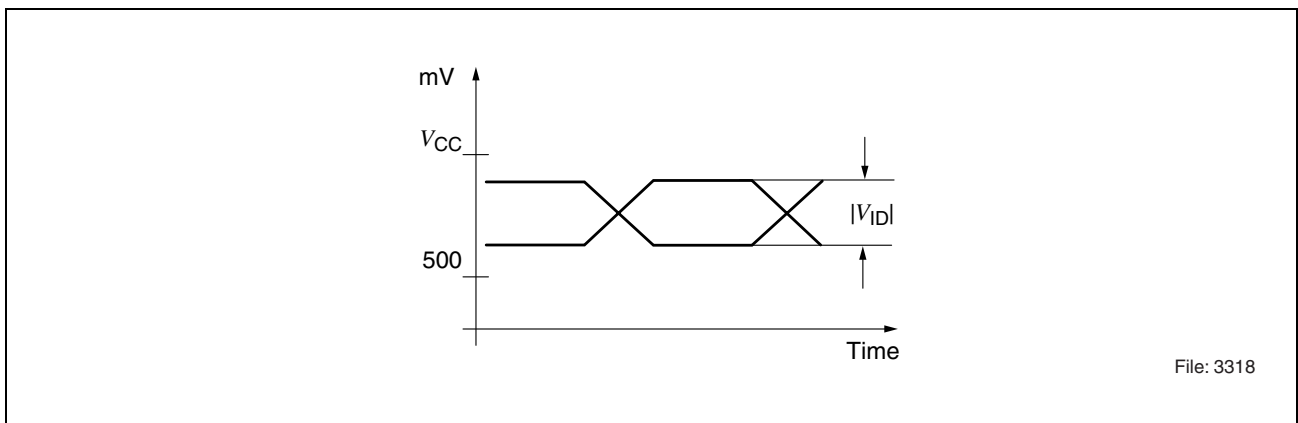
| Parameter   | Symbol                           | Values   |      |                                 | Unit |
|---|----------------------------------|----------|------|---------------------------------|------|
|   |                                  | min.     | typ. | max.                            |      |
| <b>Transmitter</b>  |                                  |          |      |                                 |      |
| Operating Case Temperature  | $T_{case}$                       | 0        | 45   | 80                              | °C   |
| Power Supply Voltage  | $V_{CC}$                         | 3.135    | 3.3  | 3.6                             | V    |
| Noise on Power Supply <sup>2)</sup>                                   | $N_{PS}$                         |          |      | 200                             | mV   |
| Data Input Voltage Range (DC-coupled) <sup>3), 4)</sup>               | $V_{DATAI}$                      | 500      |      | $V_{CC}$                        | mV   |
| Data Input Differential Voltage (DC- or AC-coupled) <sup>4), 5)</sup> | $ V_{ID} $                       | 80       |      | 1000                            | mV   |
| Data Input Skew <sup>6)</sup>   | $t_{SPN}$                        |          |      | $0.5 \times t_{R-DI}, t_{F-DI}$ | ps   |
| Data Input Rise/Fall Time <sup>7)</sup>                               | $t_{R-DI}, t_{F-DI}$             | 50       |      | 360                             | ps   |
| LVC MOS Input High Voltage  | $V_{LVC MOSIH}$                  | 2.0      |      | $V_{CC}$                        | V    |
| LVC MOS Input Low Voltage   | $V_{LVC MOSIL}$                  | $V_{EE}$ |      | 0.8                             | V    |
| LVC MOS Input Rise/Fall Time <sup>8)</sup>                            | $t_{R-LVC MOSI}, t_{F-LVC MOSI}$ |          |      | 20                              | ns   |

**Receiver**

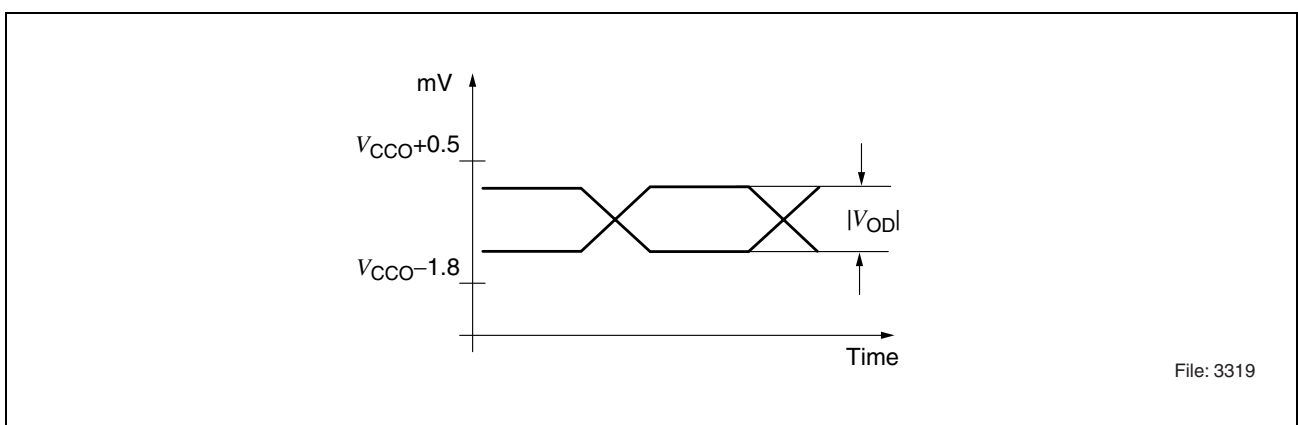
|   |                                  |               |     |               |    |
|---|----------------------------------|---------------|-----|---------------|----|
| Power Supply Voltages   | $V_{CC}, V_{CCO}$                | 3.0           | 3.3 | 3.6           | V  |
| Noise on Power Supply <sup>2)</sup>                                 | $N_{PS}$                         |               |     | 200           | mV |
| Output Current <sup>9)</sup>  | $I_{out}$                        | 3             |     | 9             | mA |
| Output Voltage (DC-coupled) <sup>10)</sup>                          | $V_{out}$                        | $V_{CCO}-1.8$ |     | $V_{CCO}+0.5$ | V  |
| Output Differential Voltage (DC- or AC-coupled) <sup>10), 11)</sup> | $ V_{OD} $                       | 80            |     | 800           | mV |
| Output Load RC Time Constant  | $t_{RC}$                         |               |     | 150           | ps |
| LVC MOS Input High Voltage  | $V_{LVC MOSIH}$                  | 2.0           |     | $V_{CC}$      | V  |
| LVC MOS Input Low Voltage   | $V_{LVC MOSIL}$                  | $V_{EE}$      |     | 0.8           | V  |
| LVC MOS Input Rise/Fall Time <sup>8)</sup>                          | $t_{R-LVC MOSI}, t_{F-LVC MOSI}$ |               |     | 20            | ns |
| Optical Input Rise/Fall Time <sup>12)</sup>                         | $t_{R-OI}, t_{F-OI}$             |               |     | 400           | ps |
| Input Extinction Ratio  | ER                               | 6.0           |     |               | dB |
| Input Center Wavelength   | $\lambda_C$                      | 830           |     | 860           | nm |

Voltages refer to  $V_{EE} = 0$  V.

- 1) Recommended range of input parameters for specified module functional performance.
- 2) Noise frequency is 1 kHz to  $f_{max}$ , where  $f_{max}$  is equal to the maximum data rate in units of MHz. E.g. for a maximum data rate of 2700 Mbit/s,  $f_{max} = 2700$  MHz. Power supply noise is defined with the recommended filter in place at the supply side of the filtering circuit (see **Figure 9** on **Page 17**).
- 3) The input stage can also be AC-coupled.
- 4) Input level diagram: see **Figure 7** on **Page 16**.
- 5)  $|V_{ID}| = |(\text{input voltage of non-inverted input minus input voltage of inverted input})|$ .
- 6) Skew between positive and negative inputs measured at 50% level.
- 7) 20% - 80% level.
- 8) Measured between 0.8 V and 2.0 V.
- 9)  $I_{out} \approx 10 \cdot 1.15 V / R_{external}$ . Resistor  $R_{external}$  to be connected externally between REFR and  $V_{EE}$ .
- 10) Output level diagram: see **Figure 8** on **Page 16**.
- 11)  $|V_{OD}| = I_{out} \cdot (300 \Omega \parallel R_{LOAD})$ . The output current range of 3 mA to 9 mA corresponds to  $|V_{OD}| = 130$  mV to 385 mV for  $R_{LOAD} = 50 \Omega$ .  
 $|V_{OD}| = |(\text{output voltage of non-inverted output minus output voltage of inverted output})|$ .
- 12) 20% - 80% level. Non filtered values.



**Figure 7** Input Level Diagram, DC-coupling

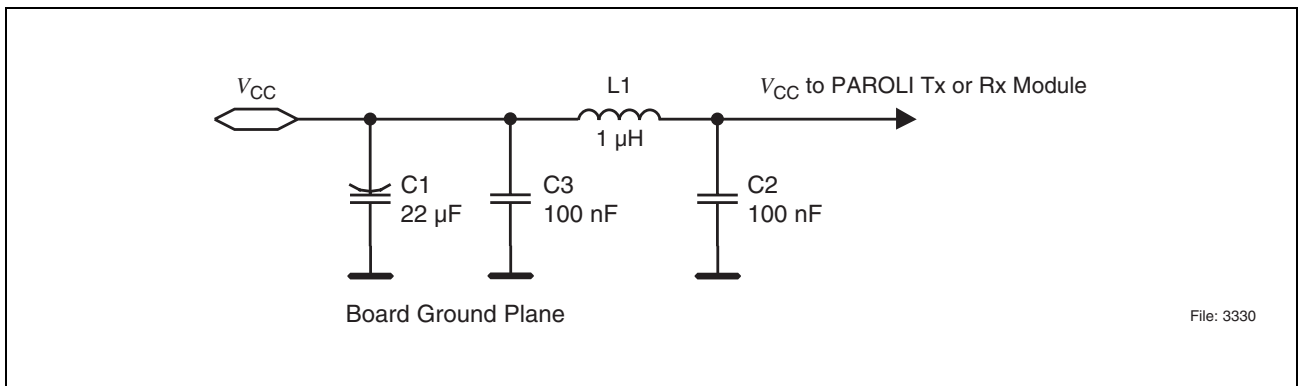


**Figure 8** Output Level Diagram, DC-coupling

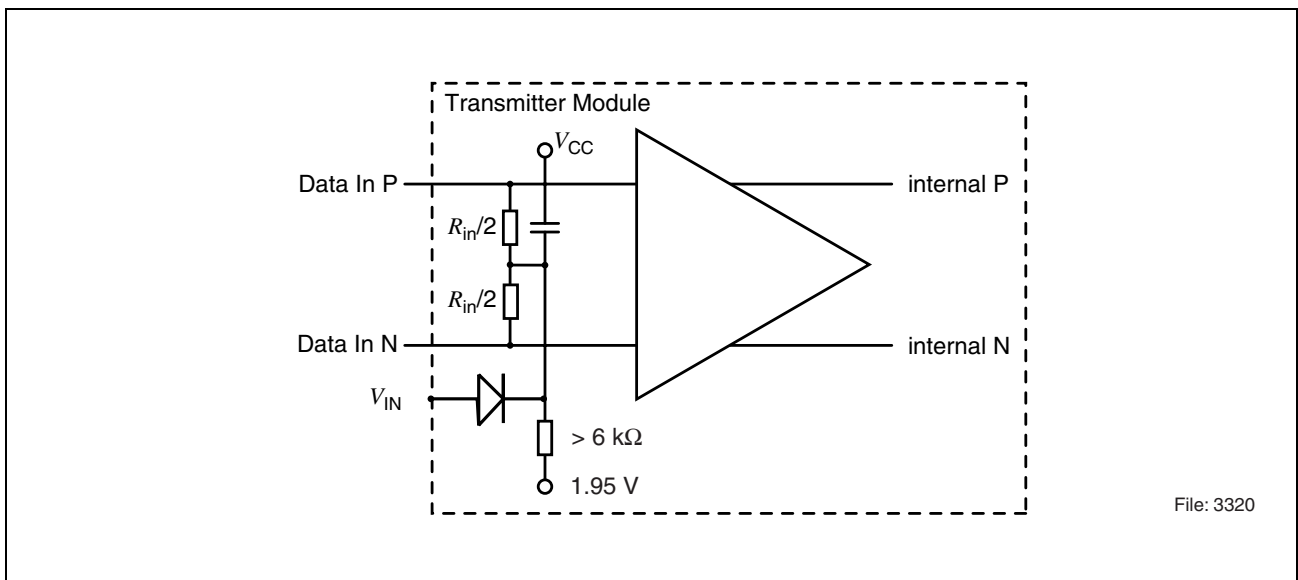


### Recommended Power Supply Filtering

A power supply filtering is recommended for the transmitter and the receiver module. A possible filtering scheme is shown in **Figure 9**. The module signal and chassis ground refer to a common ground plane, which can be contacted to the PCB ground by the mounting screws (see **Figure 17 “PCB Layout” on Page 28**).



**Figure 9** Filtering Scheme



**Figure 10** Transmitter - Input Stage

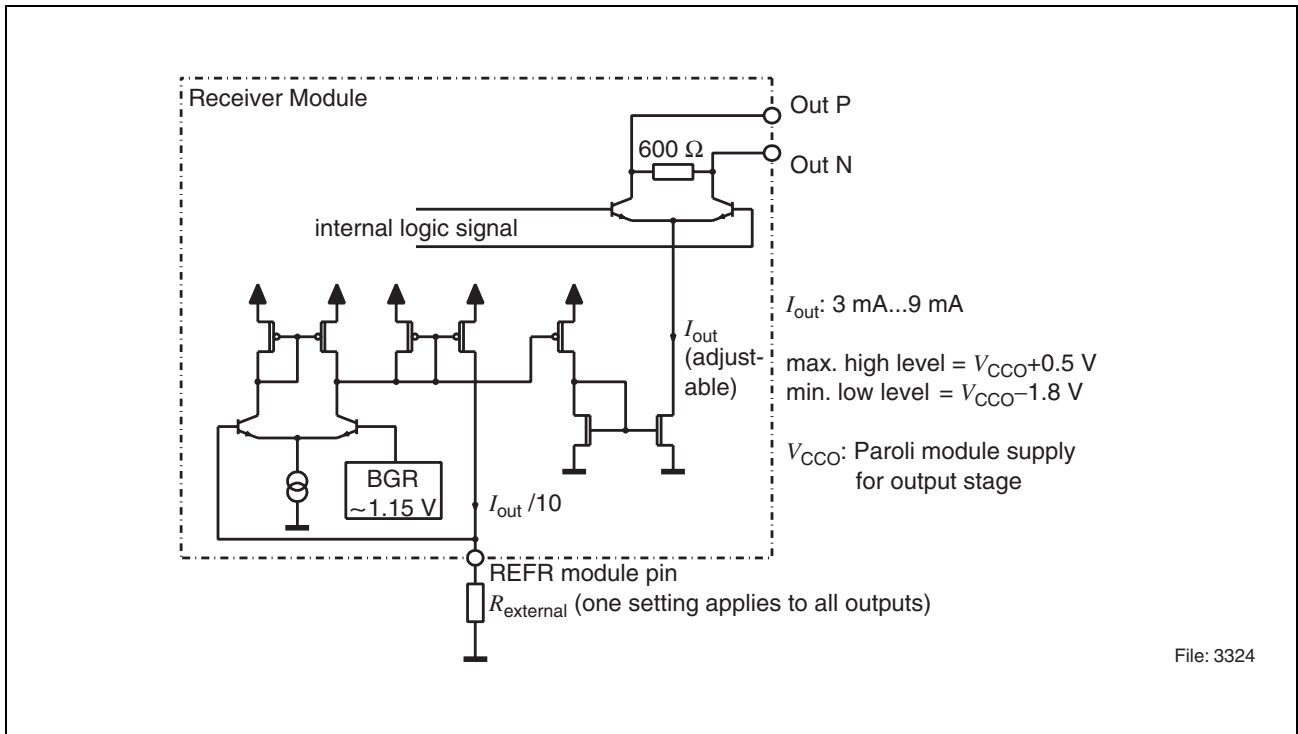


Figure 11 Receiver - CML Output Stage

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

### Transmitter Electrical Characteristics

| Parameter                                       | Symbol          | Values            |      |      | Unit     |
|---|-----------------|-------------------|------|------|----------|
|   |                 | min.              | typ. | max. |          |
| Supply Current <sup>1)</sup>                    | $I_{CC}$        |                   | 400  | 450  | mA       |
| Power Consumption <sup>1)</sup>                 | $P$             |                   | 1.3  | 1.6  | W        |
| Data Rate per Channel                           | DR              | 500 <sup>2)</sup> |      | 1250 | Mbit/s   |
| LVC MOS Output Voltage Low                      | $V_{LVC MOSOL}$ |                   |      | 0.4  | V        |
| LVC MOS Output Voltage High                     | $V_{LVC MOSOH}$ | 2.5               |      |      | V        |
| LVC MOS Input Current High/Low                  | $I_{LVC MOSI}$  | -100              |      | 100  | $\mu$ A  |
| LVC MOS Output Current High <sup>3)</sup>       | $I_{LVC MOSOH}$ |                   |      | 0.5  | mA       |
| LVC MOS Output Current Low <sup>4)</sup>        | $I_{LVC MOSOL}$ |                   |      | 4.0  | mA       |
| Data Differential Input Impedance <sup>5)</sup> | $R_{IN}$        | 80                | 100  | 120  | $\Omega$ |

<sup>1)</sup> Measured at the recommended case temperature of  $T_{case} = 45^{\circ}C$ . For  $T_{case} = 0^{\circ}C$  a decrease of approximately 10% and for  $T_{case} = 80^{\circ}C$  an increase of approximately 15% can be expected.

<sup>2)</sup> Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity. The minimum data rate depends on the disparity of the used data pattern. For example, a regular clock signal (1-0 sequence) can be transmitted down to a data rate as low as 1 Mbit/s.

<sup>3)</sup> Source current.

<sup>4)</sup> Sink current.

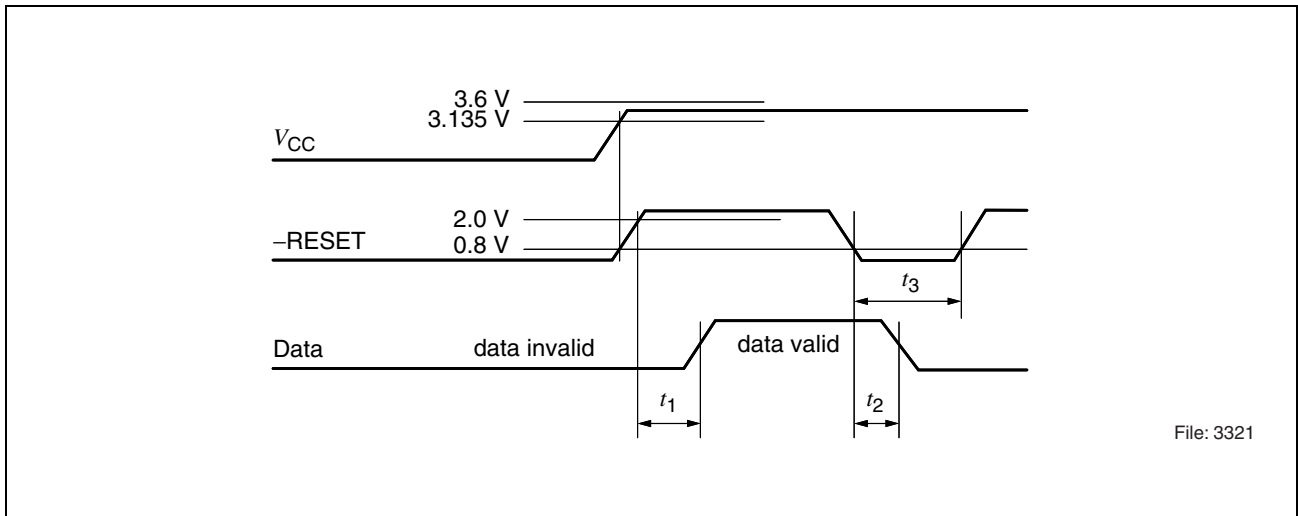
<sup>5)</sup> Data input stage.

**Transmitter Electro-Optical Characteristics**

| Parameter  | Symbol          | Values              |                     |       | Unit  |
|--|-----------------|---------------------|---------------------|-------|-------|
|  |                 | min.                | typ.                | max.  |       |
| Optical Rise Time <sup>1)</sup>                  | $t_R$           |                     |                     | 200   | ps    |
| Optical Fall Time <sup>1)</sup>                  | $t_F$           |                     |                     | 200   | ps    |
| Total Jitter <sup>2), 3)</sup>                   | TJ              |                     |                     | 0.284 | UI    |
| Deterministic Jitter <sup>3), 4)</sup>           | DJ              |                     |                     | 0.1   | UI    |
| Channel-to-channel skew <sup>5)</sup>            | $t_{CSK}$       |                     |                     | 100   | ps    |
| Launched Average Power <sup>6)</sup>             | $P_{AVG}$       | -8.0                | -5.0                | -3.0  | dBm   |
| Launched Power Shutdown                          | $P_{SD}$        |                     |                     | -30.0 | dBm   |
| Center Wavelength <sup>7)</sup>                  | $\lambda_C$     | 830                 | 850                 | 860   | nm    |
| Spectral Width (rms) <sup>8)</sup>               | $\Delta\lambda$ |                     | 0.35                | 0.65  | nm    |
| Relative Intensity Noise <sup>9)</sup>           | RIN             |                     |                     | -117  | dB/Hz |
| Extinction Ratio (dynamic)                       | ER              | 6.0                 |                     |       | dB    |
| Optical Modulation Amplitude <sup>10), 11)</sup> | OMA             | 0.19 <sup>12)</sup> | 0.46 <sup>13)</sup> |       | mW    |
| Eye mask compliance                              |                 | GBE                 |                     |       |       |

Electro-optical parameters valid for each channel and measured at the highest specified data rate.  
 All optical parameters are measured with a 62.5  $\mu\text{m}$  multimode fiber.

- <sup>1)</sup> 20% - 80% level, non filtered values.
- <sup>2)</sup> The Total Jitter (TJ) is composed of Random Jitter (RJ) and Deterministic Jitter (DJ) according to:  
 $TJ = RJ (14 \text{ Sigma value}) + DJ$ .  
 The TJ is specified at a BER of  $10^{-12}$  from TP1 to TP2 according to IEEE 802.3, sec. 38.5.  
 The RJ is measured at the 50% level of the optical signal as the mean of the rising and falling edge measurement value.
- <sup>3)</sup> UI (Unit Interval) is equal to the length of one bit. For example, 2.72 Gbit/s corresponds to 368 ps.
- <sup>4)</sup> The DJ consists of Duty Cycle Distortion and Data Dependent Jitter and is measured according to IEEE 802.3 using a K28.5 pattern.
- <sup>5)</sup> With input channel-to-channel skew 0 ps and a maximum data channel-to-channel average deviation and swing deviation of 5%.
- <sup>6)</sup> The specified output power is compliant with IEC 60825-1, Amendment 2, Class 1M Accessible Emission Limits (AEL).
- <sup>7)</sup> Wavelength is measured according to IEEE 802.3, sec. 38.6.1.
- <sup>8)</sup> Spectral width is measured according to IEEE 802.3, sec. 38.6.1.
- <sup>9)</sup> RIN is measured according to IEEE 802.3, sec. 38.6.4.
- <sup>10)</sup> Peak to peak values.
- <sup>11)</sup> OMA is defined as the difference of the optical high state ('1') and the optical low state ('0'):  
 $OMA = P_{opt}('1') - P_{opt}('0')$ .
- <sup>12)</sup> Corresponds to a minimum extinction ratio of 6 dB.
- <sup>13)</sup> Corresponds to a typical extinction ratio of 8 dB.



File: 3321

Figure 12 Timing Diagram

| Parameter                         | Symbol | Values |      |      | Unit |
|-----------------------------------|--------|--------|------|------|------|
|                                   |        | min.   | typ. | max. |      |
| -RESET on delay time              | $t_1$  |        | 15   | 50   | ms   |
| -RESET off delay time             | $t_2$  |        | 100  | 500  | ns   |
| -RESET low duration <sup>1)</sup> | $t_3$  | 10     |      |      | μs   |

<sup>1)</sup> Only when not used as power on reset. At any failure recovery, -RESET must be brought to low level for at least  $t_3$ .

**Receiver Electrical Characteristics**

| Parameter                                   | Symbol                     | Values |                      |                      | Unit    |
|---|----------------------------|--------|----------------------|----------------------|---------|
|   |                            | min.   | typ.                 | max.                 |         |
| Supply Current <sup>1)</sup>                | $I_{CC}$                   |        | 170<br>+15 $I_{out}$ | 200<br>+15 $I_{out}$ | mA      |
| Power Consumption <sup>1), 2)</sup>         | $P$                        |        | 0.7                  | 0.9                  | W       |
| Data Output Rise/Fall Time <sup>3)</sup>    | $t_{R-DO}$ ,<br>$t_{F-DO}$ |        |                      | 250                  | ps      |
| LVC MOS Output Voltage Low                  | $V_{LVC MOSOL}$            |        |                      | 400                  | mV      |
| LVC MOS Output Voltage High                 | $V_{LVC MOSOH}$            | 2500   |                      |                      | mV      |
| LVC MOS Input Current High/Low              | $I_{LVC MOSI}$             | -100   |                      | 100                  | $\mu$ A |
| LVC MOS Output Current High <sup>4)</sup>   | $I_{LVC MOSOH}$            |        |                      | 0.5                  | mA      |
| LVC MOS Output Current Low <sup>5)</sup>    | $I_{LVC MOSOL}$            |        |                      | 4.0                  | mA      |
| Total Jitter <sup>6), 7), 8), 9), 10)</sup> | TJ                         |        |                      | 0.33                 | UI      |
| Deterministic Jitter <sup>6), 9), 11)</sup> | DJ                         |        |                      | 0.08                 | UI      |
| Channel-to-channel skew <sup>12)</sup>      | $t_{CSK}$                  |        |                      | 100                  | ps      |

- <sup>1)</sup> Typical value is measured at  $T_{case} = 45^{\circ}\text{C}$  and 3.3 V, maximum value is measured at  $T_{case} = 80^{\circ}\text{C}$  and 3.6 V.
- <sup>2)</sup> Calculated for  $I_{out} = 3$  mA.
- <sup>3)</sup> Measured between 20% and 80% level. Maximum value is related to a maximum RC load time constant of  $t_{RC} = 150$  ps.
- <sup>4)</sup> Source current.
- <sup>5)</sup> Sink current.
- <sup>6)</sup> With no optical input jitter.
- <sup>7)</sup> Measured with an optical input power of 3 dB above minimum receiver sensitivity.
- <sup>8)</sup> Unused channels shall be terminated by 50  $\Omega$ .
- <sup>9)</sup> UI (Unit Interval) is equal to the length of one bit. For example, 2.72 Gbit/s corresponds to 368 ps.
- <sup>10)</sup> The Total Jitter (TJ) is the sum from Random Jitter (RJ) and Deterministic Jitter (DJ) according to:  $TJ = RJ$  (14 Sigma value) + DJ.  
The TJ is specified at a BER of  $10^{-12}$  from TP3 to TP4 according to IEEE 802.3, sec. 38.5.  
The RJ is measured at the 50% level of the optical signal as the mean of the rising and falling edge RJ measurement value.
- <sup>11)</sup> The DJ consists of Duty Cycle Distortion and Data Dependent Jitter and is measured according to IEEE 802.3 using a K28.5 pattern.
- <sup>12)</sup> With input channel-to-channel skew 0 ps.

### Receiver Electro-Optical Characteristics

| Parameter                                  | Symbol                  | Values              |       | Unit   |
|--|-------------------------|---------------------|-------|--------|
|  |                         | min.                | max.  |        |
| Data Rate Per Channel                      | DR                      | 500 <sup>1)</sup>   | 1250  | Mbit/s |
| Sensitivity (Average Power) <sup>2)</sup>  | $P_{IN}$                |                     | -16.0 | dBm    |
| Optical Modulation Amplitude <sup>3)</sup> | OMA                     | 0.030 <sup>4)</sup> |       | mW     |
| Saturation (Average Power) <sup>5)</sup>   | $P_{SAT}$               | -2.0                |       | dBm    |
| Signal Detect Assert Level <sup>6)</sup>   | $P_{SDA}$               |                     | -17.0 | dBm    |
| Signal Detect Deassert Level <sup>6)</sup> | $P_{SDD}$               | -27.0               |       | dBm    |
| Signal Detect Hysteresis <sup>6)</sup>     | $P_{SDA}$<br>$-P_{SDD}$ | 1.0                 | 4.0   | dB     |
| Return Loss of Receiver <sup>7)</sup>      | ORL                     | 12                  |       | dB     |

Electro-optical parameters valid for each channel and measured at the highest specified data rate.  
All optical parameters are measured with a 62.5  $\mu\text{m}$  multimode fiber.

- <sup>1)</sup> Specified for CID worst case pattern (disparity 72) or any pattern with a smaller disparity. The minimum data rate depends on the disparity of the used data pattern. For example, a regular clock signal (1-0 sequence) can be received down to a data rate as low as 6 Mbit/s.
- <sup>2)</sup> Sensitivity is measured for  $\text{BER} = 10^{-12}$  with a Pseudo Random Bit sequence of length  $2^{23}-1$  (PRBS23) and a test pattern source with RIN of  $-117$  dB/Hz or better. Sensitivity is specified for the worst case extinction ratio and maximum cross talk possibility. The maximum crosstalk possibility is defined as the "victim" receiver channel operating at its sensitivity limit and the neighboring channels operating at 6 dB higher incident optical power.
- <sup>3)</sup> Peak to peak value.
- <sup>4)</sup> Corresponds to a maximum sensitivity (average power) of  $-16$  dBm at an extinction ratio of 6 dB.
- <sup>5)</sup> Saturation is specified with a Pseudo Random Bit sequence of length  $2^{23}-1$  (PRBS23) and  $\text{ER} \geq 6$  dB.
- <sup>6)</sup>  $P_{SDA}$ : Average optical power when SD switches from inactive to active.  
 $P_{SDD}$ : Average optical power when SD switches from active to inactive.
- <sup>7)</sup> Return loss is specified as the ration of the received optical power to the reflected optical power back into the link fiber.

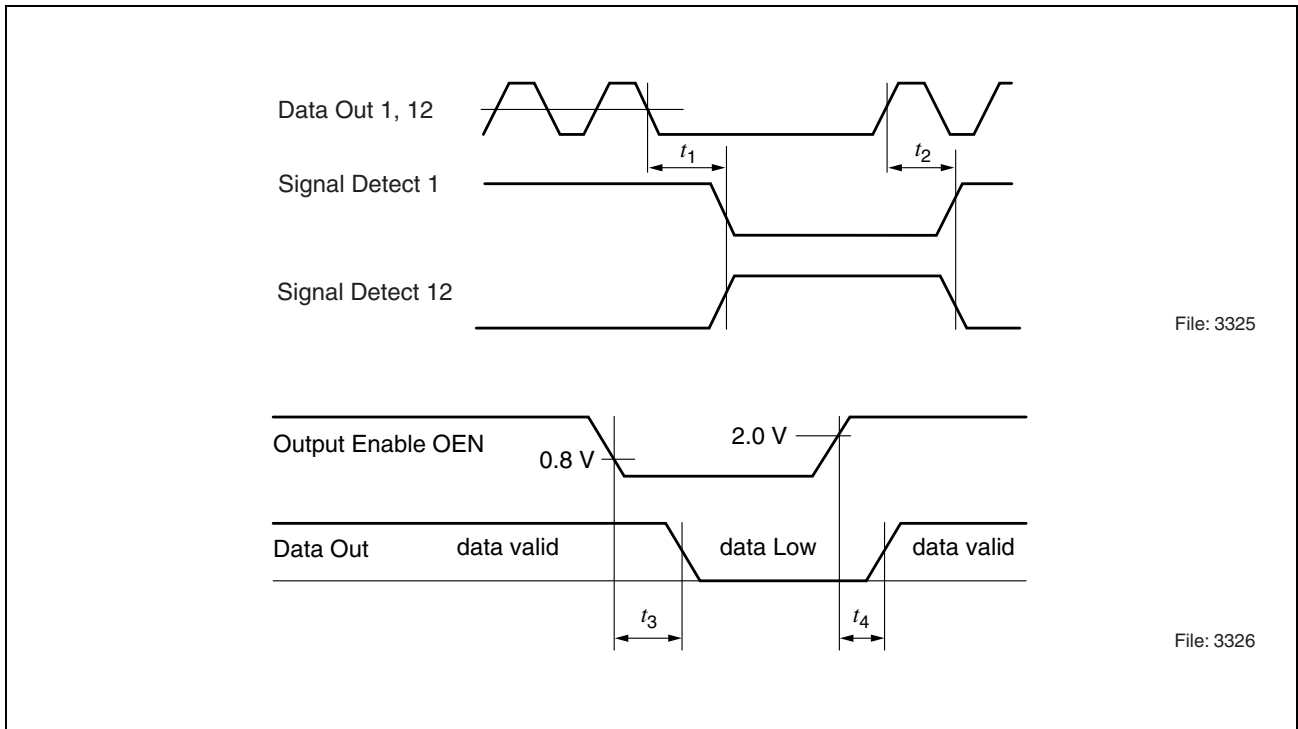
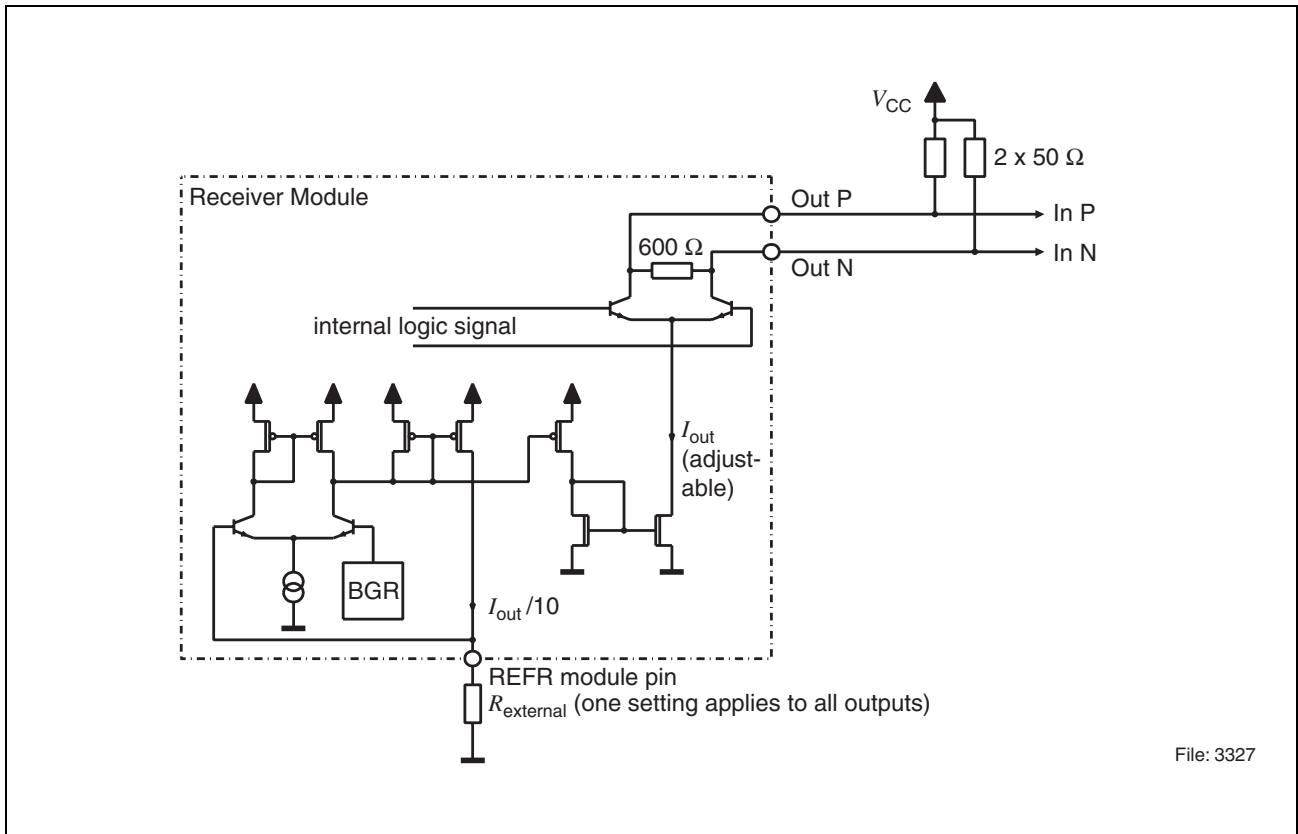


Figure 13 Timing Diagrams

| Parameter                    | Symbol | Values |      |      | Unit          |
|------------------------------|--------|--------|------|------|---------------|
|                              |        | min.   | typ. | max. |               |
| Signal Detect Deassert Time  | $t_1$  |        | 3    | 10   | $\mu\text{s}$ |
| Signal Detect Assert Time    | $t_2$  |        | 2    | 10   | $\mu\text{s}$ |
| Output Enable off Delay Time | $t_3$  |        | 14   | 20   | $\mu\text{s}$ |
| Output Enable on Delay Time  | $t_4$  |        | 18   | 20   | $\mu\text{s}$ |





File: 3327

Figure 14 Interfacing to CML

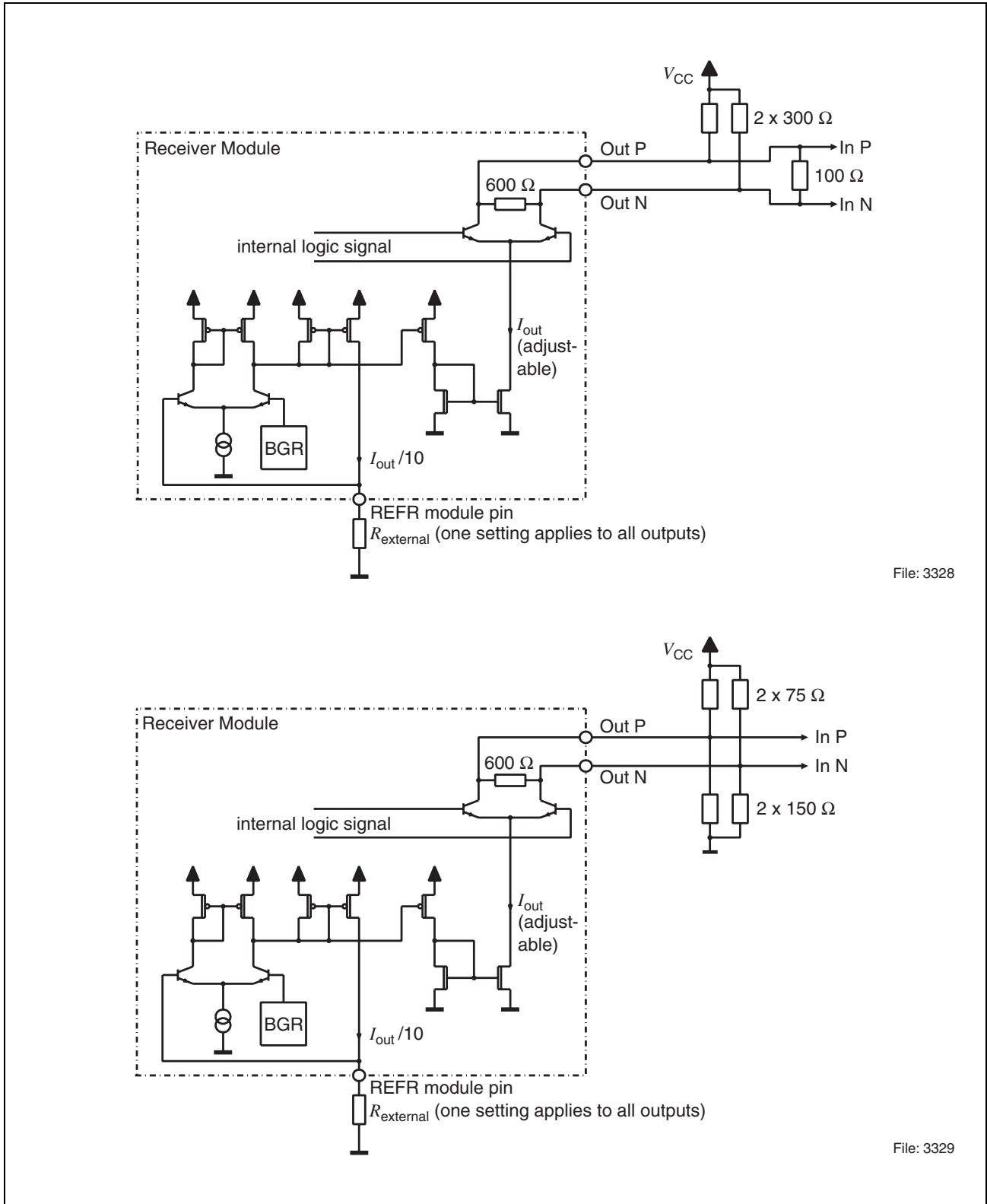


Figure 15 Interfacing to LVPECL

### Host Face-Plate Layout for Panel Accessed Modules

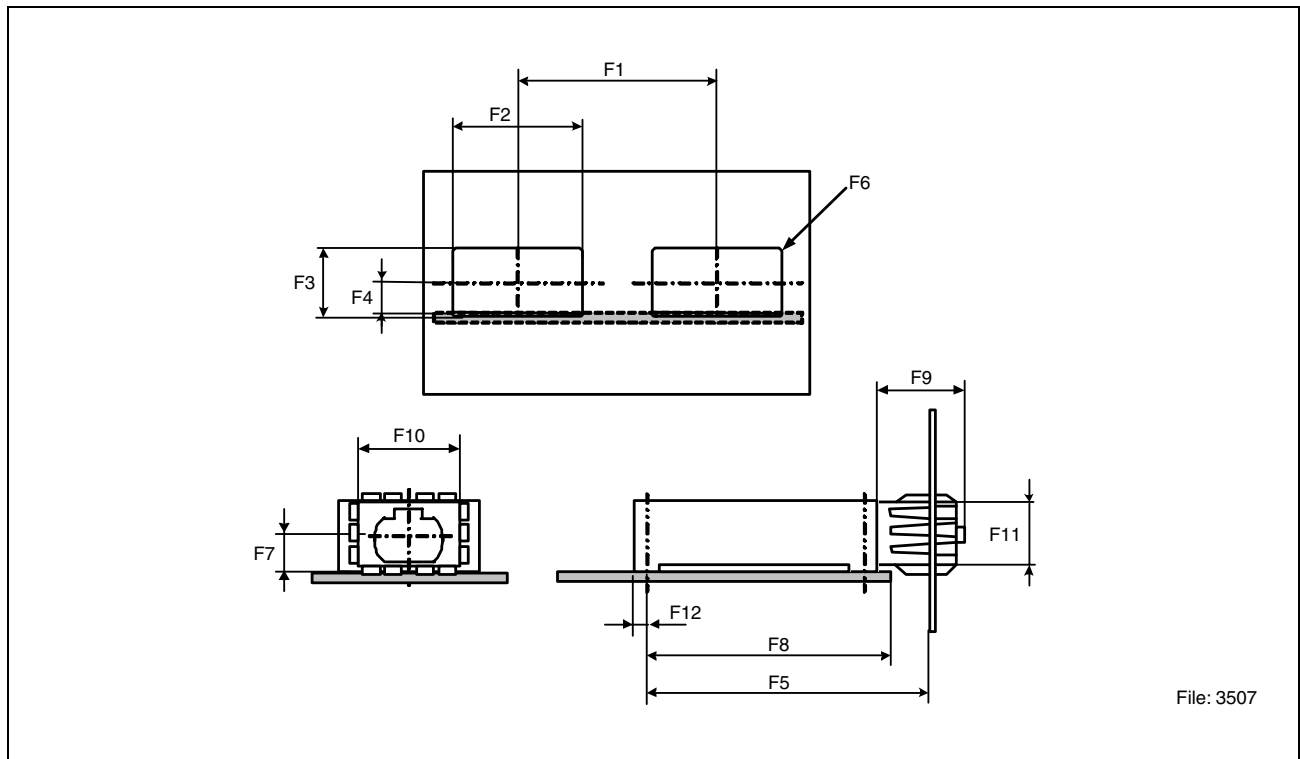
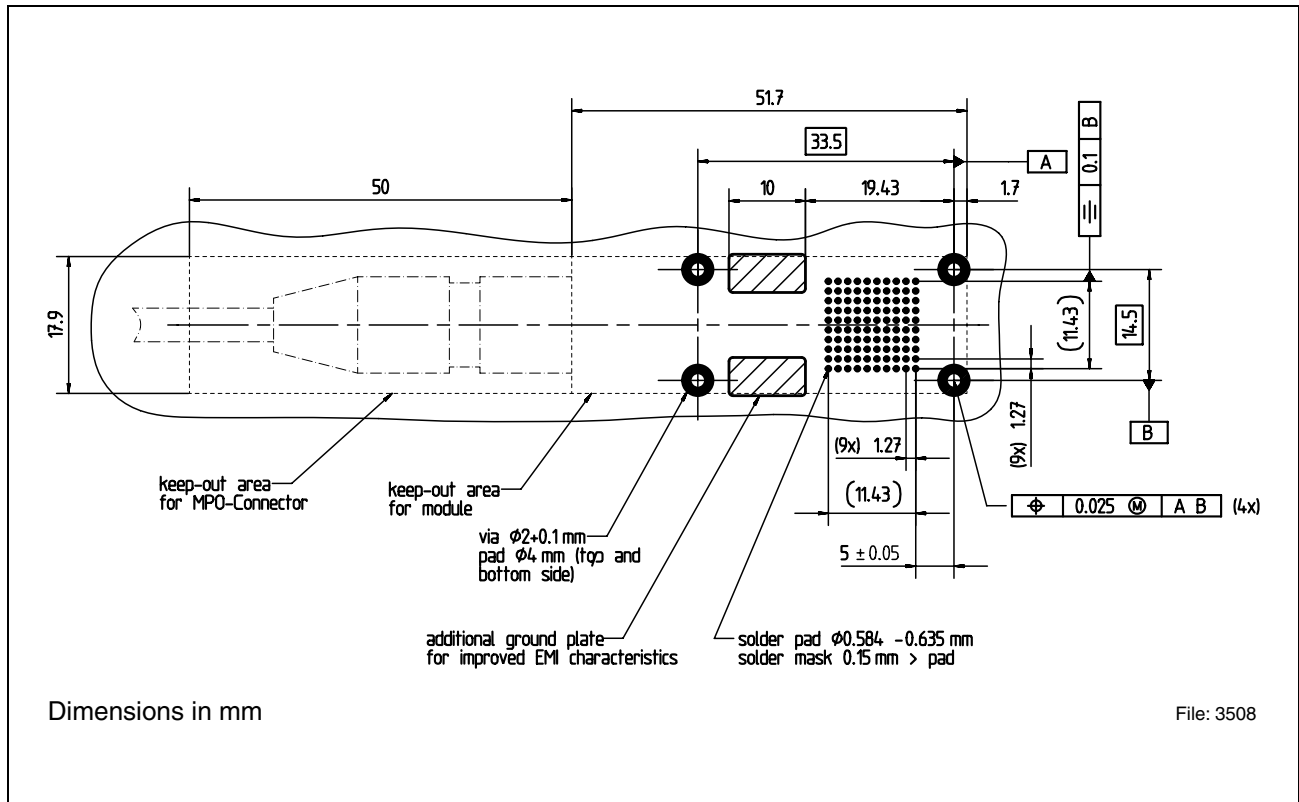


Figure 16

| Key | Values |      |      | Unit | Comments  |
|-----|--------|------|------|------|---|
|     | min.   | typ. | max. |      |   |
| F1  | 18.42  | 20   |      | mm   | Cutout center spacing                                   |
| F2  | 16.7   | 16.8 | 16.9 | mm   | Cutout width  |
| F3  | 9.1    | 9.2  | 9.3  | mm   | Cutout height   |
| F4  | 4.42   | 4.52 | 4.62 | mm   | Center of cutout and center of receptacle to top of PCB |
| F5  | 44.5   |      | 46   | mm   | Face-plate placement                                    |
| F6  |        |      | 1    | mm   | Radius  |
| F7  |        | 4.25 |      | mm   | Opt. reference plane to top of PCB                      |
| F8  |        |      | 38   | mm   | Limitation for PCB length                               |
| F9  |        | 16.8 |      | mm   | Length of receptacle                                    |
| F10 | 15.3   |      |      | mm   | Including shield, without spring contacts               |
| F11 | 7.6    |      |      |      | Including shield, without spring contacts               |
| F12 |        | 1.7  |      | mm   | See Package Outlines <b>Figure 18</b> on <b>Page 31</b> |



**Figure 17 PCB Layout**

1. **Figure 17** describes the recommended customer board layout for the PAROLI 2 modules.
2. The holes for the screwing leads and ground plates must be tied to signal ground.
3. Modules must be screwed on the 4 indicated positions (tightening torque should be typically 10 cNm).
4. Screw size for PCB or heat sink mounting = M1.6.
5. Screw length (PCB mounting) = PCB thickness + 5.2<sub>-0.5</sub> mm.
6. Screw length (heat sink mounting) = heat sink thickness + 3.1<sub>-0.5</sub> mm.
7. Modules can be mounted directly side by side.
8. The dashed lines in **Figure 17** indicate the typical keep out area for straight MPO connectors as well as for the module MPO receptacle in case of central board placement of the module.

## Thermal Characteristics

The thermal behaviour of PAROLI modules (transmitter and receiver) depends on the operating conditions for different applications.

The following table gives a guideline for system designers.

The thermal resistance  $R_{th}$  ( $R_{th} = \frac{T_{case} - T_{ambient}}{P_{el}}$ ;  $P_{el}$  = electrical power consumption)

can be used for calculating the module case temperature under different operating conditions and is displayed for two different module options:

- a) Baseplate module without heat sink.
- b) Baseplate module with customer designed heat sink  
(e.g. height = 9 mm, length = 41 mm, width = 18 mm, no. of cooling fins = 9).

| Air Velocity <sup>1)</sup> | 0 m/s | 1.5 m/s | 3 m/s | 4 m/s | Unit |
|----------------------------|-------|---------|-------|-------|------|
| $R_{th}$ - Option a)       | 23.3  | 10.3    | 8.6   | 7.5   | K/W  |
| $R_{th}$ - Option b)       | 20.0  | 5.2     | 4.2   | 4.0   | K/W  |

<sup>1)</sup> The air velocity is applied along the shortest side of the module in parallel to the direction of the heat sinks.

## Link Length

The link length calculations are based on the most conservative assumption of PAROLI modules working on their worst case specification limits. Multimode fibers of different types (modal bandwidth at 850 nm) are shown. The stated link length is valid under all specified operating conditions and includes 2 dB of additional connector loss.

| Fiber Type Diameter<br>Core/Cladding<br>[μm] | Modal Bandwidth<br>[MHz*km] | Link Distance<br>at 0.5 Gbit/s<br>[m] | Link Distance<br>at 1.25 Gbit/s<br>[m] |
|--|-----------------------------|---------------------------------------|--|
| 62.5 / 125                                   | 200                         | 850                                   | 360                                    |
| 62.5 / 125                                   | 400                         | 1300                                  | 640                                    |

## Channel Description

### Transmitter Module

(front view as looking into the MPO connector receptacle of the module)

|       |       |       |      |      |      |      |      |      |      |      |      |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|
| Ch 12 | Ch 11 | Ch 10 | Ch 9 | Ch 8 | Ch 7 | Ch 6 | Ch 5 | Ch 4 | Ch 3 | Ch 2 | Ch 1 |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|

---

Host PCB below

---

### Receiver Module

(front view as looking into the MPO connector receptacle of the module)

|       |       |       |      |      |      |      |      |      |      |      |      |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|
| Ch 12 | Ch 11 | Ch 10 | Ch 9 | Ch 8 | Ch 7 | Ch 6 | Ch 5 | Ch 4 | Ch 3 | Ch 2 | Ch 1 |
|-------|-------|-------|------|------|------|------|------|------|------|------|------|

---

Host PCB below

---

The MPO connector provides a keying functionality, which requires a 180 degree twist of fiber cable, if used as a direct connection between transmitter and receiver module. (For example the transmitter channel 1 is directly connected to the receiver channel 1).

## Handling Instructions

### Washing Process

The PAROLI mating BGA connector can be handled according to standard industry wave solder, hand solder and washing processes.

The PAROLI modules shall not be washed, due to possible influence on module performance.

### Dust Cover

The optical connector is provided with a dust cover, which protects the optical interface from potential damage and contamination from dust during handling. The dust cover should always remain in the module, when no connector is used.

Package Outlines

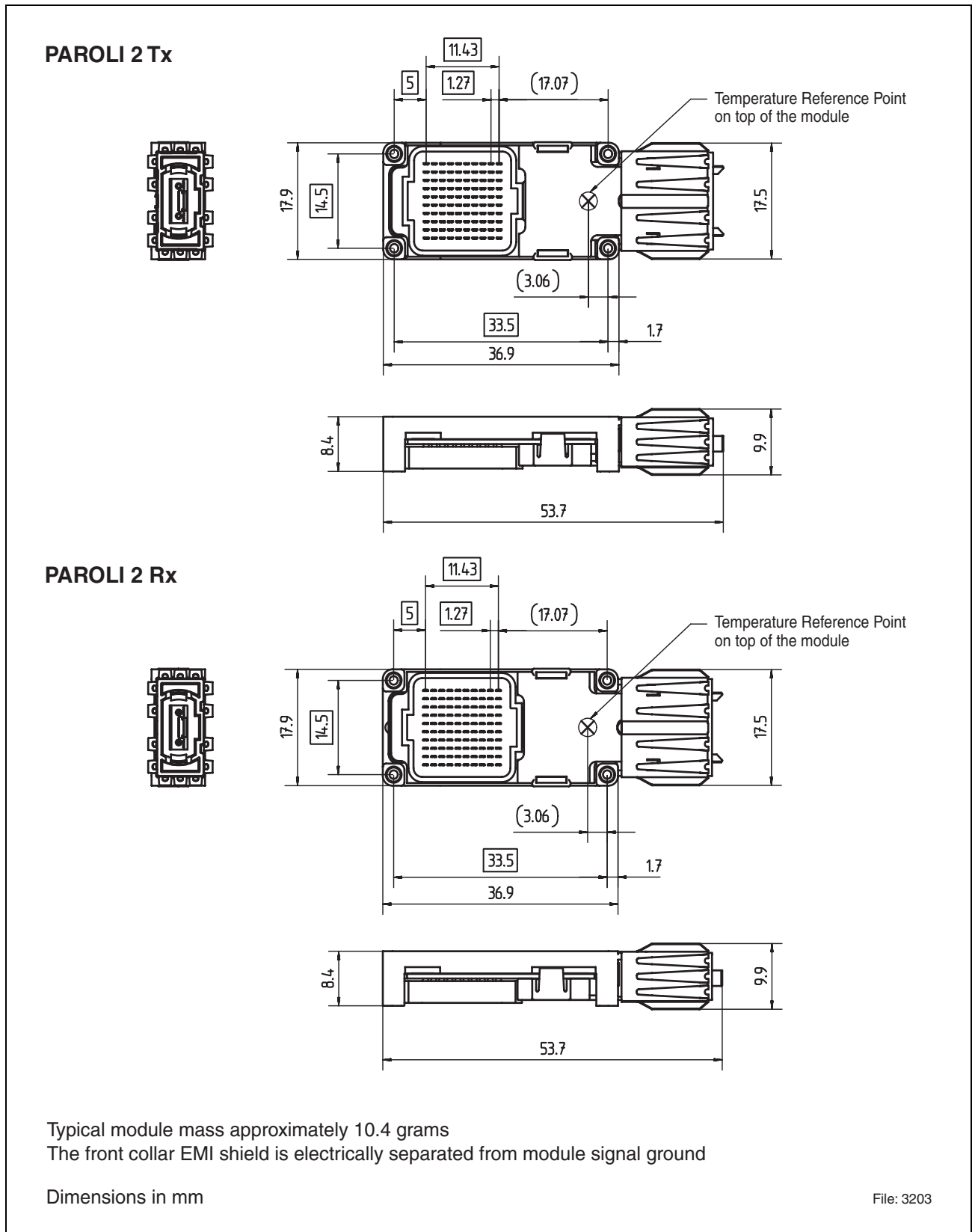


Figure 18

**Ordering Information**

| <b>Part Number</b> | <b>Description</b>  |
|--------------------|---|
| V23832-T2531-M101  | PAROLI Transmitter, 12 x 1.25 Gbit/s, multistandard electrical interface  |
| V23832-T2131-M101  | PAROLI Transmitter, 12 x 1.6 Gbit/s, multistandard electrical interface   |
| V23832-T2431-M101  | PAROLI Transmitter, 12 x 2.7 Gbit/s, multistandard electrical interface   |
| V23832-T2331-M101  | PAROLI Transmitter, 12 x 3.125 Gbit/s, multistandard electrical interface |
| V23832-R521-M101   | PAROLI Receiver, 12 x 1.25 Gbit/s, LVDS electrical interface              |
| V23832-R121-M101   | PAROLI Receiver, 12 x 1.6 Gbit/s, LVDS electrical interface               |
| V23832-R421-M101   | PAROLI Receiver, 12 x 2.7 Gbit/s, LVDS electrical interface               |
| V23832-R321-M101   | PAROLI Receiver, 12 x 3.125 Gbit/s, LVDS electrical interface             |
| V23832-R511-M101   | PAROLI Receiver, 12 x 1.25 Gbit/s, CML electrical interface               |
| V23832-R111-M101   | PAROLI Receiver, 12 x 1.6 Gbit/s, CML electrical interface                |
| V23832-R411-M101   | PAROLI Receiver, 12 x 2.7 Gbit/s, CML electrical interface                |
| V23832-R311-M101   | PAROLI Receiver, 12 x 3.125 Gbit/s, CML electrical interface              |



---

**V23832-T2531-M101**

**V23832-R511-M101**

**Revision History: 2003-11-19**

DS2

---

Previous Version: 2003-05-21

---

| <b>Page</b> | <b>Subjects (major changes since last revision)</b> |
|-------------|---|
|-------------|---|

|  |                             |
|--|-----------------------------|
|  | Document completely revised |
|--|-----------------------------|

---

**Edition 2003-11-19**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
81669 München, Germany**

**© Infineon Technologies AG 2003.  
All Rights Reserved.**

**Attention please!**

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.