

4-BIT SINGLE-CHIP MICROCONTROLLER

FOR INFRARED REMOTE CONTROL TRANSMISSION

The μ PD6P5 is a microcontroller for infrared remote control transmitters which is provided with a one-time PROM as the program memory.

Because users can write programs for the μ PD6P5, it is ideal for program evaluation and small-scale production of the application systems using the μ PD64A or 65.

When reading this document, also refer to the μ PD64A, 65 Data Sheet (U14380E).

FEATURES

- Program memory (one-time PROM) : 2,026 \times 10 bits
- Data memory (RAM) : 32 \times 4 bits
- Built-in carrier generation circuit for infrared remote control
- 9-bit programmable timer : 1 channel
- Command execution time : 16 μ s (when operating at $f_x = 4$ MHz: ceramic oscillation)
- Stack level : 1 level (Stack RAM is for data memory RF as well.)
- I/O pins ($K_{I/O}$) : 8 units
- Input pins (K_i) : 4 units
- Sense input pin (S_0, S_2) : 2 units
- S_1 /LED pin (I/O) : 1 unit (In output mode, this is the remote control transmission display pin.)
- Power supply voltage : $V_{DD} = 2.2$ to 3.6 V
- Operating ambient temperature : $T_A = -40$ to $+85$ °C
- Oscillator frequency : $f_x = 2.4$ to 4.8 MHz
- POC circuit

APPLICATION

Infrared remote control transmitter (for AV and household electric appliances)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

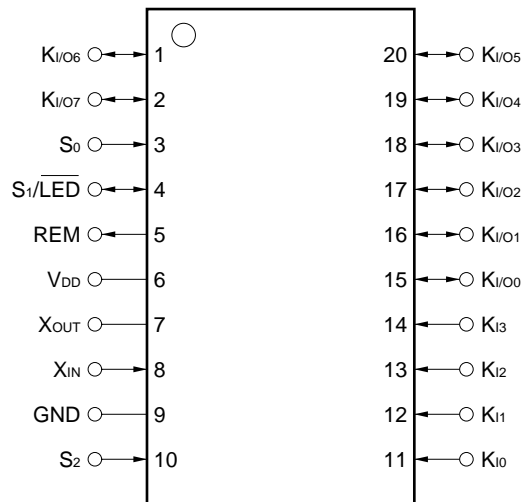
| Part Number | Package |
|--------------|-------------------------------------|
| μPD6P5MC-5A4 | 20-pin plastic SSOP (7.62 mm (300)) |

PIN CONFIGURATION (TOP VIEW)

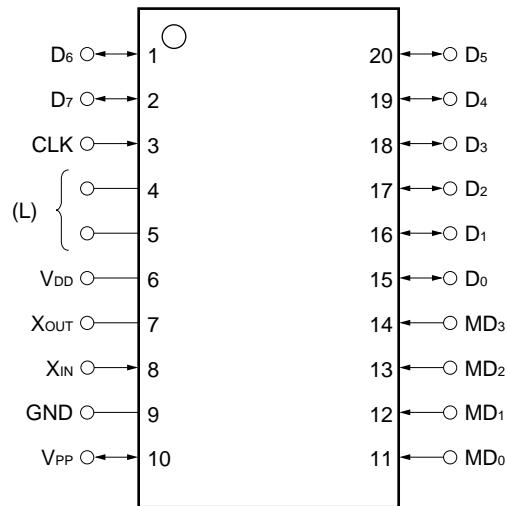
20-pin Plastic SSOP (7.62 mm (300))

- μPD6P5MC-5A4

(1) Normal operation mode

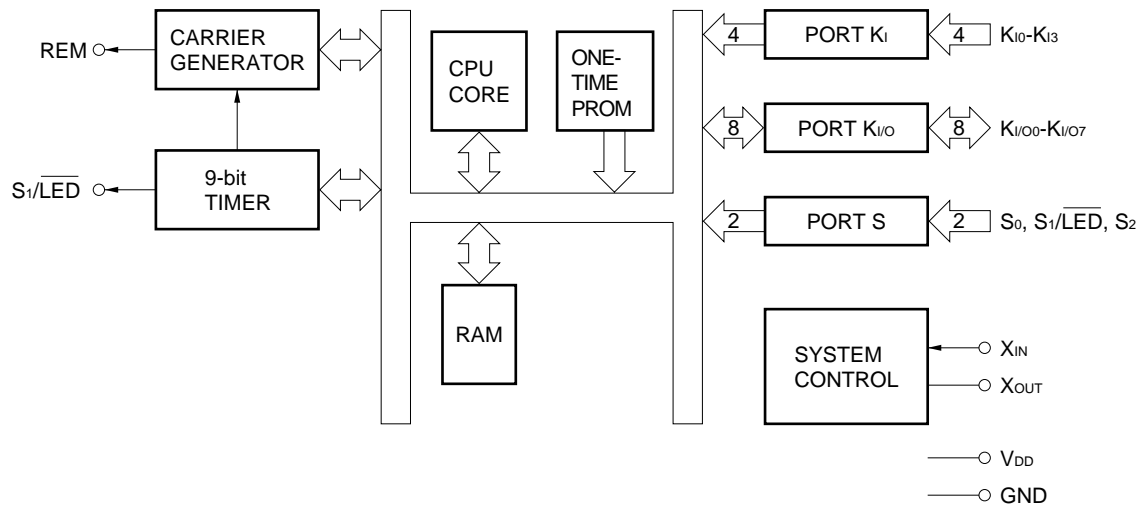


(2) PROM programming mode



Caution Round brackets () indicate the pins not used in the PROM programming mode.
 L: Connect each of these pins to GND via a pull-down resistor.

BLOCK DIAGRAM



LIST OF FUNCTIONS

| Item | μ PD6P5 |
|-------------------------------|--|
| ROM capacity | 2,026 \times 10 bits One-time PROM |
| RAM capacity | 32 \times 4 bits |
| Stack | 1 level (shared with RF of RAM) |
| I/O pin | <ul style="list-style-type: none"> • Key input (K_i) : 4 pins • Key I/O (K_{i/o}) : 8 pins • Key expansion input (S₀, S₁, S₂) : 3 pins • Remote control transmitter display output ($\overline{\text{LED}}$) : 1 pin (shared with S₁ pin) |
| Number of keys | <ul style="list-style-type: none"> • 32 keys • 56 keys (when expanded by key expansion input) |
| Clock frequency | Ceramic oscillation <ul style="list-style-type: none"> • f_x = 2.4 to 4.8 MHz |
| Instruction execution time | 16 μ s (at f _x = 4 MHz) |
| Carrier frequency | f _x /8, f _x /16, f _x /64, f _x /96, f _x /128, f _x /192, no carrier (high level) |
| Timer | 9-bit programmable timer : 1 channel |
| POC circuit | Provided |
| Supply voltage | V _{DD} = 2.2 to 3.6 V |
| Operating ambient temperature | <ul style="list-style-type: none"> • T_A = -40 to +85 °C |
| Package | <ul style="list-style-type: none"> • 20-pin plastic SSOP (7.62 mm (300)) |

TABLE OF CONTENTS

1. PIN FUNCTIONS 6

 1.1 Normal Operation Mode 6

 1.2 PROM Programming Mode 7

 1.3 INPUT/OUTPUT Circuits of Pins 8

 1.4 Dealing with Unused Pins 9

 1.5 Notes on Using K₁ Pin at Reset 9

2. DIFFERENCES AMONG μPD64A, 65, AND μPD6P5 10

 2.1 Program Memory (One-time PROM) 11

3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY) 12

 3.1 Operation Mode When Writing/Verifying Program Memory 12

 3.2 Program Memory Writing Procedure 13

 3.3 Program Memory Reading Procedure 14

4. ELECTRICAL SPECIFICATIONS 15

5. CHARACTERISTIC CURVE (REFERENCE VALUES) 21

6. APPLIED CIRCUIT EXAMPLE 22

7. PACKAGE DRAWINGS 23

8. RECOMMENDED SOLDERING CONDITIONS 24

APPENDIX A. DEVELOPMENT TOOLS 25

APPENDIX B. EXAMPLE OF REMOTE-CONTROL TRANSMISSION FORMAT 26

1. PIN FUNCTIONS

1.1 Normal Operation Mode

| Pin No. | Symbol | Function | Output Format | When Reset |
|-----------------|-----------------------------------|---|----------------------------------|--|
| 1 2 15-20 | $K_{I/O0}-K_{I/O7}$ | These pins refer to the 8-bit I/O ports. I/O switching can be made in 8-bit units. In INPUT mode, a pull-down resistor is added. In OUTPUT mode, they can be used as a key scan output from key matrix. | CMOS push-pull ^{Note 1} | High-level output |
| 3 | S_0 | Refers to the input port. Can also be used as a key return input from key matrix. In INPUT mode, the availability of the pull-down resistor of the S_0 and S_1 ports can be specified by software in terms in 2-bit units. If INPUT mode is canceled by software, this pin is placed in OFF mode and enters the high-impedance state. | — | High-impedance (OFF mode) |
| 4 | S_1/\overline{LED} | Refers to the I/O port. In INPUT mode (S_1), this pin can also be used as a key return input from key matrix. The availability of the pull-down resistor of the S_0 and S_1 ports can be specified by software in 2-bit units. In OUTPUT mode (\overline{LED}), this pin becomes the remote control transmission display output (active low). When the remote control carrier is output from the \overline{REM} output, this pin outputs the low level from the \overline{LED} output synchronously with the REM signal. | CMOS push-pull | High-level output (\overline{LED}) |
| 5 | REM | Refers to the infrared remote control transmission output. The output is active high. Carrier frequency: $f_x/8$, $f_x/64$, $f_x/96$, high-level, $f_x/16$, $f_x/128$, $f_x/192$ (usable on software) | CMOS push-pull | Low-level output |
| 6 | V_{DD} | Refers to the power supply. | — | — |
| 7 8 | X_{OUT} X_{IN} | These pins are connected to system clock ceramic resonators. | — | Low level (oscillation stopped) |
| 9 | GND | Refers to the ground. | — | — |
| 10 | S_2 | Refers to the input port. The use of the STOP mode release of the S_2 port can be specified by software. When using this pin as a key input from a key matrix, enable the use of the STOP mode release (at this time, a pull-down resistor is connected internally.) When the STOP mode release is disabled, this pin can be used as the input port which does not release the STOP mode even if the release condition is established (at this time, a pull-down resistor is not connected internally.) | — | Input (high-impedance, STOP mode release cannot be used) |
| 11-14 | $K_{I0}-K_{I3}$ ^{Note 2} | These pins refer to the 4-bit input ports. They can be used as a key return input from key matrix. The use of the pull-down resistor can be specified by software in 4-bit units. | — | Input (low-level) |

Notes 1. Note that the drive capability of the low-level output side is held low.

2. In order to prevent malfunction, be sure to input a low level to more than one of pins K_{I0} to K_{I3} when POC is released due to supply voltage startup.

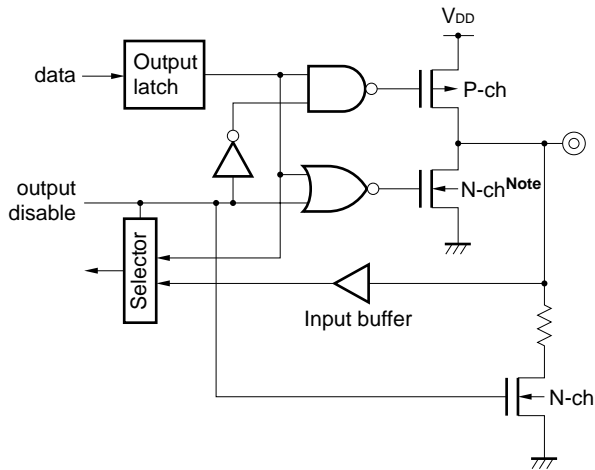
1.2 PROM Programming Mode

| Pin No. | Symbol | Function | I/O |
|---------------|----------------------------------|--|-------|
| 1, 2 15-20 | D ₀ -D ₇ | 8-bit data input/output when writing/verifying program memory | I/O |
| 3 | CLK | Clock input for updating address when writing/verifying program memory | Input |
| 6 | V _{DD} | Power Supply. Supply +6 V to this pin when writing/verifying program memory. | – |
| 7 | X _{OUT} | Clock necessary for writing program memory. Connect 4 MHz ceramic resonator to these pins. | – |
| 8 | X _{IN} | | Input |
| 9 | GND | GND | – |
| 10 | V _{PP} | Supplies voltage for writing/verifying program memory. Apply +12.5 V to this pin. | – |
| 11-14 | MD ₀ -MD ₃ | Input for selecting operation mode when writing/verifying program memory. | Input |

1.3 INPUT/OUTPUT Circuits of Pins

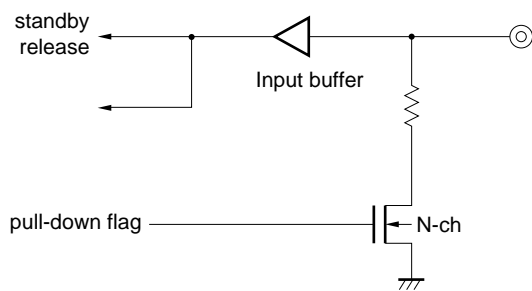
The input/output circuits of the μPD6P5 pins are shown in partially simplified forms below.

(1) K1/00-K1/07

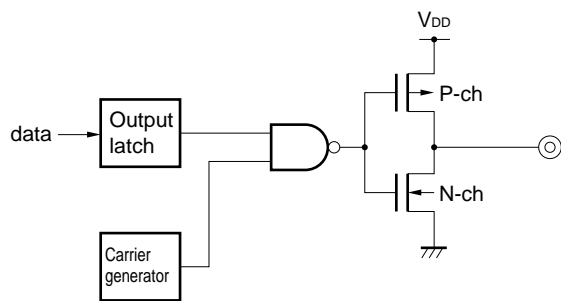


Note The drive capability is held low.

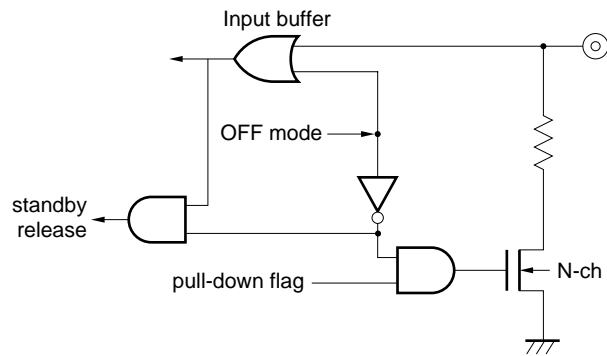
(2) K10-K13



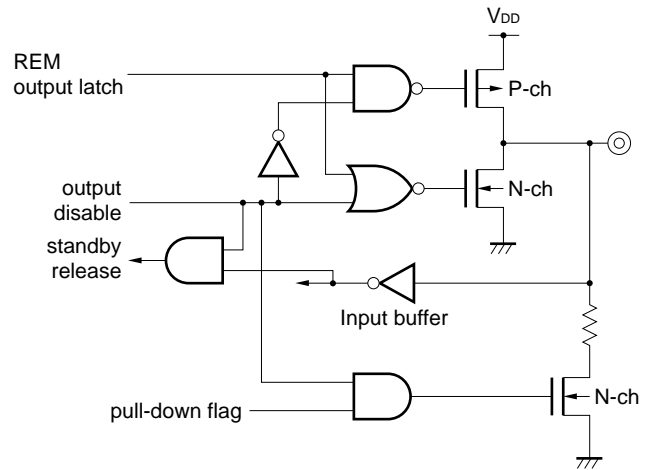
(3) REM



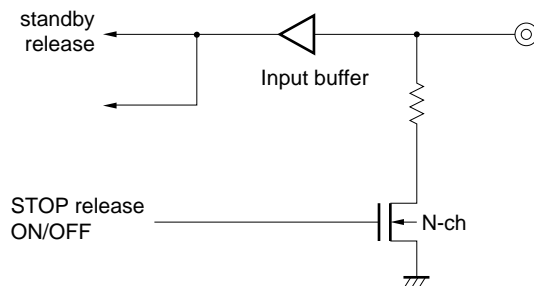
(4) S0



(5) S1/LED



(6) S2



1.4 Dealing with Unused Pins

The following connections are recommended for unused pins in the normal operation mode.

Table 1-1. Connections for Unused Pins

| Pin | | Connection | |
|---------------------|-------------|----------------------------|------------------------------------|
| | | Inside the Microcontroller | Outside the Microcontroller |
| K _{I/O} | INPUT mode | — | Leave open |
| | OUTPUT mode | High-level output | |
| REM | | — | |
| S ₁ /LED | | OUTPUT mode (LED) setting | Directly connect these pins to GND |
| S ₀ | | OFF mode setting | |
| S ₂ | | — | |
| K _I | | — | |

Caution The I/O mode and the terminal output level are recommended to be fixed by setting them repeatedly in each loop of the program.

1.5 Notes on Using K_I Pin at Reset

In order to prevent malfunction, be sure to input a low level to more than one of pins K_{I0} to K_{I3} when POC is released due to supply voltage startup.

2. DIFFERENCES AMONG μPD64A, 65, AND μPD6P5

Table 2-1 shows the differences among the μPD64A, 65, and μPD6P5.

The only differences among these models are the program memory, supply voltage, system clock frequency, and oscillation stabilization wait time, and the CPU function and internal peripheral hardware are the same.

The electrical characteristics also differ slightly. For the electrical characteristics, refer to the Data Sheet of each model.

Table 2-1. Differences among μPD64A, 65, and μPD6P5

| Item | μPD6P5 | μPD64A | μPD65 |
|---|---|--|-----------------|
| ROM | One-time PROM | Mask ROM | |
| | 2,026 × 10 bits | 1,002 × 10 bits | 2,026 × 10 bits |
| Clock frequency | Ceramic oscillation 2.4 to 4.8 MHz | Ceramic oscillation 2.4 to 8 MHz | |
| Oscillation stabilization wait time | | | |
| • On releasing STOP mode by release condition | 286/f _x | 52/f _x | |
| • At reset | 478/f _x to 926/f _x | 246/f _x to 694/f _x | |
| Supply voltage | V _{DD} = 2.2 to 3.6 V | V _{DD} = 2.0 to 3.6 V | |
| Electrical specifications | Some electrical specifications, such as data retention voltage and current consumption, differ. For details, refer to Data Sheet of each model. | | |

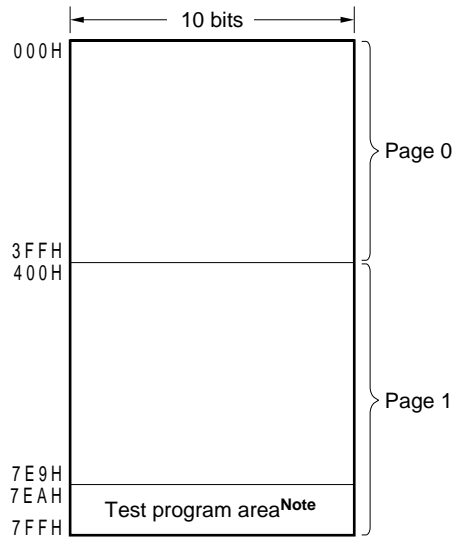
2.1 Program Memory (One-time PROM) ... 2,026 steps × 10 bits

This one-time PROM is configured with 10 bits per step and is addressed by the program counter.

The program memory stores programs and table data.

The 22 steps from addresses 7EAH through 7FFH constitute a test program area and must not be used.

Figure 2-1. Program Memory Map



Note Even if execution jumps to the test program area by mistake, it returns to address 000H.

3. WRITING AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The program memory of the μPD6P5 is a one-time PROM of 2,026 × 10 bits.

To write or verify this program memory, the pins shown in Table 3-1 are used. Note that no address input pin is used. Instead, the address is updated by using the clock input from the CLK pin.

Table 3-1. Pins Used to Write/Verify Program Memory

| Pin Name | Function |
|------------------------------------|--|
| V _{PP} | Supplies voltage when writing/verifying program memory. Apply +12.5 V to this pin. |
| V _{DD} | Power supply. Supply +6 V to this pin when writing/verifying program memory. |
| CLK | Inputs clock to update address when writing/verifying program memory. By inputting pulse four times to CLK pin, address of program memory is updated. |
| MD ₀ -MD ₃ | Input to select operation mode when writing/verifying program memory. |
| D ₀ -D ₇ | Inputs/outputs 8-bit data when writing/verifying program memory. |
| X _{IN} , X _{OUT} | Clock necessary for writing program memory. Connect 4-MHz ceramic resonator to this pin. |

3.1 Operation Mode When Writing/Verifying Program Memory

The μPD6P5 is set in the program memory write/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after the μPD6P5 has been in the reset status (V_{DD} = 5 V, V_{PP} = 0 V) for a specific time. In this mode, the operation modes shown in Table 3-2 can be set by setting the MD₀ through MD₃ pins. Connect all the pins other than those shown in Table 3-1 to GND via pull-down resistor.

Table 3-2. Setting Operation Mode

| Setting of Operation Mode | | | | | | Operation Mode |
|---------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------------------|
| V _{PP} | V _{DD} | MD ₀ | MD ₁ | MD ₂ | MD ₃ | |
| +12.5 V | +6 V | H | L | H | L | Clear program address to 0 |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | × | H | H | Program inhibit mode |

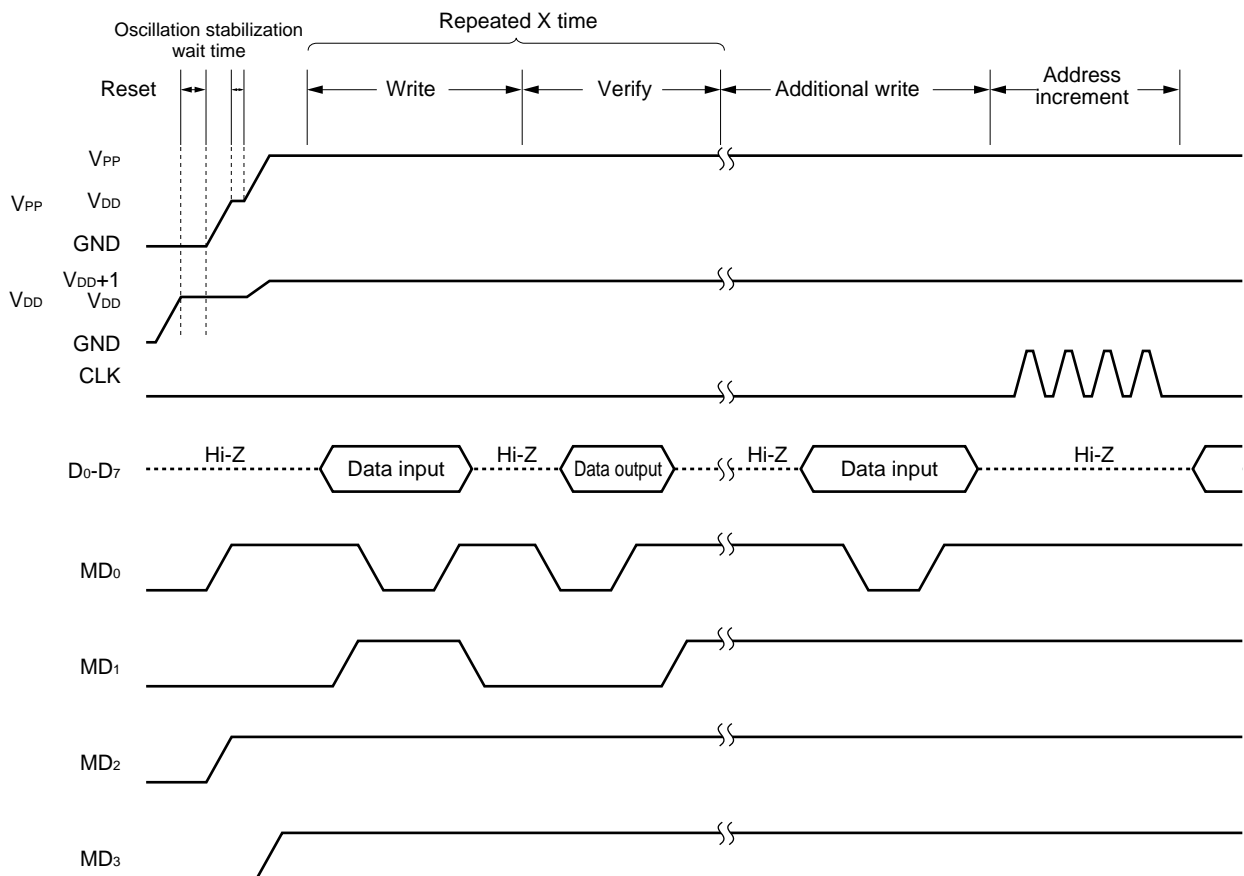
×: don't care (L or H)

3.2 Program Memory Writing Procedure

The program memory is written at high speed in the following procedure.

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
- (4) Wait for 2 ms until oscillation of the ceramic resonator connected across the X_{IN} and X_{OUT} pins stabilizes.
- (5) Set the program memory address 0 clear mode by using the mode setting pins.
- (6) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
- (7) Set the program inhibit mode.
- (8) Write data to the program memory in the 1-ms write mode.
- (9) Set the program inhibit mode.
- (10) Set the verify mode. If the data have been written to the program memory, proceed to (11). If not, repeat steps (8) through (10).
- (11) Additional writing of (number of times of writing in (8) through (10): X) × 1 ms.
- (12) Set the program inhibit mode.
- (13) Input a pulse to the CLK pin four times to update the program memory address (+1).
- (14) Repeat steps (8) through (13) up to the last address.
- (15) Set the 0 clear mode of the program memory address.
- (16) Change the voltages on the V_{DD} and V_{PP} pins to 5 V.
- (17) Turn off power.

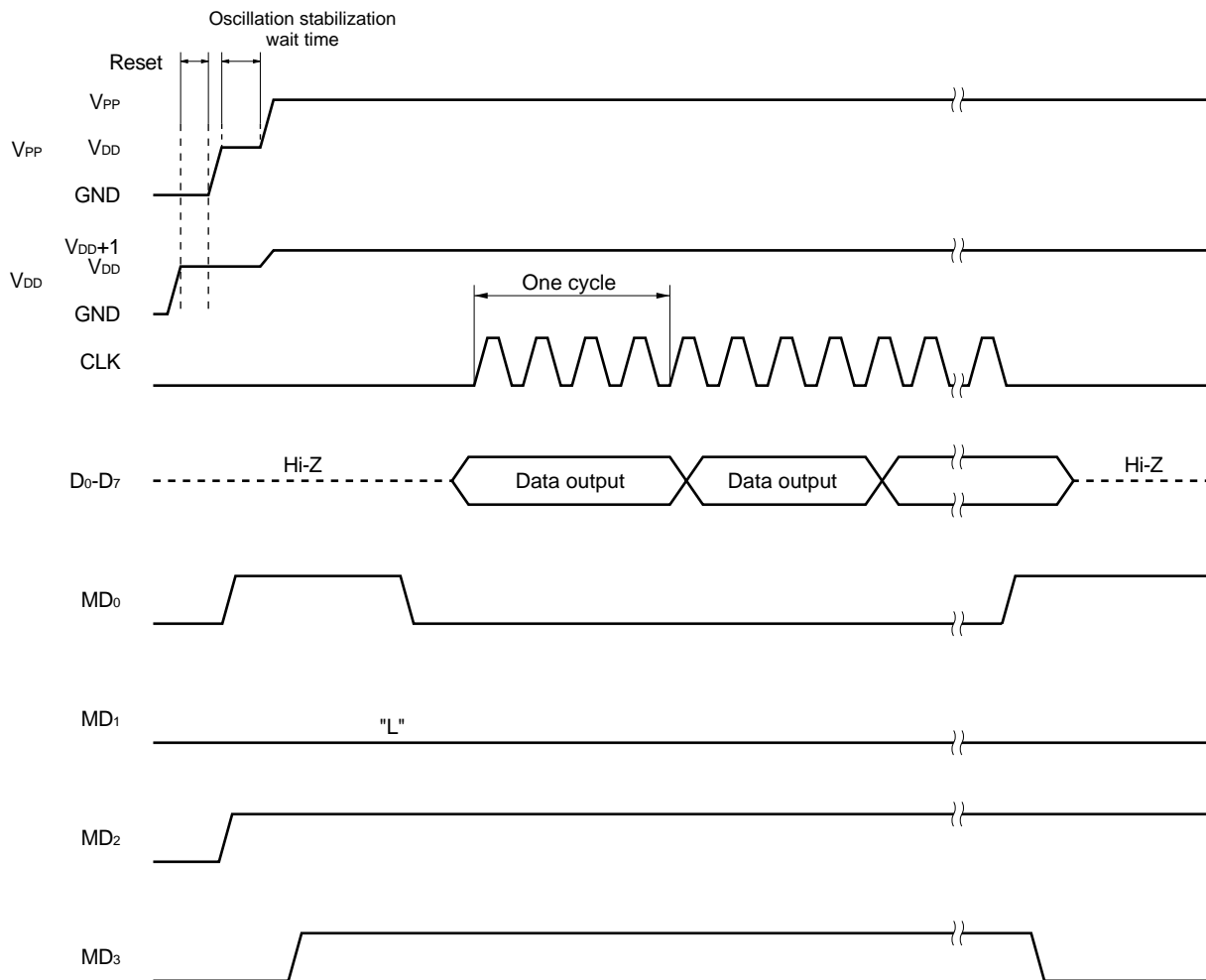
The following figure illustrates steps (2) through (13) above.



3.3 Program Memory Reading Procedure

- (1) Pull down the pins not used to GND via resistor. Keep the CLK pin low.
- (2) Supply 5 V to the V_{DD} pin. Keep the V_{PP} pin low.
- (3) Supply 5 V to the V_{PP} pin after waiting for 10 μs.
- (4) Wait for 2 ms until oscillation of the ceramic resonator connected across the X_{IN} and X_{OUT} pins stabilizes.
- (5) Set the program memory address 0 clear mode by using the mode setting pins.
- (6) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
- (7) Set the program inhibit mode.
- (8) Set the verify mode. Data of each address is output sequentially each time the clock pulse is input to the CLK pin four times.
- (9) Set the program inhibit mode.
- (10) Set the program memory address 0 clear mode.
- (11) Change the voltage on the V_{DD} and V_{PP} pins to 5 V.
- (12) Turn off power.

The following figure illustrates steps (2) through (10) above.



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

| Parameter | Symbol | Conditions | | Rating | Unit |
|-------------------------------|---------------------------------|--|------------|-------------------------------|------|
| Power supply voltage | V _{DD} | | | -0.3 to +7.0 | V |
| | V _{PP} | | | -0.3 to +13.5 | V |
| Input voltage | V _I | K _{I/O} , K _I , S ₀ , S ₁ , S ₂ | | -0.3 to V _{DD} + 0.3 | V |
| Output voltage | V _O | | | -0.3 to V _{DD} + 0.3 | V |
| High-level output current | I _{OH} ^{Note} | REM | Peak value | -30 | mA |
| | | | rms | -20 | mA |
| | | $\overline{\text{LED}}$ | Peak value | -7.5 | mA |
| | | | rms | -5 | mA |
| | | One K _{I/O} pin | Peak value | -13.5 | mA |
| | | | rms | -9 | mA |
| | | Total of $\overline{\text{LED}}$ and K _{I/O} pins | Peak value | -18 | mA |
| | | | rms | -12 | mA |
| Low-level output current | I _{OL} ^{Note} | REM | Peak value | 7.5 | mA |
| | | | rms | 5 | mA |
| | | $\overline{\text{LED}}$ | Peak value | 7.5 | mA |
| | | | rms | 5 | mA |
| Operating ambient temperature | T _A | | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | | -65 to +150 | °C |

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Power Supply Voltage Range (T_A = -40 to +85 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|-----------------|---------------------------------|------|------|------|------|
| Power supply voltage | V _{DD} | f _x = 2.4 to 4.8 MHz | 2.2 | 3.0 | 3.6 | V |

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|----------------------------------|-------------------|--|---|----------------------|------|----------------------|------|
| High-level input voltage | V _{IH1} | S ₂ | | 0.8 V _{DD} | | V _{DD} | V |
| | V _{IH2} | K _{I/O} | | 0.65 V _{DD} | | V _{DD} | V |
| | V _{IH3} | K _I , S ₀ , S ₁ | | 0.65 V _{DD} | | V _{DD} | V |
| Low-level input voltage | V _{IL1} | S ₂ | | 0 | | 0.2 V _{DD} | V |
| | V _{IL2} | K _{I/O} | | 0 | | 0.3 V _{DD} | V |
| | V _{IL3} | K _I , S ₀ , S ₁ | | 0 | | 0.15 V _{DD} | V |
| High-level input leakage current | I _{LIH1} | K _I V _I = V _{DD} , pull-down resistor not incorporated | | | | 3 | μA |
| | I _{LIH2} | S ₀ , S ₁ , S ₂ V _I = V _{DD} , pull-down resistor not incorporated | | | | 3 | μA |
| Low-level input leakage current | I _{LIL1} | K _I | V _I = 0 V | | | -3 | μA |
| | I _{LIL2} | K _{I/O} | V _I = 0 V | | | -3 | μA |
| | I _{LIL3} | S ₀ , S ₁ , S ₂ | V _I = 0 V | | | -3 | μA |
| High-level output voltage | V _{OH1} | REM, $\overline{\text{LED}}$, K _{I/O} | I _{OH} = -0.3 mA | 0.8 V _{DD} | | | V |
| Low-level output voltage | V _{OL1} | REM, $\overline{\text{LED}}$ | I _{OL} = 0.3 mA | | | 0.3 | V |
| | V _{OL2} | K _{I/O} | I _{OL} = 15 μA | | | 0.4 | V |
| High-level output current | I _{OH1} | REM | V _{DD} = 3.0 V, V _{OH} = 1.0 V | -5 | -9 | | mA |
| | I _{OH2} | K _{I/O} | V _{DD} = 3.0 V, V _{OH} = 2.2 V | -2.5 | -5 | | mA |
| Low-level output current | I _{OL1} | K _{I/O} | V _{DD} = 3.0 V, V _{OL} = 0.4 V | 30 | 70 | | μA |
| | | | V _{DD} = 3.0 V, V _{OL} = 2.2 V | 100 | 220 | | μA |
| Built-in pull-down resistor | R ₁ | K _I , S ₀ , S ₁ , S ₂ | | 75 | 150 | 300 | kΩ |
| | R ₂ | K _{I/O} | | 130 | 250 | 500 | kΩ |
| Data hold power supply voltage | V _{DDDR} | In STOP mode | | 1.2 | | 3.6 | V |
| Supply current ^{Note} | I _{DD1} | Operating mode | f _x = 4 MHz, V _{DD} = 3 V ±10 % | | 1.1 | 2.2 | mA |
| | I _{DD2} | HALT mode | f _x = 4 MHz, V _{DD} = 3 V ±10 % | | 1.0 | 2.0 | mA |
| | I _{DD3} | STOP mode | V _{DD} = 3 V ±10 % | | 2.2 | 9.5 | μA |
| | | | V _{DD} = 3 V ±10 %, T _A = 25°C | | 2.2 | 3.5 | μA |

AC Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|-----------------|-----------------------------|-------------|------|------|------|
| Instruction execution time | t _{cy} | | 13.3 | | 27 | μs |
| K1, S0, S1, S2 high-level width | t _H | | 10 | | | μs |
| | | When canceling standby mode | HALT mode | 10 | | |
| | | STOP mode | Note | | | μs |

Note 10 + 286/f_x + oscillation growth time

Remark t_{cy} = 64/f_x (f_x: System clock oscillator frequency)

POC Circuit (T_A = -40 to +85 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------------|------------------|------------|------|------|------|------|
| POC-detected voltage ^{Note} | V _{POC} | | | 2.0 | 2.2 | V |

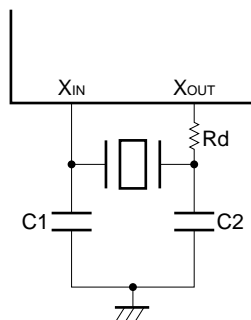
Note Refers to the voltage with which the POC circuit cancels an internal reset. If V_{POC} < V_{DD}, the internal reset is canceled.

From the time of V_{POC} ≥ V_{DD} until the internal reset takes effect, lag of up to 1 ms occurs. When the period of V_{POC} ≥ V_{DD} lasts less than 1 ms, the internal reset may not take effect.

System Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.2 to 3.6 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|----------------|------------|------|------|------|------|
| Oscillator frequency (ceramic resonator) | f _x | | 2.4 | 3.64 | 4.8 | MHz |

An external circuit example



Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

PROM Programming Mode

DC Programming Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------|-----------|-----------------------------------|----------------|------|--------------|---------------|
| High-level input voltage | V_{IH1} | Other than CLK | $0.7 V_{DD}$ | | V_{DD} | V |
| | V_{IH2} | CLK | $V_{DD} - 0.5$ | | V_{DD} | V |
| Low-level input voltage | V_{IL1} | Other than CLK | 0 | | $0.3 V_{DD}$ | V |
| | V_{IL2} | CLK | 0 | | 0.4 | V |
| Input leakage current | I_{LI} | $V_{IN} = V_{IL}$ or V_{IH} | | | 10 | μA |
| High-level output voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | $V_{DD} - 1.0$ | | | V |
| Low-level output voltage | V_{OL} | $I_{OL} = 1.6 \text{ mA}$ | | | 0.4 | V |
| V_{DD} supply current | I_{DD} | | | | 30 | mA |
| V_{PP} supply current | I_{PP} | $MD_0 = V_{IL}$, $MD_1 = V_{IH}$ | | | 30 | mA |

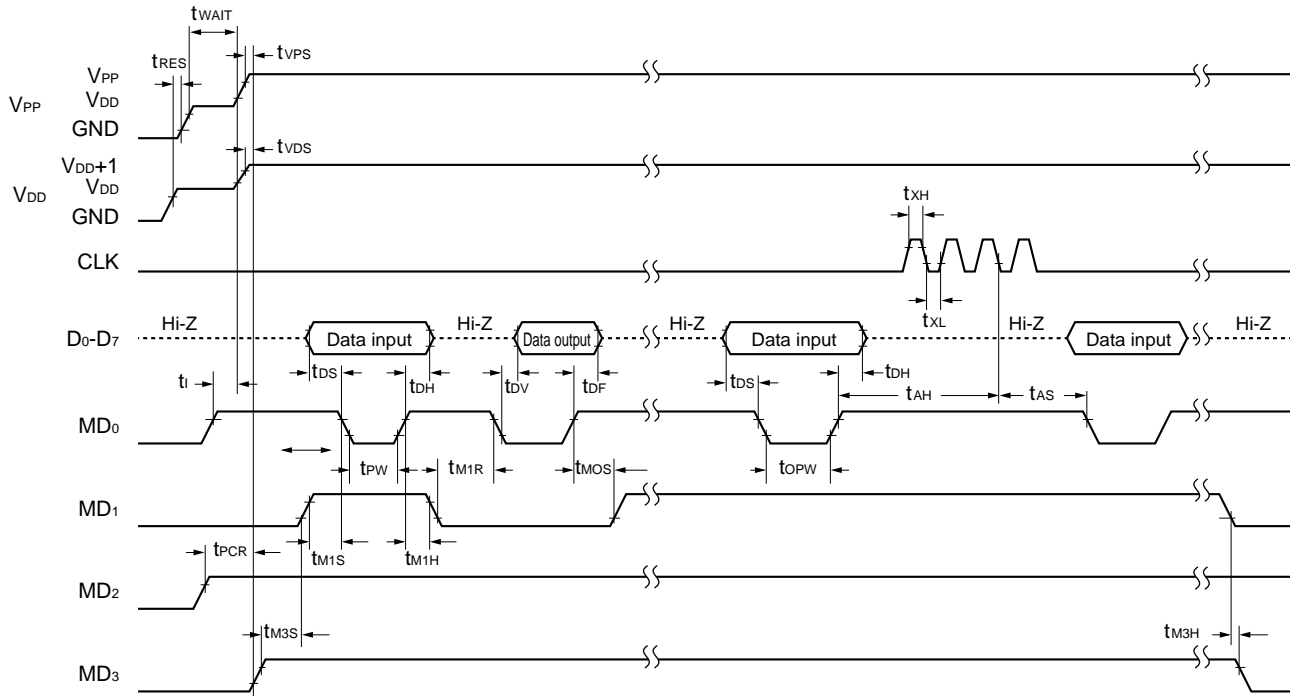
- Cautions**
1. Keep V_{PP} to within +13.5 V including overshoot.
 2. Apply V_{DD} before V_{PP} and turn it off after V_{PP} .

AC Programming Characteristics ($T_A = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

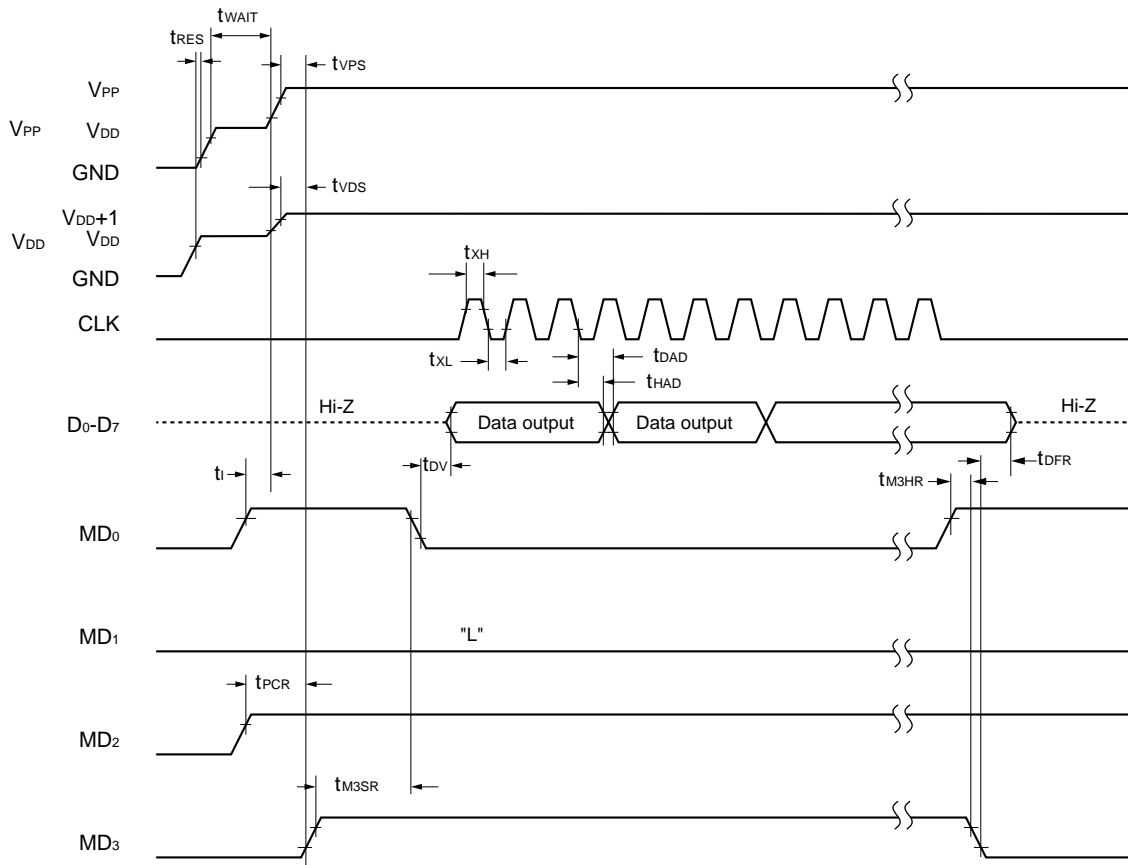
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-----------------------------------|--|-------|------|------|---------------|
| Address setup time ^{Note 1} (vs. MD ₀ ↓) | t _{AS} | | 2 | | | μs |
| MD ₁ setup time (vs. MD ₀ ↓) | t _{M1S} | | 2 | | | μs |
| Data setup time (vs. MD ₀ ↓) | t _{DS} | | 2 | | | μs |
| Address hold time ^{Note 1} (vs. MD ₀ ↑) | t _{AH} | | 2 | | | μs |
| Data hold time (vs. MD ₀ ↑) | t _{DH} | | 2 | | | μs |
| MD ₀ ↑ → data output float delay time | t _{DF} | | 0 | | 130 | ns |
| V _{PP} setup time (vs. MD ₃ ↑) | t _{VPS} | | 2 | | | μs |
| V _{DD} setup time (vs. MD ₃ ↑) | t _{VDS} | | 2 | | | μs |
| Initial program pulse width | t _{PW} | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | t _{OPW} | | 0.95 | | 21.0 | ms |
| MD ₀ setup time (vs. MD ₁ ↑) | t _{MOS} | | 2 | | | μs |
| MD ₀ ↓ → data output delay time | t _{DV} | MD ₀ = MD ₁ = V _{IL} | | | 1 | μs |
| MD ₁ hold time (vs. MD ₀ ↑) | t _{M1H} | t _{M1H} + t _{M1R} ≥ 50 μs | 2 | | | μs |
| MD ₁ recovery time (vs. MD ₀ ↓) | t _{M1R} | | 2 | | | μs |
| Program counter reset time | t _{PCR} | | 10 | | | μs |
| CLK input high-, low-level width | t _{XH} , t _{XL} | | 0.125 | | | μs |
| CLK input frequency | f _X | | | | 4.19 | MHz |
| Initial mode set time | t _i | | 2 | | | μs |
| MD ₃ setup time (vs. MD ₁ ↑) | t _{M3S} | | 2 | | | μs |
| MD ₃ hold time (vs. MD ₁ ↓) | t _{M3H} | | 2 | | | μs |
| MD ₃ setup time (vs. MD ₀ ↓) | t _{M3SR} | When program memory is read | 2 | | | μs |
| Address ^{Note 1} → data output delay time | t _{DAD} | When program memory is read | | | 2 | μs |
| Address ^{Note 1} → data output hold time | t _{HAD} | When program memory is read | 0 | | 130 | ns |
| MD ₃ hold time (vs. MD ₀ ↑) | t _{M3HR} | When program memory is read | 2 | | | μs |
| MD ₃ ↓ → data output float delay time | t _{DFR} | When program memory is read | | | 2 | μs |
| Reset setup time | t _{RES} | | 10 | | | μs |
| Oscillation stabilization wait time ^{Note 2} | t _{WAIT} | | 2 | | | ms |

- Notes**
1. The internal address signal is incremented at the falling edge of the third clock of CLK.
 2. Connect a 4 MHz ceramic resonator between the X_{IN} and X_{OUT} pins.

Program Memory Write Timing

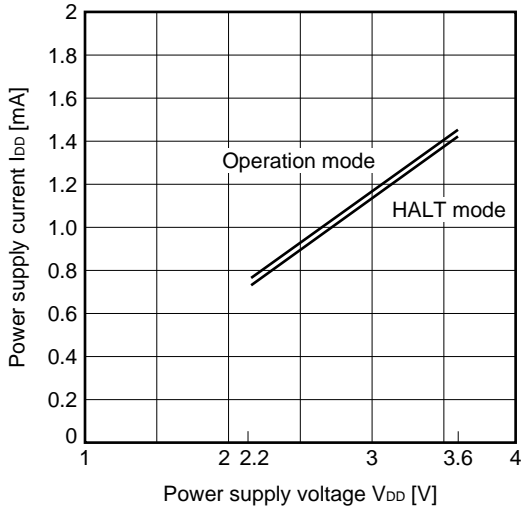


Program Memory Read Timing

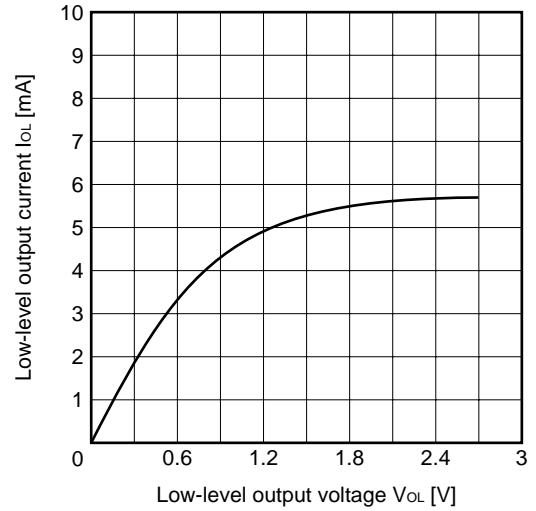


5. CHARACTERISTIC CURVE (REFERENCE VALUES)

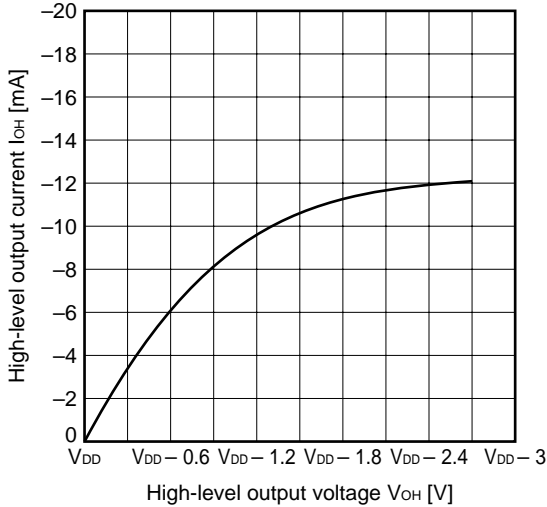
I_{DD} vs V_{DD} (fx = 4 MHz)
(T_A = 25°C)



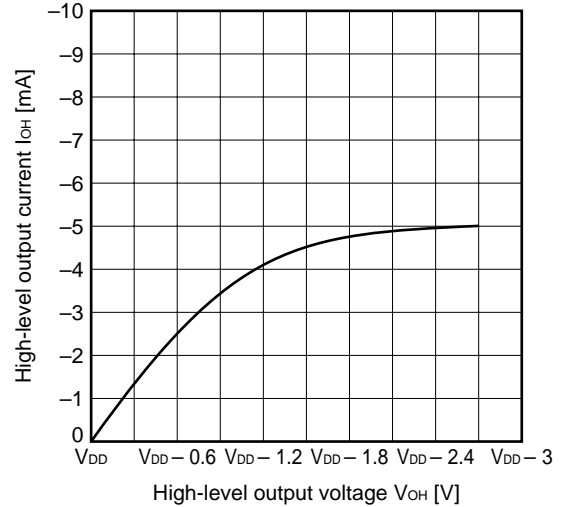
I_{OL} vs V_{OL} (REM, LED)
(T_A = 25°C, V_{DD} = 3.0 V)



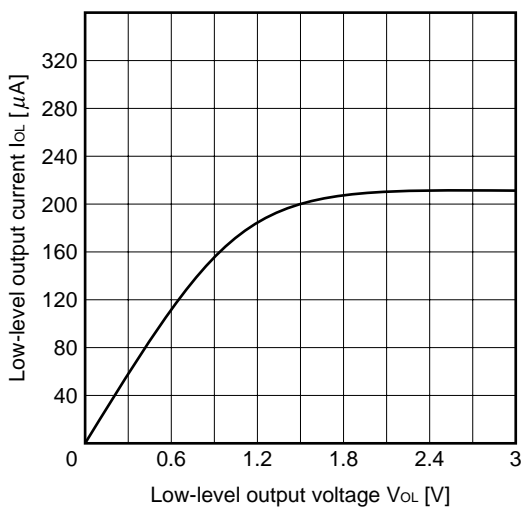
I_{OH} vs V_{OH} (REM)
(T_A = 25°C, V_{DD} = 3.0 V)



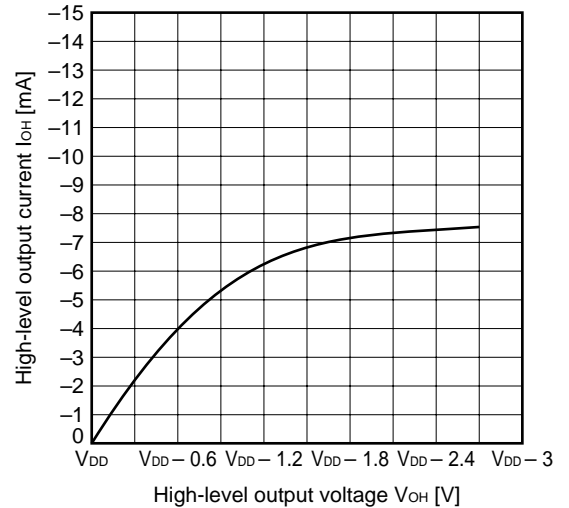
I_{OH} vs V_{OH} (LED)
(T_A = 25°C, V_{DD} = 3.0 V)



I_{OL} vs V_{OL} (K_{I/O})
(T_A = 25°C, V_{DD} = 3.0 V)



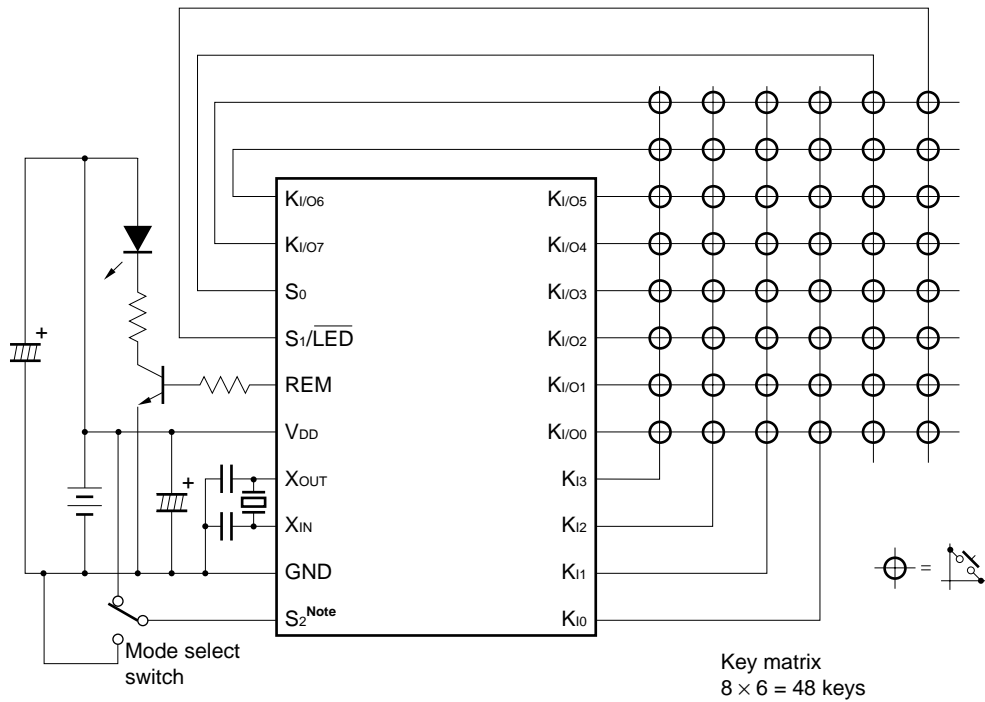
I_{OH} vs V_{OH} (K_{I/O})
(T_A = 25°C, V_{DD} = 3.0 V)



6. APPLIED CIRCUIT EXAMPLE

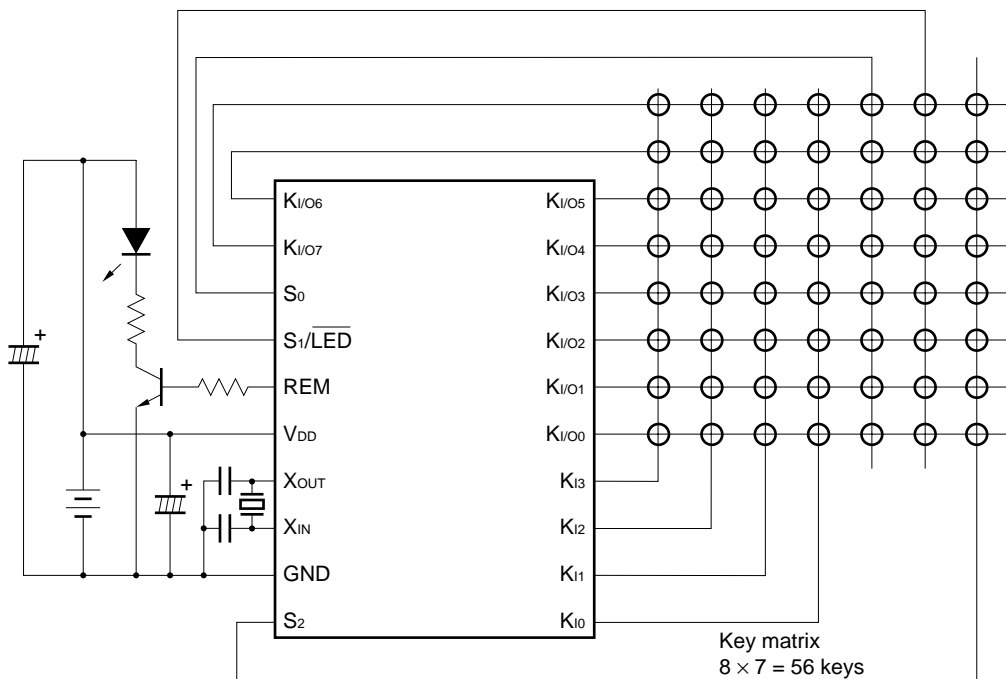
Example of Application to System

- Remote-control transmitter (48 keys; mode selection switch accommodated)



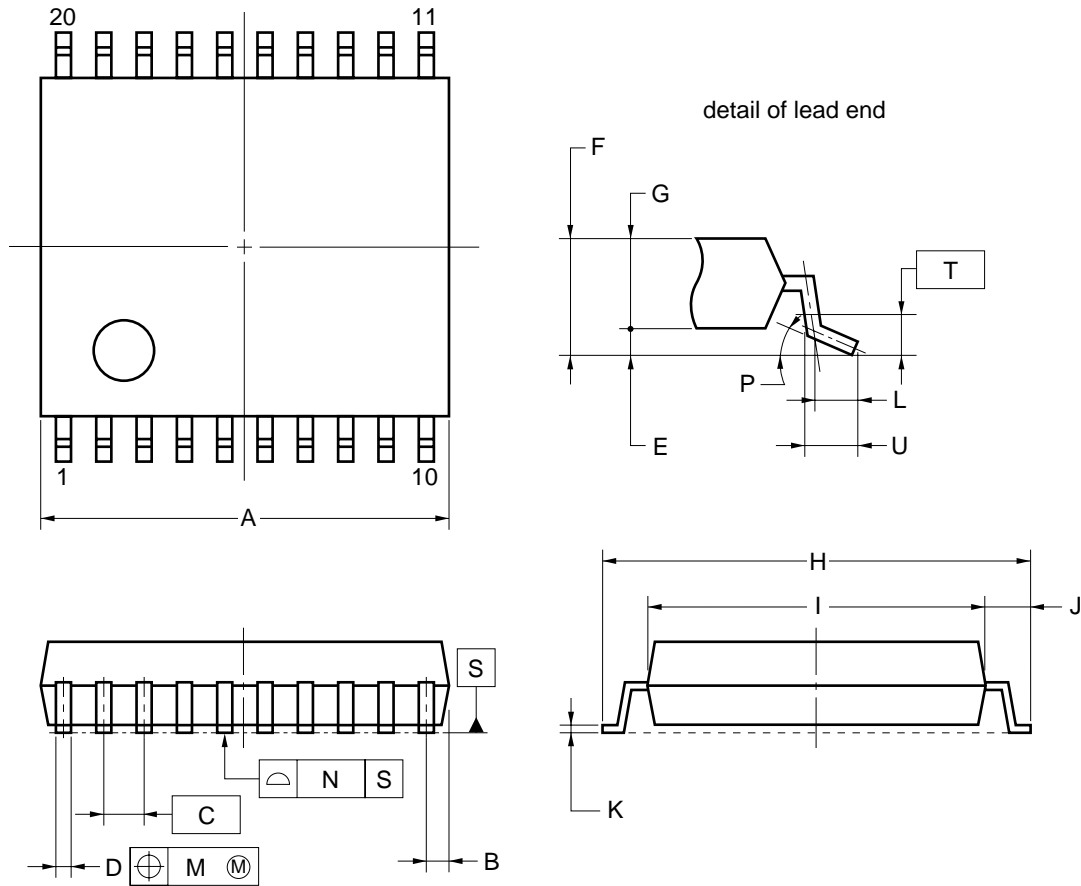
Note S₂: Set this pin to disable when releasing STOP mode.

- Remote-control transmitter (56 keys accommodated)



7. PACKAGE DRAWINGS

20-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 6.65±0.15 |
| B | 0.475 MAX. |
| C | 0.65 (T.P.) |
| D | 0.24 ^{+0.08} _{-0.07} |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | 3° ^{+5°} _{-3°} |
| T | 0.25 |
| U | 0.6±0.15 |

S20MC-65-5A4-2

8. RECOMMENDED SOLDERING CONDITIONS

Carry out the soldered packaging of this product under the following recommended conditions.

For details of the soldering conditions, refer to information material **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than the recommended conditions, please consult one of our NEC sales representatives.

Table 8-1. Soldering Conditions for Surface-Mount Type

μPD6P5MC-5A4: 20-pin plastic SSOP (7.62 mm (300))

| Soldering Method | Soldering Condition | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow | Package peak temperature: 235 °C, Time: 30 sec. Max. (at 210 °C or higher), Count: three times or less | IR35-00-3 |
| VPS | Package peak temperature: 215 °C, Time: 40 sec. Max. (at 200 °C or higher), Count: three times or less | VP15-00-3 |
| Wave soldering | Solder bath temperature: 260 °C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120 °C Max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300 °C Max., Time: 3 sec. Max. (per pin row) | — |

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

A PROM programmer, program adapter, and emulator are provided for the μPD6P5.

Hardware

- **PROM programmer (AF-9706^{Note}, AF-9708^{Note}, AF-9709^{Note})**

This PROM programmer supports the μPD6P5.

By connecting a program adapter to this PROM programmer, the μPD6P5 can be programmed.

Note These are products of Ando Electric Co., Ltd. For details, consult Ando Electric Co., Ltd. (03-3733-1166).

- **Program adapter (PA-61P34BMC)**

It is used to program the μPD6P5 in combination with AF-9706, AF-9708, or AF-9709.

- **Emulator (EB-65^{Note})**

It is used to emulate the μPD6P5.

Note This is a product of Naito Densai Machida Mfg. Co., Ltd. For details, consult Naito Densai Machida Mfg. Co., Ltd. (044-822-3813).

Software

- **Assembler (AS6133)**

- This is a development tool for remote control transmitter software.

Part Number List of AS6133

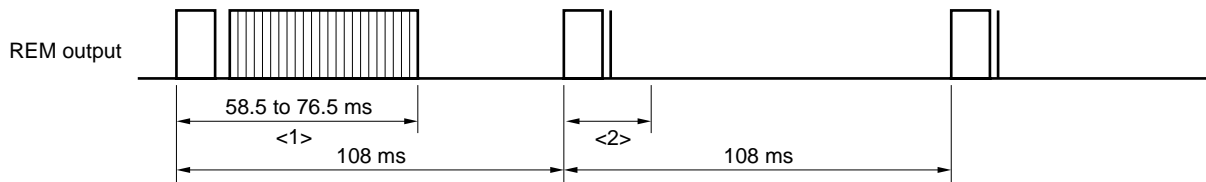
| Host Machine | OS | Supply Medium | Part Number |
|--|--------------------------------|---------------|--------------|
| PC-9800 series (CPU: 80386 or more) | MS-DOS™ (Ver. 5.0 to Ver. 6.2) | 3.5-inch 2HD | μS5A13AS6133 |
| IBM PC/AT™ compatible | MS-DOS (Ver. 6.0 to Ver. 6.22) | 3.5-inch 2HC | μS7B13AS6133 |
| | PC DOS™ (Ver. 6.1 to Ver. 6.3) | | |

Caution Although Ver.5.0 or later has a task swap function, this function cannot be used with this software.

APPENDIX B. EXAMPLE OF REMOTE-CONTROL TRANSMISSION FORMAT
 (in the case of NEC transmission format in command one-shot transmission mode)

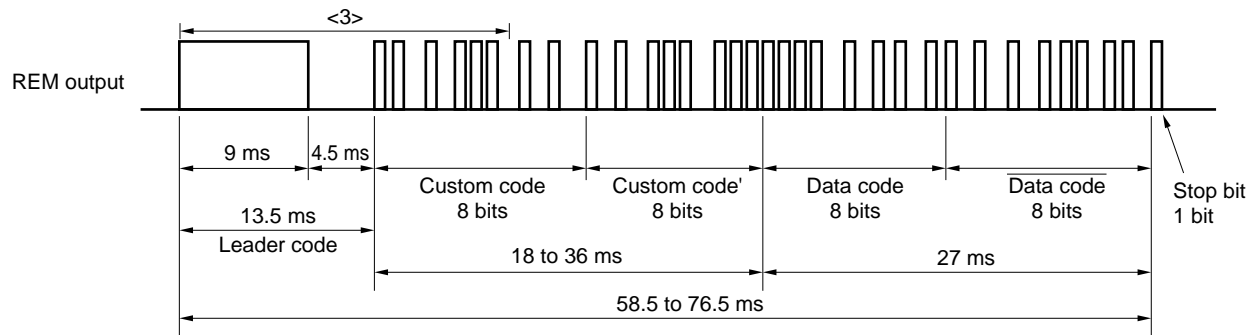
Caution When using the NEC transmission format, please apply for a custom code at NEC.

(1) REM output waveform (From <2> on, the output is made only when the key is kept pressed.)

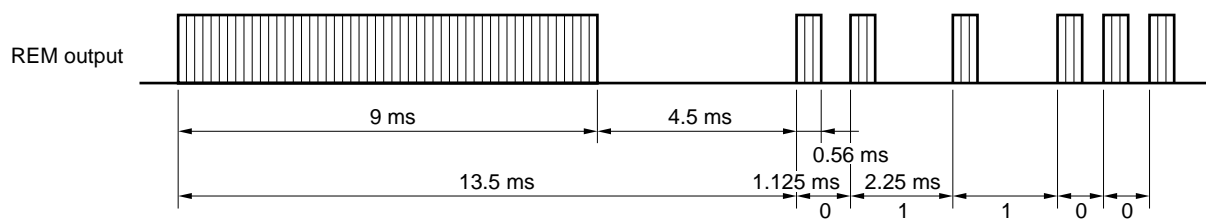


Remark If the key is repeatedly pressed, the power consumption of the infrared light-emitting diode (LED) can be reduced by sending the reader code and the stop bit from the second time.

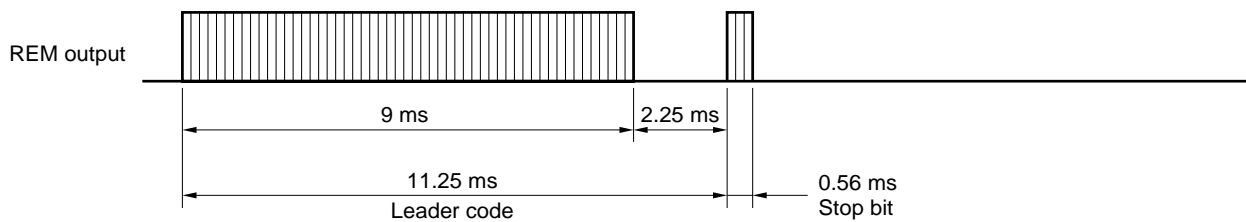
(2) Enlarged waveform of <1>



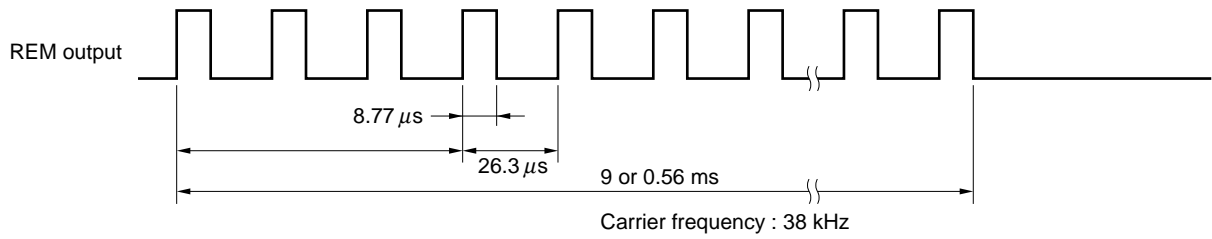
(3) Enlarged waveform of <3>



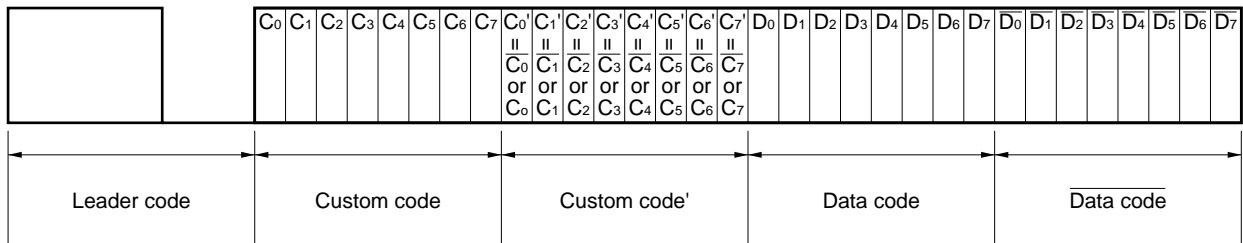
(4) Enlarged waveform of <2>



(5) Carrier waveform (Enlarged waveform of each code's high period)



(6) Bit array of each code



Caution To prevent malfunction with other systems when receiving data in the NEC transmission format, not only fully decode (make sure to check Data code as well) the total 32 bits of the 16-bit custom codes (Custom code, Custom code') and the 16-bit data codes (Data code, Data code) but also check to make sure that no signals are present.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 65-250-3583

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Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

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