

FEATURES

- **SMALL PACKAGE OUTLINE:**
SOT-363 package measures just 2.0 mm x 1.25 mm
- **LOW HEIGHT PROFILE:**
Just 0.60 mm high
- **HIGH COLLECTOR CURRENT:**
Ic MAX = 100 mA

DESCRIPTION

The UPA814TF contains two NE688 NPN high frequency silicon bipolar chips. NEC's new low profile TF package is ideal for all portable wireless applications where reducing component height is a prime consideration. Each transistor chip is independently mounted and easily configured for two stage cascade LNAs and other similar applications.

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{CB0}	Collector to Base Voltage	V	9
V _{CE0}	Collector to Emitter Voltage	V	6
V _{EB0}	Emitter to Base Voltage	V	2
I _c	Collector Current	mA	100
P _T	Total Power Dissipation		
	1 Die	mW	110
	2 Die	mW	200
T _J	Junction Temperature	°C	150
T _{STG}	Storage Temperature	°C	-65 to +150

Note: 1. Operation in excess of any one of these parameters may result in permanent damage.

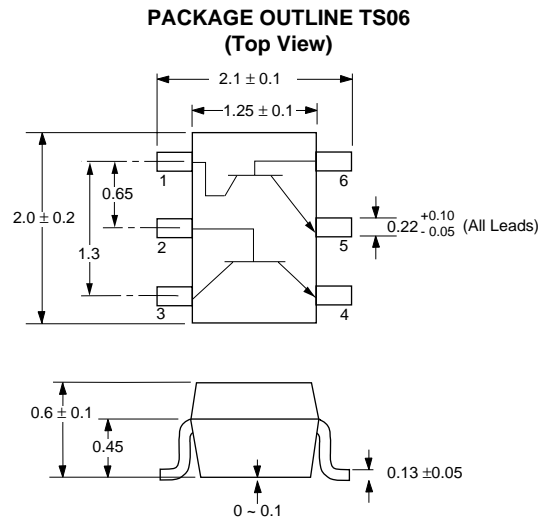
ELECTRICAL CHARACTERISTICS (TA = 25°C)

PART NUMBER PACKAGE OUTLINE			UPA814TF TS06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I _{CB0}	Collector Cutoff Current at V _{CB} = 5V, I _E = 0	μA			0.1
I _{EB0}	Emitter Cutoff Current at V _{EB} = 1V, I _C = 0	μA			0.1
h _{FE}	Forward Current Gain ¹ at V _{CE} = 1V, I _C = 3 mA		80	110	160
f _T	Gain Bandwidth at V _{CE} = 3V, I _C = 20 mA, f = 2 GHz	GHz		9.0	
C _{re}	Feedback Capacitance ² at V _{CB} = 1V, I _E = 0, f = 1 MHz	pF		0.75	0.85
S _{21E} ²	Insertion Power Gain at V _{CE} = 3V, I _C = 20 mA, f = 2 GHz	dB		6.5	
NF	Noise Figure at V _{CE} = 3V, I _C = 7 mA, f = 2 GHz	dB		1.5	
h _{FE1} /h _{FE2}	h _{FE} Ratio: h _{FE1} = Smaller Value of Q ₁ , or Q ₂ h _{FE2} = Larger Value of Q ₁ or Q ₂		0.85		

Notes: 1. Pulsed measurement, pulse width ≤ 350 μs, duty cycle ≤ 2 %.

2. The emitter terminal should be connected to the ground terminal of the 3 terminal capacitance bridge. For Tape and Reel version use part number UPA814TF-T1, 3K per reel.

OUTLINE DIMENSIONS (Units in mm)



PIN OUT

1. Collector Transistor 1
2. Base Transistor 2
3. Collector Transistor 2
4. Emitter Transistor 2
5. Emitter Transistor 1
6. Base Transistor 1

Note:

Pin 1 is the lower left most pin as the package lettering is oriented and read left to right.