

## SWITCHING N- AND P-CHANNEL POWER MOS FET

### DESCRIPTION

The μPA2790GR is N- and P-channel MOS Field Effect Transistors designed for Motor Drive application.

### FEATURES

- Low on-state resistance

N-channel  $R_{DS(on)1} = 28 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 3 \text{ A}$ )

$R_{DS(on)2} = 40 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 3 \text{ A}$ )

P-channel  $R_{DS(on)1} = 60 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -3 \text{ A}$ )

$R_{DS(on)2} = 80 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -3 \text{ A}$ )

- Low input capacitance

N-channel  $C_{iss} = 500 \text{ pF TYP.}$

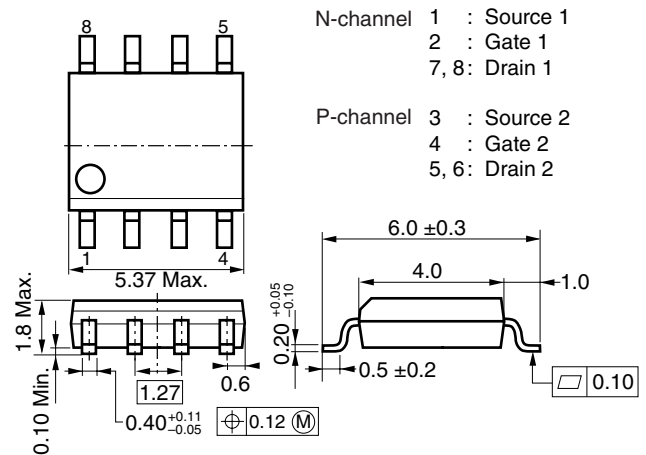
P-channel  $C_{iss} = 460 \text{ pF TYP.}$

- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

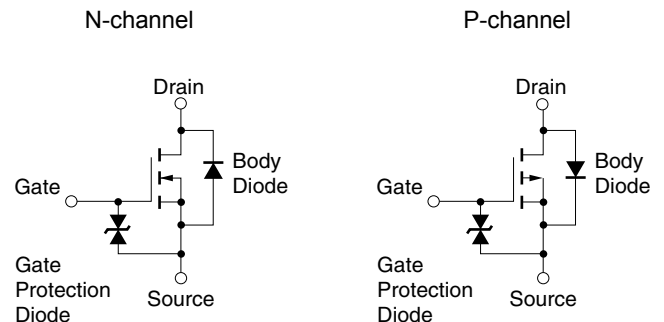
### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2790GR	Power SOP8

### PACKAGE DRAWING (Unit: mm)



### EQUIVALENT CIRCUITS



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C. All terminals are connected.)**

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	-30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	∓20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±6	∓6	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±24	∓24	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	1.7		W
Total Power Dissipation (2 units) <sup>Note2</sup>	P <sub>T</sub>	2.0		W
Channel Temperature	T <sub>ch</sub>	150		°C
Storage Temperature	T <sub>stg</sub>	-55 to +150		°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	6	-6	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	3.6	3.6	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

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2. Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 1.6 mm

3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> =  $\frac{1}{2}$  x V<sub>DSS</sub>, R<sub>G</sub> = 25 Ω, L = 100 μH, V<sub>GS</sub> = V<sub>GSS</sub> → 0 V

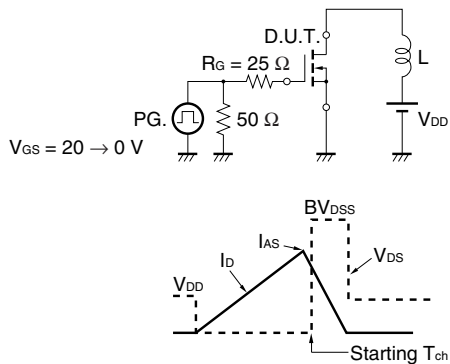
**ELECTRICAL CHARACTERISTICS (TA = 25°C. All terminals are connected.)**

**N-channel**

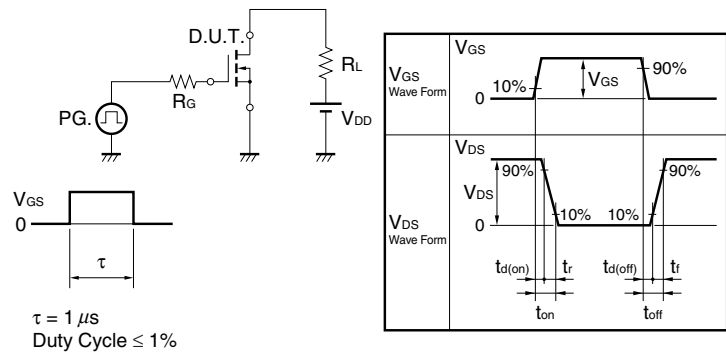
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.5		2.5	V
Forward Transfer Admittance <sup>Note</sup>	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 3\text{ A}$	2			S
Drain to Source On-state Resistance <sup>Note</sup>	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		21	28	mΩ
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 3\text{ A}$		28	40	mΩ
	$R_{DS(on)3}$	$V_{GS} = 4.0\text{ V}, I_D = 3\text{ A}$		34	53	mΩ
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}$		500		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$		135		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		77		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, I_D = 3\text{ A}$		9.2		ns
Rise Time	$t_r$	$V_{GS} = 10\text{ V}$		8.8		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		28		ns
Fall Time	$t_f$			7.4		ns
Total Gate Charge	$Q_G$	$I_D = 6\text{ A}$		12.6		nC
Gate to Source Charge	$Q_{GS}$	$V_{DD} = 24\text{ V}$		1.7		nC
Gate to Drain Charge	$Q_{GD}$	$V_{GS} = 10\text{ V}$		3.8		nC
Body Diode Forward Voltage <sup>Note</sup>	$V_{F(S-D)}$	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		0.85		V
Reverse Recovery Time	$t_{rr}$	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		18		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100\text{ A}/\mu\text{s}$		11		nC

**Note** Pulsed

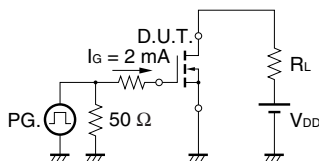
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**



**TEST CIRCUIT 3 GATE CHARGE**

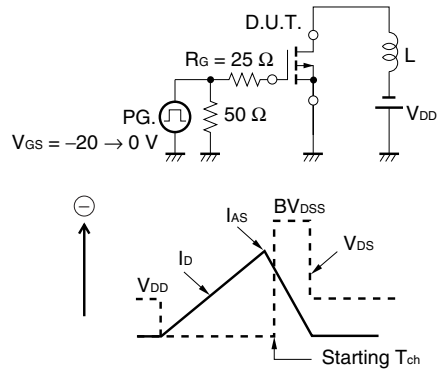


**P-channel**

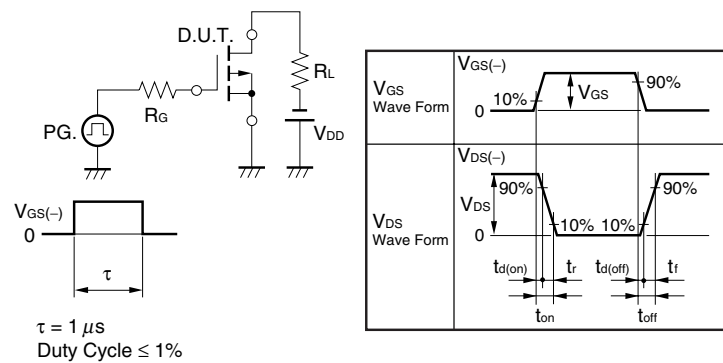
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-10	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$			$\mp 10$	$\mu\text{A}$
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance <sup>Note</sup>	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -3\text{ A}$	2			S
Drain to Source On-state Resistance <sup>Note</sup>	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -3\text{ A}$		43	60	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -3\text{ A}$		58	80	$\text{m}\Omega$
	$R_{DS(on)3}$	$V_{GS} = -4.0\text{ V}, I_D = -3\text{ A}$		65	110	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}$		460		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$		130		pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		77		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, I_D = -3\text{ A}$		8.5		ns
Rise Time	$t_r$	$V_{GS} = -10\text{ V}$		4.8		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		42		ns
Fall Time	$t_f$			19		ns
Total Gate Charge	$Q_G$	$I_D = -6\text{ A}$		11		nC
Gate to Source Charge	$Q_{GS}$	$V_{DD} = -24\text{ V}$		1.7		nC
Gate to Drain Charge	$Q_{GD}$	$V_{GS} = -10\text{ V}$		3.3		nC
Body Diode Forward Voltage <sup>Note</sup>	$V_{F(S-D)}$	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		0.92		V
Reverse Recovery Time	$t_{rr}$	$I_F = 6\text{ A}, V_{GS} = 0\text{ V}$		21		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100\text{ A}/\mu\text{s}$		12		nC

**Note** Pulsed

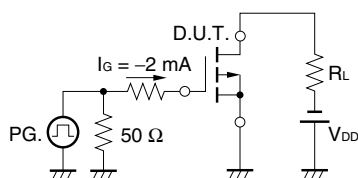
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

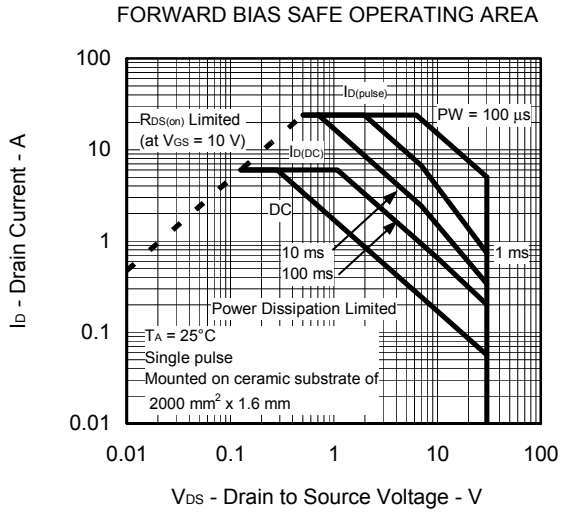
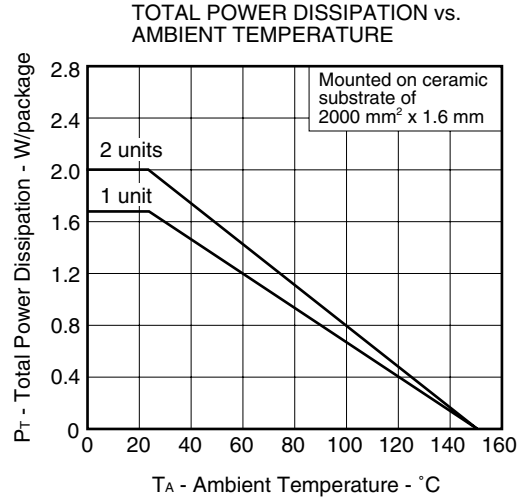
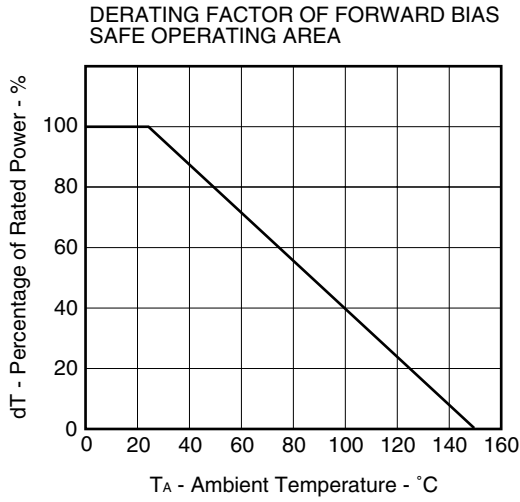


**TEST CIRCUIT 3 GATE CHARGE**

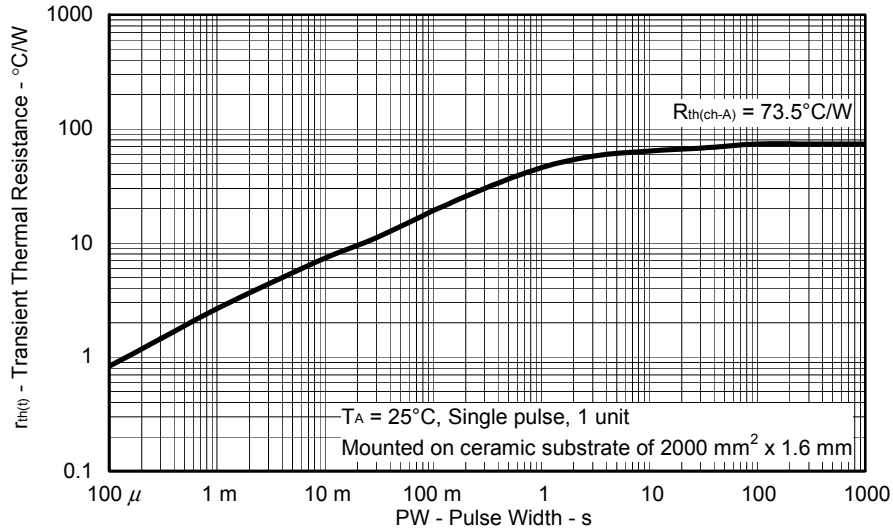


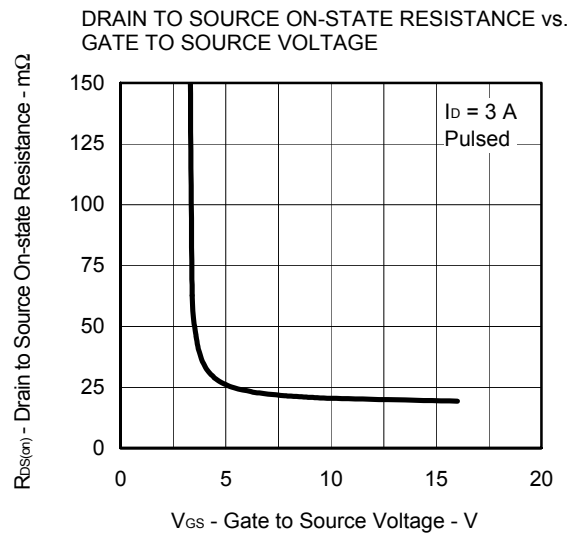
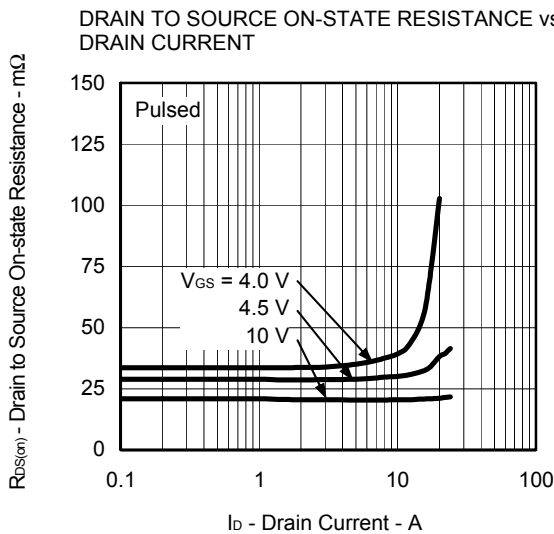
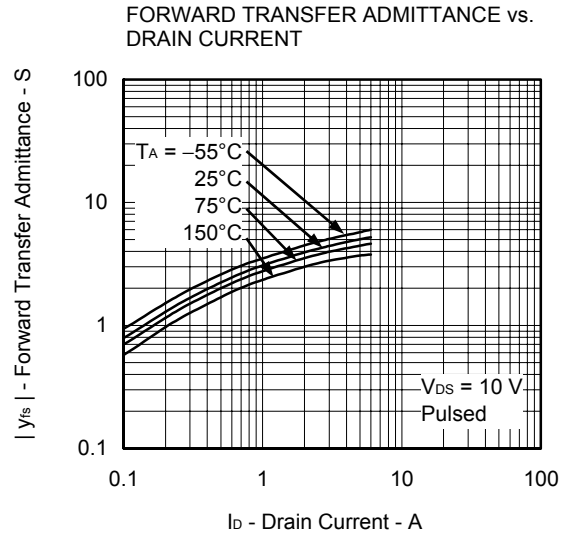
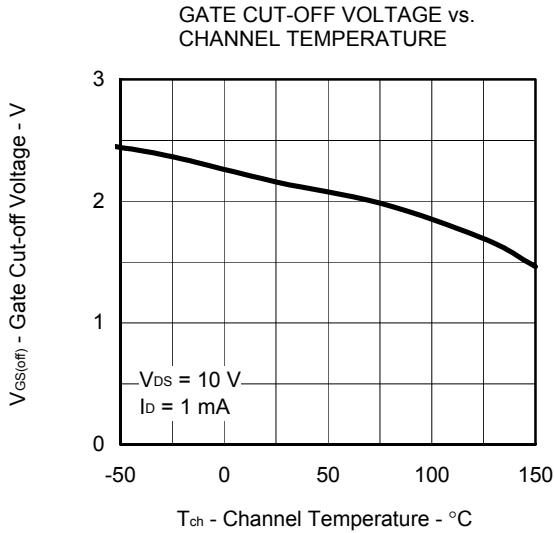
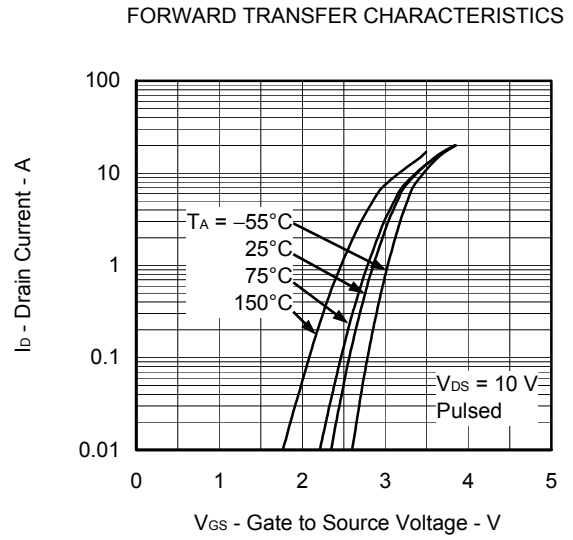
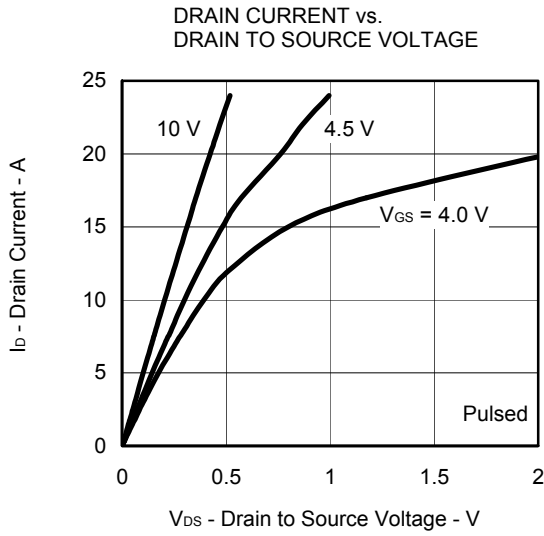
★ TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

(1) N-channel

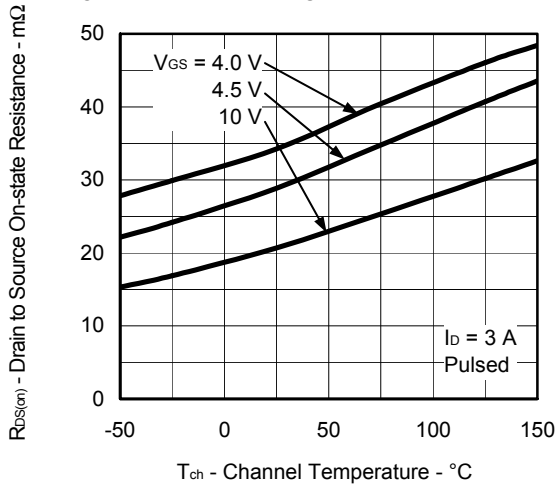


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

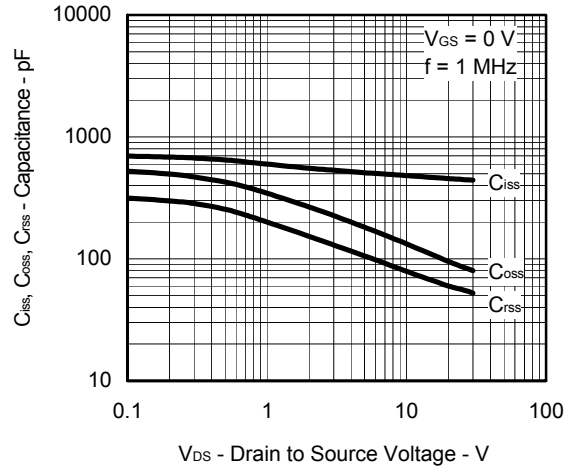




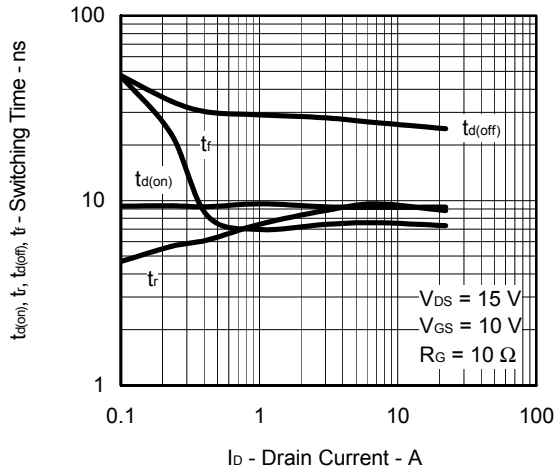
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



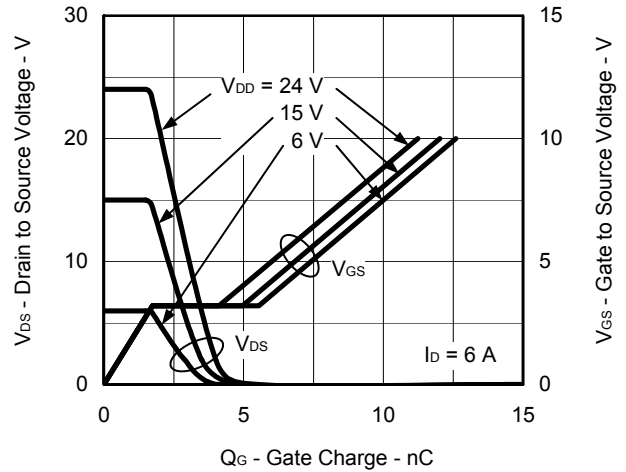
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



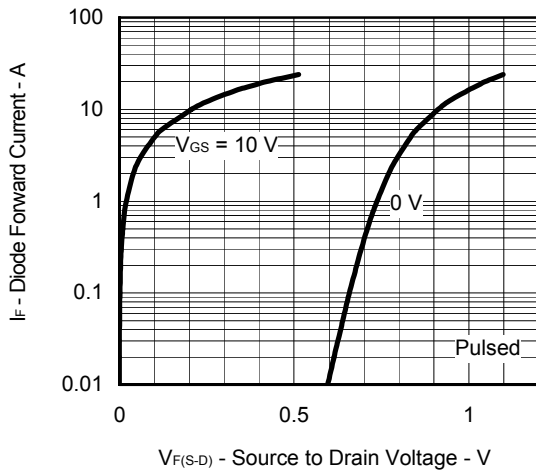
SWITCHING CHARACTERISTICS



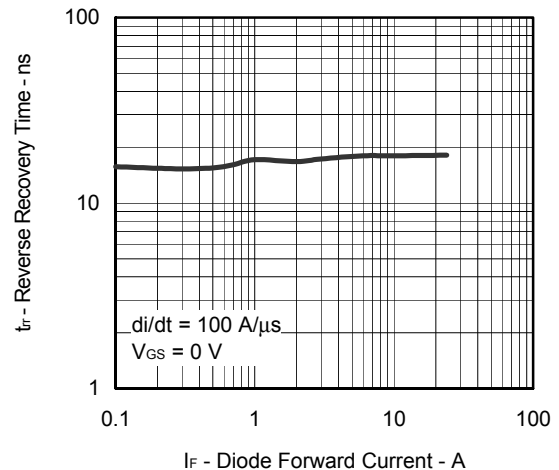
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

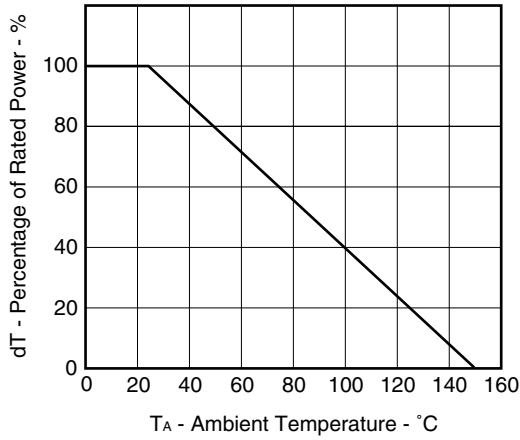


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

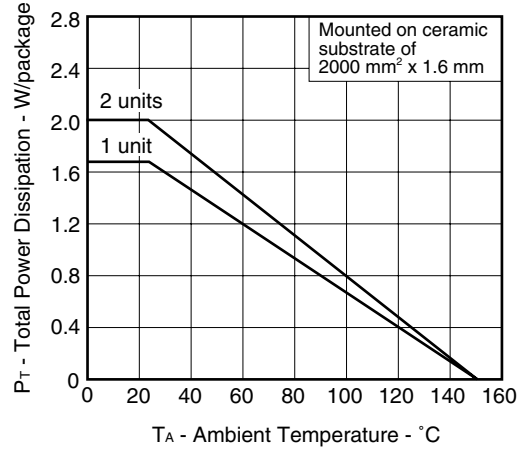


(2) P-channel

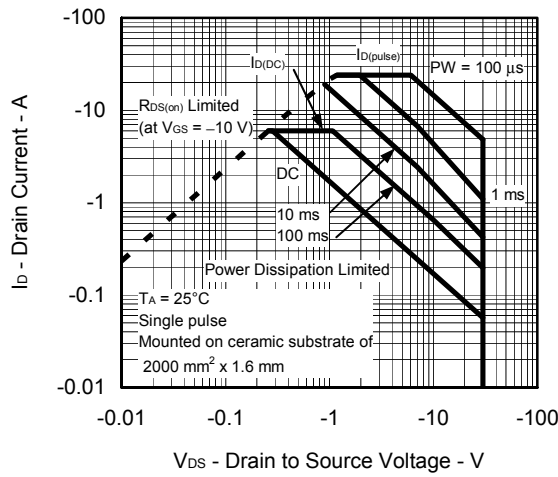
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



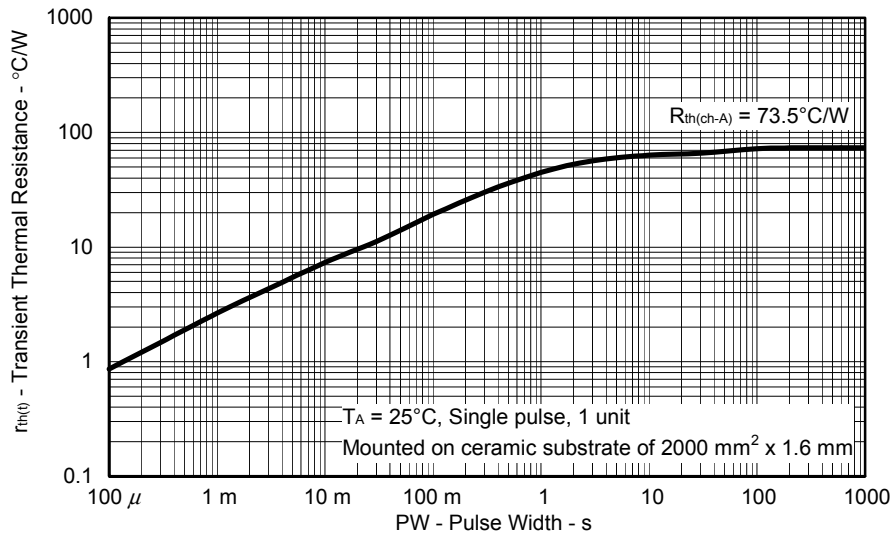
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



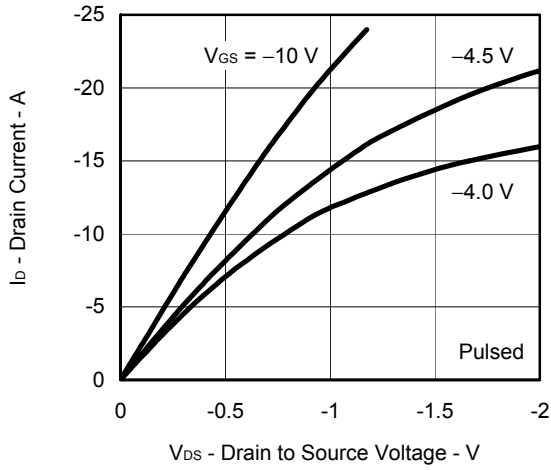
FORWARD BIAS SAFE OPERATING AREA



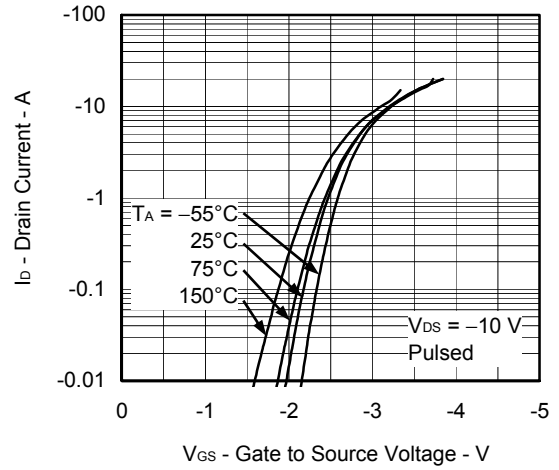
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



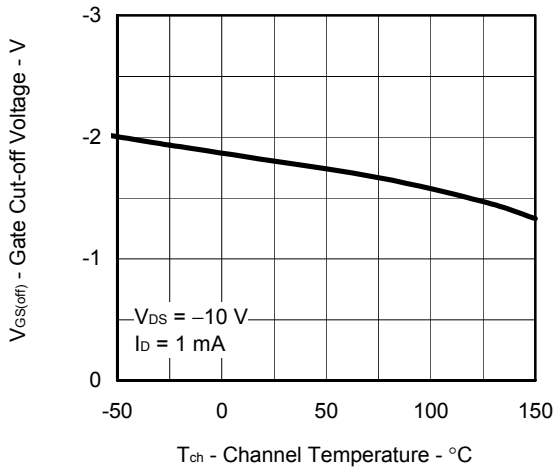
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



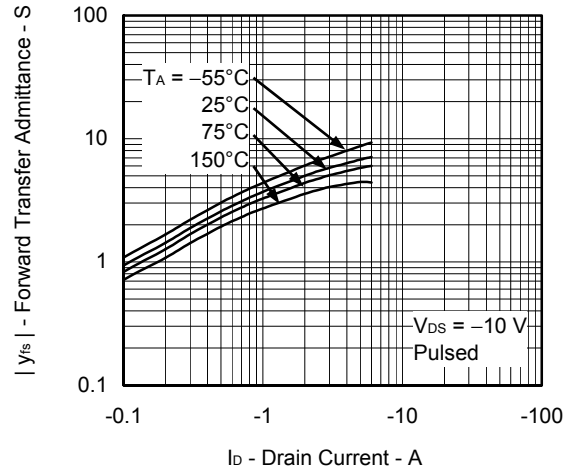
FORWARD TRANSFER CHARACTERISTICS



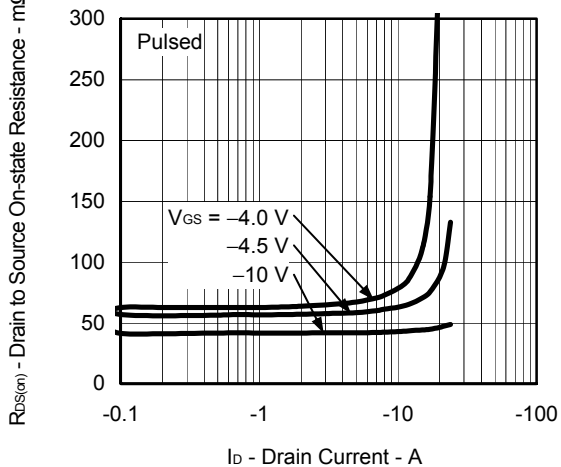
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



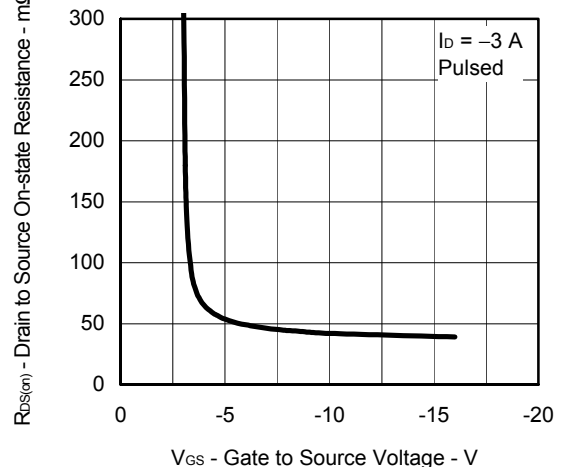
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



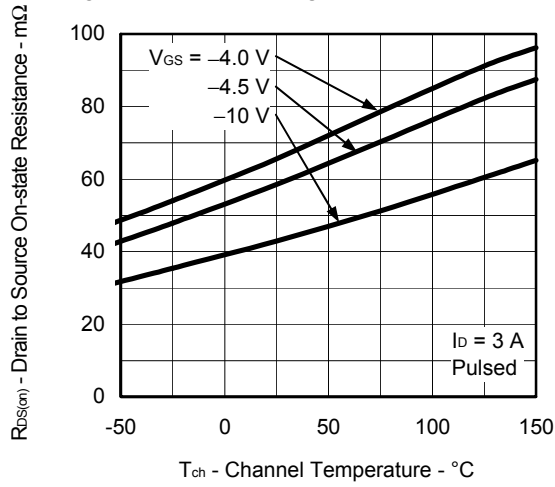
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



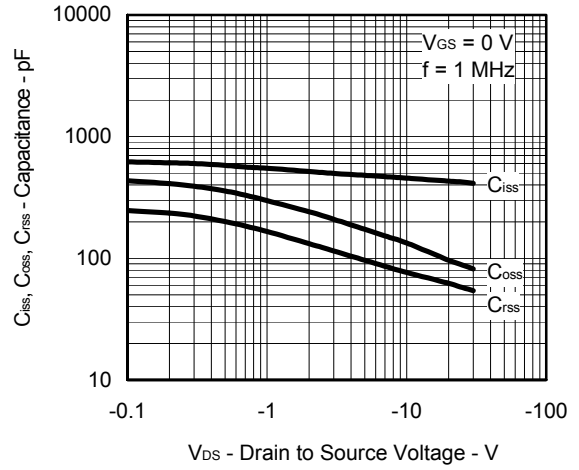
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



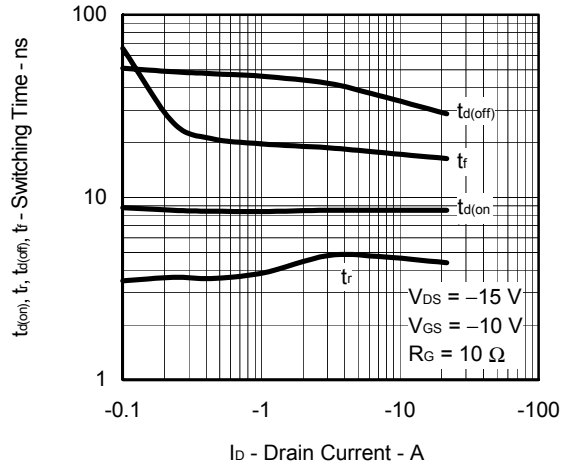
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



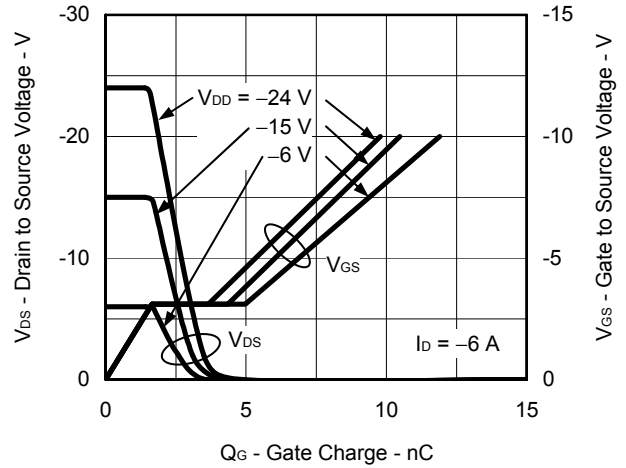
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



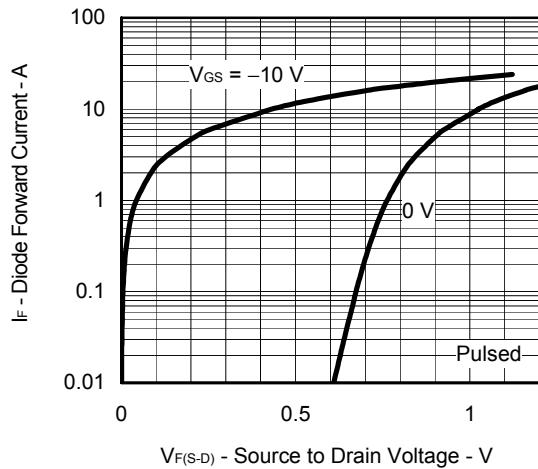
SWITCHING CHARACTERISTICS



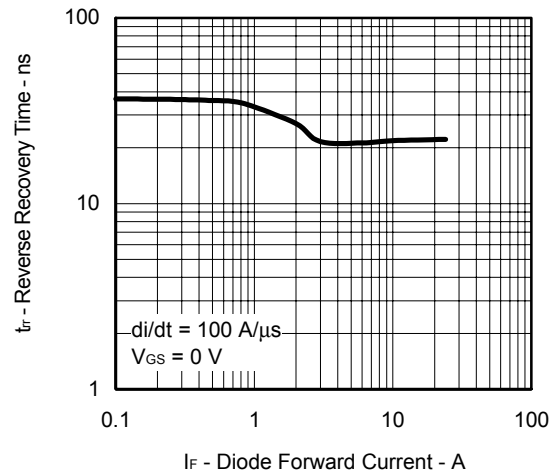
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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