

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2708GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 5.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9.0 \text{ A)}$
 $R_{DS(on)2} = 7.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 9.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 4700 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2708GR-E1	Power SOP8
μ PA2708GR-E2	Power SOP8
μ PA2708GR-E1-A ^{Note}	Power SOP8
μ PA2708GR-E2-A ^{Note}	Power SOP8

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 17	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 68	A
Total Power Dissipation ^{Note2}	P_{T1}	1.1	W
Total Power Dissipation (PW =10 sec) ^{Note2}	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	17	A
Single Avalanche Energy ^{Note3}	E_{AS}	28.9	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

Channel to Ambient ^{Note}	$R_{th(ch-A)}$	114	$^\circ\text{C/W}$
Channel to Drain Lead ^{Note}	$R_{th(ch-L)}$	30	$^\circ\text{C/W}$

Note Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

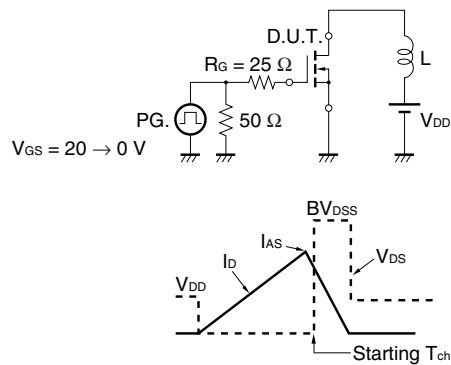
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

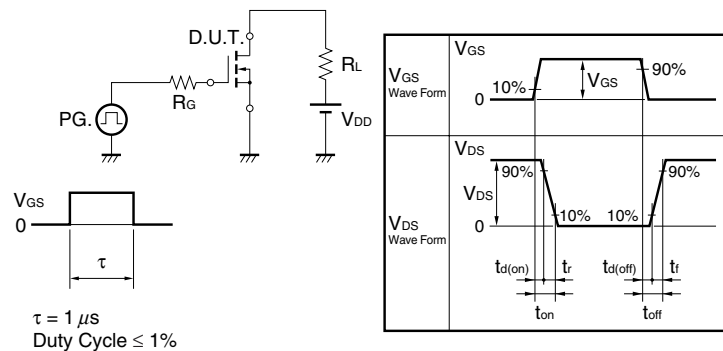
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.0		2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 9.0\text{ A}$	10			S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 9.0\text{ A}$		4.5	5.5	mΩ
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 9.0\text{ A}$		5.6	7.5	mΩ
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$		4700		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		670		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		340		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, I_D = 9.0\text{ A}$		19		ns
Rise Time	t_r	$V_{GS} = 10\text{ V}$		26		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		100		ns
Fall Time	t_f			27		ns
Total Gate Charge	Q_G	$V_{DD} = 15\text{ V}$		38		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = 5\text{ V}$		13		nC
Gate to Drain Charge	Q_{GD}	$I_D = 17\text{ A}$		12		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = 17\text{ A}, V_{GS} = 0\text{ V}$		0.8		V
Reverse Recovery Time	t_{rr}	$I_F = 17\text{ A}, V_{GS} = 0\text{ V}$		33		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		27		nC
Gate Resistance	R_G	$f = 1\text{ MHz}$		1.2		Ω

Note Pulsed

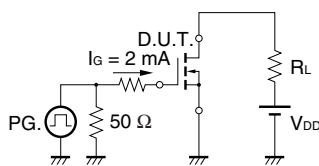
TEST CIRCUIT 1 AVALANCHE CAPABILITY



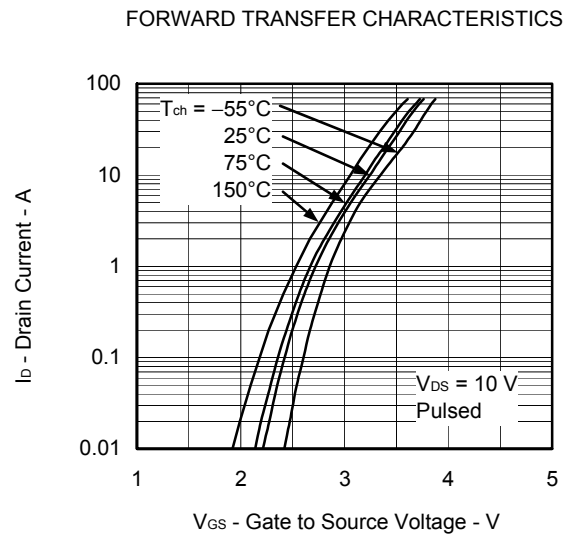
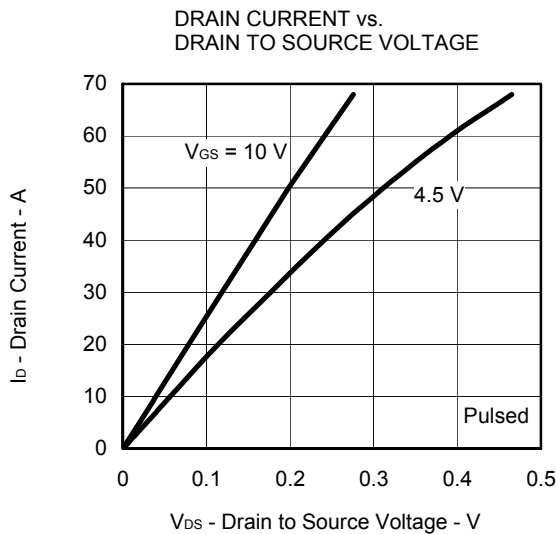
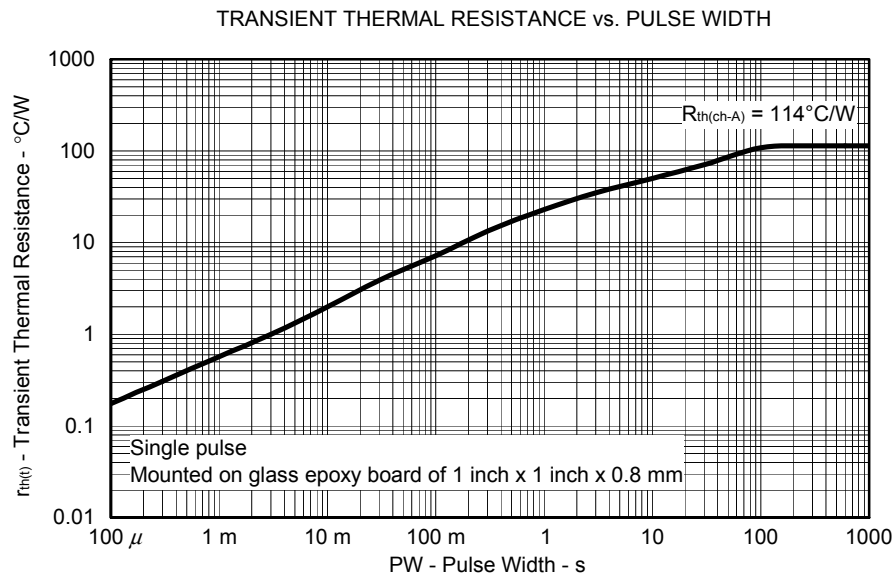
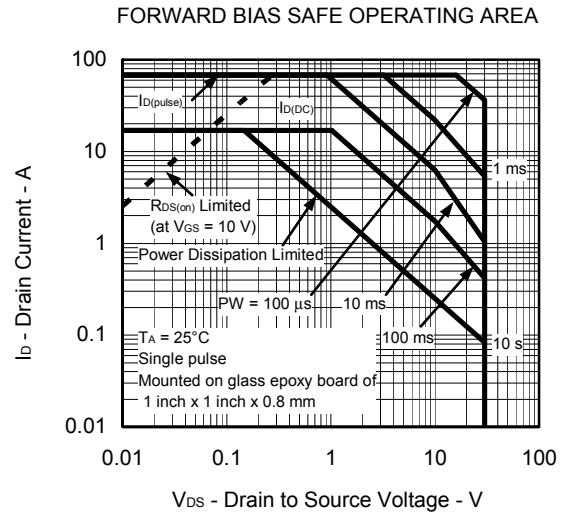
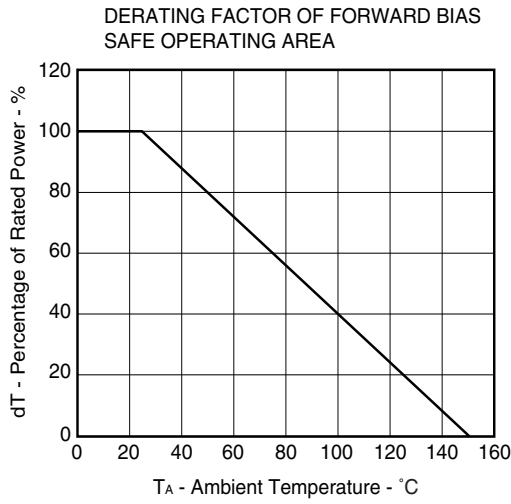
TEST CIRCUIT 2 SWITCHING TIME



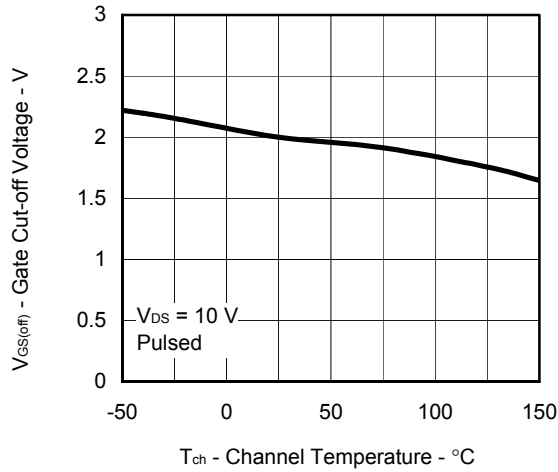
TEST CIRCUIT 3 GATE CHARGE



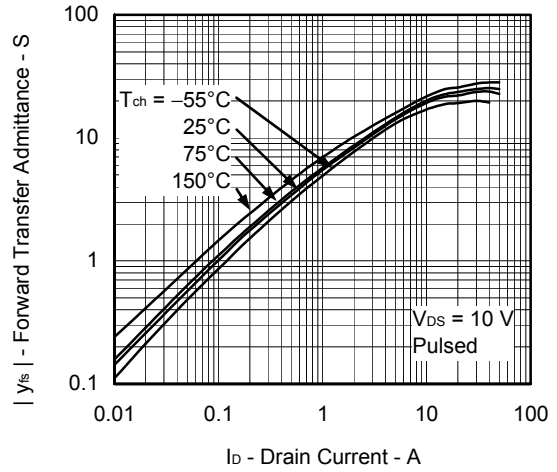
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



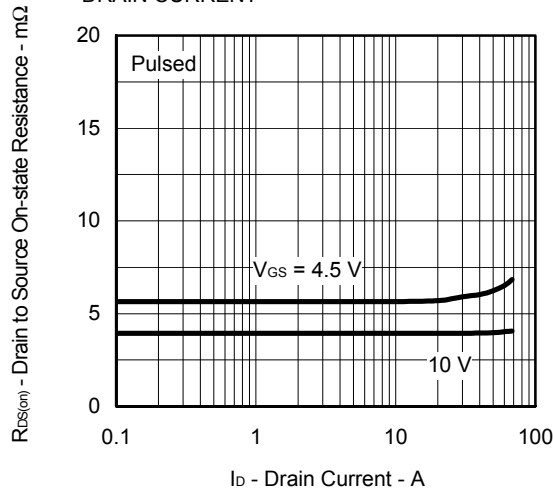
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



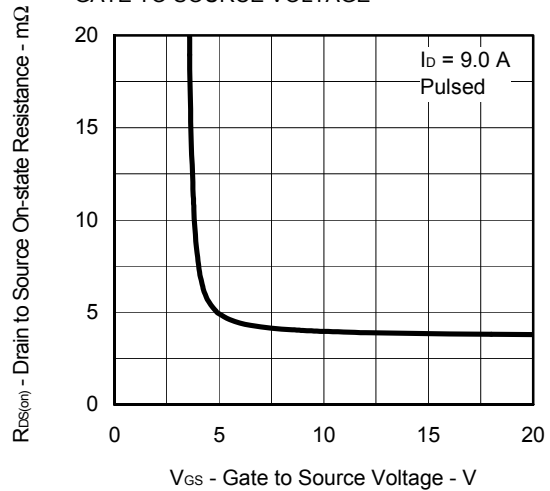
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



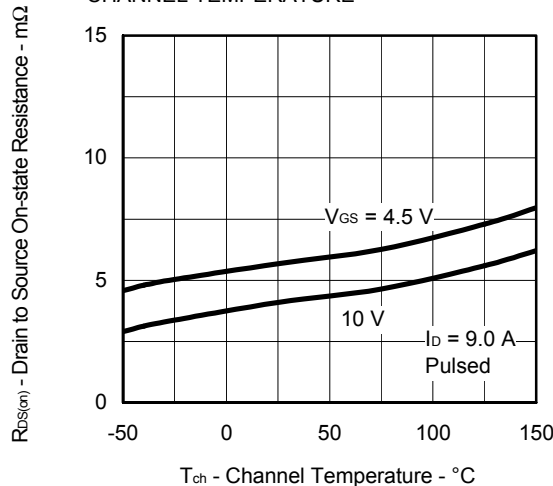
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



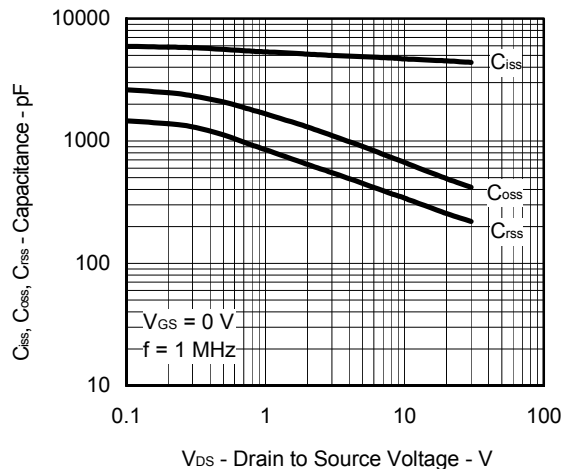
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



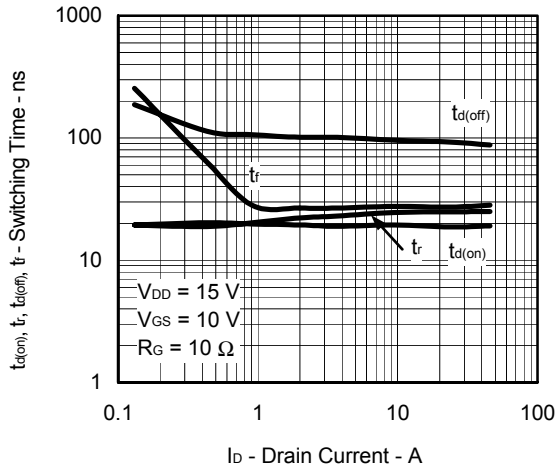
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



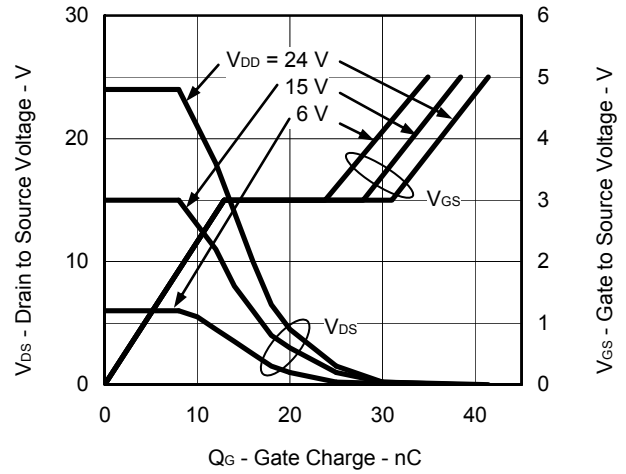
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



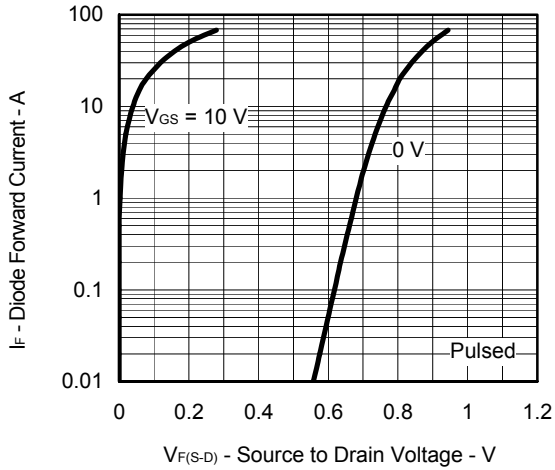
SWITCHING CHARACTERISTICS



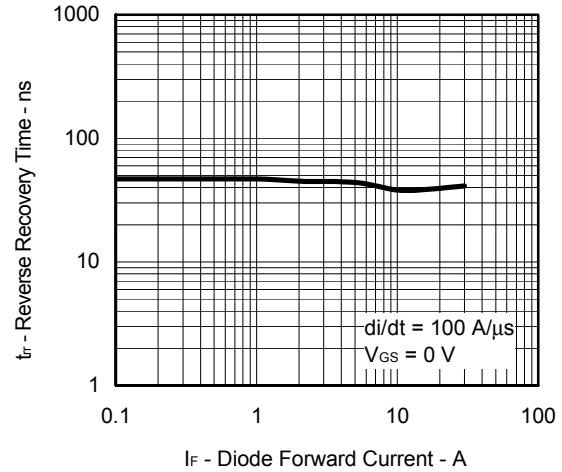
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



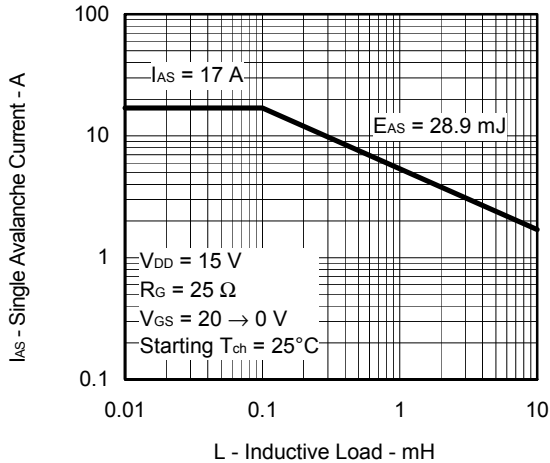
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



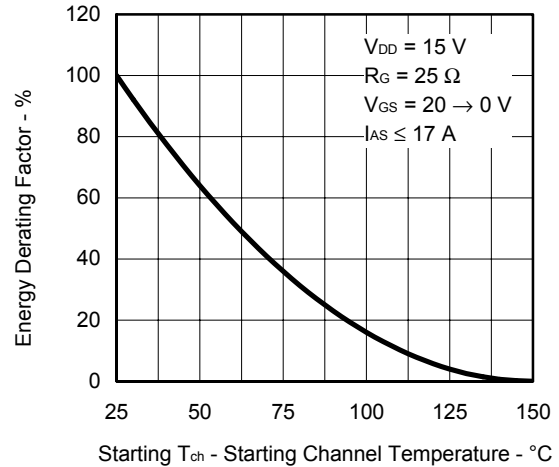
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

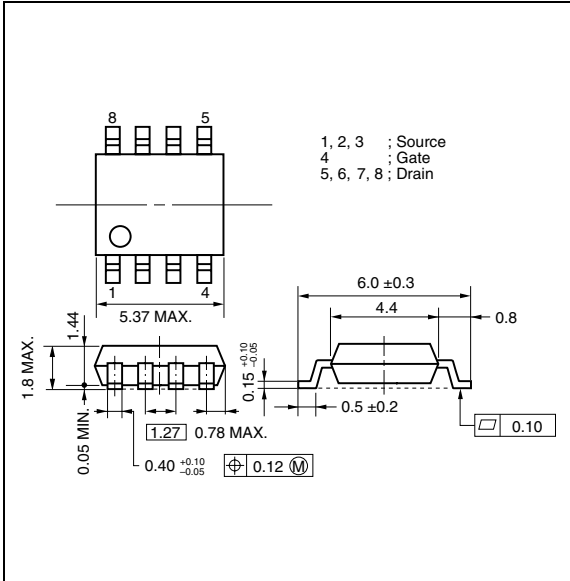


SINGLE AVALANCHE ENERGY DERATING FACTOR

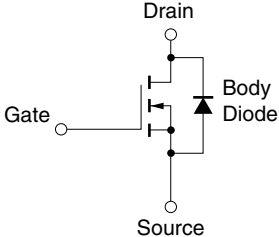


PACKAGE DRAWING (Unit: mm)

Power SOP8



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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