

HIGH-VOLTAGE MIXED-SIGNAL IC

UC1606

65COM x 132SEG Matrix LCD Controller-Driver

Product Specifications
Version 1.32

September 24, 2003

ULTRACHIP

The Coolest LCD Driver Ever!!

TABLE OF CONTENT

| | |
|--|-----------|
| Introduction | 1 |
| Ordering Information | 2 |
| Block Diagram..... | 3 |
| Pin Description..... | 4 |
| Control Registers..... | 7 |
| Command Table..... | 9 |
| Command description | 10 |
| LCD Voltage Settings | 15 |
| LCD Display Controls | 18 |
| Host Interface..... | 20 |
| Display Data RAM | 24 |
| Reset & Power Management..... | 27 |
| Absolute Maximum Ratings | 31 |
| Specifications..... | 32 |
| AC Characteristics..... | 33 |
| Physical Dimensions | 37 |
| Alignment Mark Information | 38 |
| Pad Coordinates | 39 |
| Tray Information..... | 42 |
| Revision History..... | 43 |

UC1606

Single-Chip, Ultra-Low Power Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1606 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1606 contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, and other battery operated devices and/or portable Instruments

FEATURE HIGHLIGHTS

- Support industry standard 8-bit parallel interface (8080 or 6800), 4-wire SPI (S8), and 3-wire SPI (S9) serial interface.
- Support four multiplexing rates (25, 33, 49, 65).
- Self-configuring 6x charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Software programmable 4 temperature compensation coefficients.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional for small LCD panels.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- V_{DD} (digital) range: 2.4V ~ 5V
 V_{DD} (analog) range: 2.4V ~ 5V
LCD V_{OP} range: 6.5V ~ 12.5V
- Available in gold bump dies
Bump pitch: 70uM min.
Bump gap: 24uM min.

ORDERING INFORMATION

| Product ID | Description |
|------------|-----------------------------|
| UC1606xGAF | 65 COM x 132 SEG LCD driver |

General Notes**APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

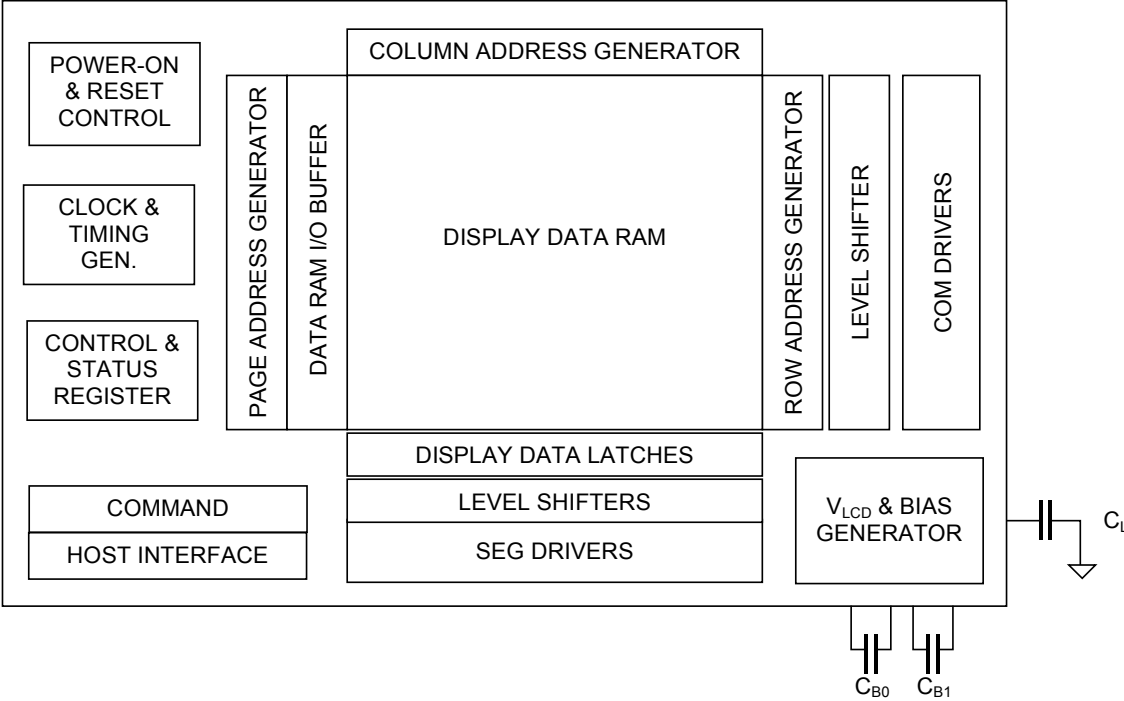
BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

BLOCK DIAGRAM



PIN DESCRIPTION

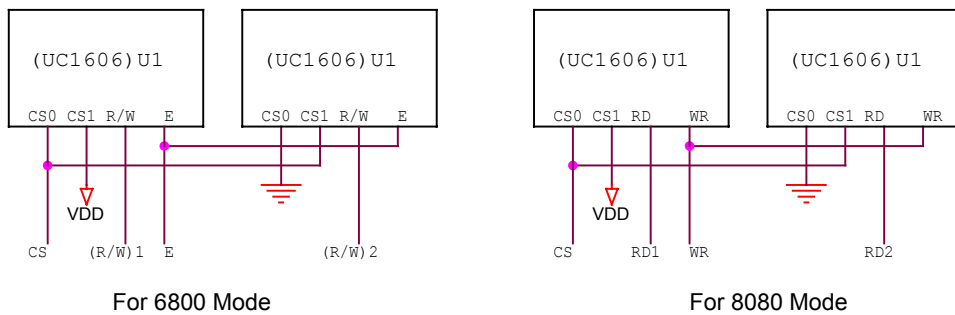
| Name | Type | Pins | Description |
|--|------|------|---|
| MAIN POWER SUPPLY | | | |
| V _{DD} V _{DD2} V _{DD3} | PWR | | V _{DD2} /V _{DD3} is the analog power supply and it should be connected to the same power source. V _{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V _{DD2} /V _{DD3} . Minimize the trace resistance for V _{DD} and V _{DD2} /V _{DD3} . |
| V _{SS} V _{SS2} | GND | | Ground. Connect V _{SS} and V _{SS2} to the shared GND pin. Minimize the trace resistance for V _{SS} and V _{SS2} . |
| LCD POWER SUPPLY | | | |
| V _{B1+} V _{B1-} V _{B0+} V _{B0-} | PWR | | LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C _{BX} value between V _{BX+} and V _{BX-} . The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image. |
| V _{LCD-IN} V _{LCD-OUT} | PWR | | Main LCD Power Supply. Connect these pins together. A by-pass capacitor C _L is optional. When C _L is used, connect C _L between V _{LCD} and V _{SS} , and keep the trace resistance under 300 Ohm. |

NOTE

- In COG applications, use one maximum width trace to connect V_{DD}/V_{DD2}/V_{DD3} to the LCM pad to minimize trace resistance. However, to avoid noise cross-coupling, insert a slit, 0.2~0.3mm long, between V_{DD}/V_{DD2}/V_{DD3}. Same treatment for V_{SS}/V_{SS2}.
- Recommended capacitor values:
C_B: 150 ~ 250x LCD load capacitance or 1.0uF (2V), whichever is higher.
C_L: 5nF ~ 20nF (16V) is appropriate for most applications.

| Name | Type | Pins | Description |
|--------------------------|------|------|--|
| LCD DRIVER OUTPUT | | | |
| SEG1 ~ SEG132 | HV | | SEG (column) driver outputs. Support up to 132 columns. Leave unused drivers open-circuit. |
| CIC | HV | | Icon driver output. |
| COM1 ~ COM64 | HV | | COM (row) driver outputs. Support up to 64 rows. When Mux Rate is not 65, please use only COM1~COM(x-1), x=65, 49, 33, or 25, and leave COM (x) ~ COM64 open-circuit. |
| MISC. PINS | | | |
| V _{DDX} | O | | Auxiliary V _{DD} . These pins are connected to the main V _{DD} bus on chip, and they are provided to facilitate chip configurations in COG and COF applications. There is no need to connect V _{DDX} to V _{DD} externally. These pins should not be used to provide V _{DD} power to the chip. |
| EO | O | | Reserved. Leave this pin open circuit. |
| TST4 | I | | Test control. Connect to V _{SS} . |
| TST[3:1] | I/O | | Test I/O pins. Leave these pins open circuit during normal use. |
| TP[3:1] | I | | Test control. Leave these pins open circuit during normal use. |

***1** When read data is needed under joint bus (using more than one UC1606), following application circuits are recommended. Each R/W (RD) pin should be separated from others.



CONTROL REGISTERS

UC1606 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. The commands supported by UC1606 are described in the next two sections, first a summary table, followed by a detailed description.

Name: The Symbolic reference of the register byte.
Note that, some symbol names refer to collection of bits (flags) within one register byte.

Default: Numbers shown in **Bold** fonts are values after *Power-Up-Reset* and *System-Reset*.

| Name | Bits | Default | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|------|---------|---|----------------------|------|------|------|------|----------|----|----|----|----|-----|------|-----|------|------|-----|-----|------|-------------|------|-------|------|------|------|------|------|------|
| SL | 6 | 0H | Start Line. Mapping from COM1 to Display Data RAM. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CR | 8 | 0H | Return Column Address. Useful for cursor implementation. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CA | 8 | 0H | Display Data RAM Column Address (Used in Host to Display Data RAM access) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PA | 4 | 0H | Display Data RAM Page Address (Used in Host to Display Data RAM access) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BR | 2 | PIN | Bias Ratio. The ratio between V_{LCD} and V_{BIAS} . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="5">Bias Ratio (BR[1:0])</th> </tr> <tr> <th>Mux Rate</th> <th>00</th> <th>01</th> <th>10</th> <th>11</th> </tr> </thead> <tbody> <tr> <td>65</td> <td>7.33</td> <td>8.0</td> <td>8.66</td> <td>9.33</td> </tr> <tr> <td>49</td> <td>6.0</td> <td>6.67</td> <td>7.33</td> <td>8.0</td> </tr> <tr> <td>33/25</td> <td>4.67</td> <td>5.33</td> <td>6.0</td> <td>6.66</td> </tr> </tbody> </table> Default value depends on BR[1:0] pin configuration, and can be re-defined by Set LCD Bias Ratio command. | Bias Ratio (BR[1:0]) | | | | | Mux Rate | 00 | 01 | 10 | 11 | 65 | 7.33 | 8.0 | 8.66 | 9.33 | 49 | 6.0 | 6.67 | 7.33 | 8.0 | 33/25 | 4.67 | 5.33 | 6.0 | 6.66 | | |
| Bias Ratio (BR[1:0]) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Mux Rate | 00 | 01 | 10 | 11 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 65 | 7.33 | 8.0 | 8.66 | 9.33 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 49 | 6.0 | 6.67 | 7.33 | 8.0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 33/25 | 4.67 | 5.33 | 6.0 | 6.66 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TC | 2 | PIN | Temperature Compensation (per °C). 00b: 0.0% 01b: -0.05% 10b: -0.1% 11b: -0.2% Default value depends on TC[1:0] pin configuration. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GN | 3 | 3H | Gain, coarse setting of V_{BIAS} and V_{LCD} <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="9">GN[2:0]</th> </tr> <tr> <th></th> <th>000</th> <th>001</th> <th>010</th> <th>011</th> <th>100</th> <th>101</th> <th>110</th> <th>111</th> </tr> </thead> <tbody> <tr> <td>Gain</td> <td>1.43</td> <td>1.58</td> <td>1.72</td> <td>1.89</td> <td>2.08</td> <td>2.28</td> <td>2.49</td> <td>2.72</td> </tr> </tbody> </table> | GN[2:0] | | | | | | | | | | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | Gain | 1.43 | 1.58 | 1.72 | 1.89 | 2.08 | 2.28 | 2.49 | 2.72 |
| GN[2:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | | | | | | | | | | | | | | | | | | | | | | |
| Gain | 1.43 | 1.58 | 1.72 | 1.89 | 2.08 | 2.28 | 2.49 | 2.72 | | | | | | | | | | | | | | | | | | | | | | |
| PM | 6 | 10H | Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MR | 2 | PIN | Multiplexing Rate: Number of pixel rows: 00b: 25 01b: 33 10b: 49 11b: 65 Default value depends on MR[1:0] pin configuration. | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Name | Bits | Default | Description |
|------|------|---------|---|
| OM | 2 | – | Operating Modes (Read Only) 10b: Sleep 11b: Normal 01b: (Not used) 00b: Reset |
| BZ | 1 | – | Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access. |
| RS | 1 | | Reset in progress, Host Interface not ready |
| PC | 3 | 7H | Vlcd pump control. PC[0]: 0b: Low LCD loading 1b: Regular LCD loading PC[2:1]: 00b: External Vlcd 01b: 4x 10b: 5x 11b: 6x |
| APC0 | 8 | 6CH | Advanced Product Configuration. For UltraChip only. Please do not use. |
| DC | 3 | 0H | Display Control: DC[0]: PXV: Pixels Inverse (Default: OFF) DC[1]: APO: All Pixels ON (Default: OFF) DC[2]: Display ON/OFF (Default: OFF). |
| AC | 4 | 0H | Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default 0:OFF) AC[1]: Reserved (always set to 0) AC[2]: PID: PA (page address) auto increment direction (0: +1 1: -1) AC[3]: CUM: Cursor update mode, (Default 0:OFF) when CUM=1, CA increment on write only, wrap around suspended |
| LC | 4 | 0H | LCD Mapping Control: LC[0]: MSF: MSB First mapping Option LC[1]: Reserved (always set to 0) LC[2]: MX, Mirror X (Column sequence inversion) LC[3]: MY, Mirror Y (Row sequence inversion) |

COMMAND TABLE

The following is a list of host commands supported by UC1606

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
Useful Data bits
- Don't Care

| | Command | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Action | Default value |
|----|---|-----|-----|----|----|----|----|----|----|----|----|------------------------------------|---------------|
| 1 | Write Data Byte | 1 | 0 | # | # | # | # | # | # | # | # | Write 1 byte | N/A |
| 2 | Read Data Byte | 1 | 1 | # | # | # | # | # | # | # | # | Read 1 byte | N/A |
| 3 | Get Status | 0 | 1 | BZ | MX | DE | RS | 0 | 0 | 0 | 0 | Get Status | N/A |
| 4 | Set Column Address LSB | 0 | 0 | 0 | 0 | 0 | 0 | # | # | # | # | Set CA[3:0] | 0 |
| | Set Column Address MSB | 0 | 0 | 0 | 0 | 0 | 1 | # | # | # | # | Set CA[7:4] | 0 |
| 5 | Set Gain | 0 | 0 | 0 | 0 | 1 | 0 | 0 | # | # | # | Set GN[2:0] | 011b |
| 6 | Set Pump Control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | # | # | # | Set PC[2:0] | 111b |
| 7 | Set Adv. Product Config. (double byte command) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R | For UltraChip only. Do not use. | N/A |
| | | 0 | 0 | # | # | # | # | # | # | # | # | | |
| 8 | Set Start Line | 0 | 0 | 0 | 1 | # | # | # | # | # | # | Set SL[5:0] | 0 |
| 9 | Set Page Address | 0 | 0 | 1 | 0 | 1 | 1 | # | # | # | # | Set PA[3:0] | 0 |
| 10 | Set Potentiometer (double-byte command) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set PM[5:0] | PM=16 |
| | | 0 | 0 | - | - | # | # | # | # | # | # | | |
| 11 | Set RAM Address Control | 0 | 0 | 1 | 0 | 0 | 0 | 1 | # | 0 | # | Set AC[2:0] | 000b |
| 12 | Set Column Mirroring | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | # | Set LC[3] | 0 |
| 13 | Set All-Pixel-ON | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | # | Set DC[1] | 0=disable |
| 14 | Set Inverse Display | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | # | Set DC[0] | 0=disable |
| 15 | Set Display Enable | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | # | Set DC[2] | 0=disable |
| 16 | Set LCD Mapping Control | 0 | 0 | 1 | 1 | 0 | 0 | # | # | 0 | # | Set LC[3:0] | 0 |
| 17 | System Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | System Reset | N/A |
| 18 | NOP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | No operation | N/A |
| 19 | Set LCD Bias Ratio | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | Set BR[1:0] | PIN |
| 20 | Reset Cursor Mode | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | AC[3]=0, CA=CR | N/A |
| 21 | Set Cursor Mode | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | AC[3]=1, CR=CA | N/A |
| 22 | Set Test Control (double byte command) | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | TT | | For UltraChip only. Do not use. | N/A |
| | | 0 | 0 | # | # | # | # | # | # | # | # | | |

* Other than commands listed above, all other bit patterns may result in undefined behavior.

COMMAND DESCRIPTION

(1) Write data to display memory

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|--------------------------|----|----|----|----|----|----|----|
| Write data | 1 | 0 | 8bits data write to SRAM | | | | | | | |

(2) Read data to display memory

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|-----|-----|----------------------|----|----|----|----|----|----|----|
| Read data | 1 | 1 | 8bits data from SRAM | | | | | | | |

Write/Read Data Byte (command 1,2) operation accesses display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will be increased or decreased automatically depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decreased by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

(3) Get Status

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|----|----|----|----|----|----|----|----|
| Get Status | 0 | 1 | BZ | MX | DE | RS | 0 | 0 | 0 | 0 |

Status flag definitions:

BZ: Busy with internal process. When BZ=1 host interface can access if RS=0.

MX: Status of register LC[2], mirror X.

DE: Display enable flag. DE=1 when display enabled

RS: Reset in progress. If RS=1, host interface will be inaccessible.

(4) Set Column Address

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|-----|-----|----|----|----|----|-----|-----|-----|-----|
| Set Column Address LSB CA[3:0] | 0 | 0 | 0 | 0 | 0 | 0 | CA3 | CA2 | CA1 | CA0 |
| Set Column Address MSB CA[7:4] | 0 | 0 | 0 | 0 | 0 | 1 | CA7 | CA6 | CA5 | CA4 |

Set the SRAM column address before Write/Read memory from host interface.

CA possible value=**0-131**

(5) Set Gain

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------|-----|-----|----|----|----|----|----|-----|-----|-----|
| Set Gain GN[2:0] | 0 | 0 | 0 | 0 | 1 | 0 | 0 | GN2 | GN1 | GN0 |

Program Gain (GN[2:0]) . See section LCD VOLTAGE SETTING for more detail.

| | GN[2:0] | | | | | | | |
|-------------|---------|------|------|------|------|------|------|------|
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| Gain | 1.43 | 1.58 | 1.72 | 1.89 | 2.08 | 2.28 | 2.49 | 2.72 |

(6) Set Pump Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------|-----|-----|----|----|----|----|----|-----|-----|-----|
| Set Pump Control PC[2:0] | 0 | 0 | 0 | 0 | 1 | 0 | 1 | PC2 | PC1 | PC0 |

Set PC[2:0] to program to use internal charge pump of external VLCD source:

PC[0]: **0b**: Low LCD loading **1b**: Regular LCD loading
 PC[2:1]: **00b**: External V_{LCD} **01b**: 4x
 10b: 5x **11b**: 6x

(7) Set Advance Product Configuration

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|------------------------|----|----|----|----|----|----|----|
| Set APC[0] | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | R |
| (Double byte command) | 0 | 0 | APC register parameter | | | | | | | |

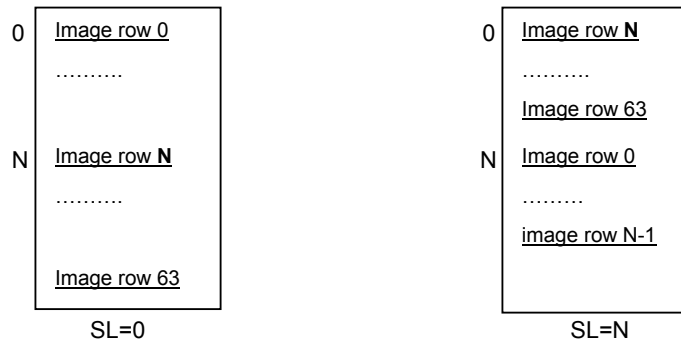
For UltraChip only. Please do NOT use.

(8) Set Start Line

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|-----|-----|----|----|-----|-----|-----|-----|-----|-----|
| Set Start Line SL[5:0] | 0 | 0 | 0 | 1 | SL5 | SL4 | SL3 | SL2 | SL1 | SL0 |

Set the start line number

Start line setting will scroll the displayed image up by SL rows. The valid value is between 0 (no scrolling) and 63. One example of the visual effect on LCD is illustrated in the figure below.



COM Icon (CIC) is not affected by this command.

(9) Set Page Address

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------------|-----|-----|----|----|----|----|-----|-----|-----|-----|
| Set Page Address LSB PA [3:0] | 0 | 0 | 1 | 0 | 1 | 1 | PA3 | PA2 | PA1 | PA0 |

Set the SRAM page address before write/read memory from host interface.

Effective range of value = **0 ~ 8**

(10) Set Potentiometer

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|-----|-----|----|----|-----|-----|-----|-----|-----|-----|
| Set Potentiometer PM [5:0] (Double byte command) | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | 0 | 0 | - | - | PM5 | PM4 | PM3 | PM2 | PM1 | PM0 |

Program Potentiometer (PM[5:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range of PM value = 0 ~ 63

(11) Set RAM Address Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|----|----|----|----|----|-----|-----|-----|
| Set AC [2:0] | 0 | 0 | 1 | 0 | 0 | 0 | 1 | AC2 | AC1 | AC0 |

Program registers AC[2:0] for RAM address control.

AC[0] -- Automatic column/page wrap around (WA).

AC[1] – Reserved. (Always set to 0).

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
 The column address will be reset to 0 and page address will increase/decrease
 (+/- 1 depend on PID = 0/1) after column address equal to maximum column value.

(12) Set Column Mirroring

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------------|-----|-----|----|----|----|----|----|----|----|----|
| Set Column Mirroring LC [3] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | MY |

Set LC[2] for COM (row) mirror (MY).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

(13) Set All Pixel ON

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set All Pixel ON DC [1] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | DC1 |

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(14) Set Inverse Display(PXV)

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set Inverse Display DC [0] | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | DC0 |

Set DC[0] to force all SEG drivers to output the inverse of the data which stored in display memory. This function has no effect on the existing data stored in display RAM.

(15) Set Display Enable

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set Display Enable DC[2] | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | DC2 |

This command is for programming registers DC[2].

When DC[2] is set to 1, UC1606 will turn on COM drivers and SEG drivers.

(16) Set LCD Mapping Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------|-----|-----|----|----|----|----|----|----|-----|-----|
| Set LCD Mapping Control LC[3:0] | 0 | 0 | 1 | 1 | 0 | 0 | MY | MX | LC1 | MSF |

Set LC[3:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 131-CA as write/read(from host interface) display RAM column address so this function will only take effect after rewriting the RAM data

LC1 – Reserved. (Always set to 0).

MSF is implemented by MSB-LSB swapping. When MSB first (LC[0]) bit is set, data D[7:0] will be re-aligned then stored to RAM.

(17) System Reset

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|----|----|----|----|----|----|----|----|
| System Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

This command will activate the system reset. The system will take about 5ms to reset

(18) NOP

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|----|----|----|----|----|----|----|----|
| No operation | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

This command is used for “no operation”.

(19) Set LCD Bias Ratio

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|-----|-----|----|----|----|----|----|----|-----|-----|
| Set Bias Ratio BR [1:0] | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BR1 | BR0 |

Bias ratio definition:

| | Bias Ratio (BR[1:0]) | | | |
|----------|----------------------|------|------|------|
| Mux Rate | 00 | 01 | 10 | 11 |
| 65 | 7.33 | 8.0 | 8.66 | 9.33 |
| 49 | 6.0 | 6.67 | 7.33 | 8.0 |
| 33/25 | 4.67 | 5.33 | 6.0 | 6.66 |

(20) Reset Cursor Mode

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|-----|-----|----|----|----|----|----|----|----|----|
| Return to cursor. AC[3]=0, CA=CR | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

This command is used to reset cursor update mode function. See description below.

(21) Set Cursor Mode

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|-----|-----|----|----|----|----|----|----|----|----|
| Set AC[3]=1 CR=CA | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

Set Cursor Mode command is used to turn on cursor update mode function. AC[3] will be set to 1, register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increment with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support "Read-Modify-Write" for cursor implementation.

Reset Cursor Mode command will clear cursor update mode flag (AC[3]=0), CA will be restored to previous CA value which is stored in CR, and CA, PA increment will return to its normal condition.

(22) Set Test Control

| Action | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|-------------------|----|----|----|----|----|----|----|
| Set TT | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | TT | |
| (Double byte command) | 0 | 0 | Testing parameter | | | | | | | |

This command is used for UltraChip production testing. For UltraChip Only. Please do not use.

LCD VOLTAGE SETTINGS

MULTIPLEX RATES

Four multiplex rates are supported in UC1606 (65, 49, 33, 25). MR is not software programmable. It is determined by pin programming.

BIAS SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_B , i.e. $BR = V_{LCD}/V_B$, where $V_B = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The reference *Bias Ratio* can be estimated by:

$$\sqrt{Mux + 1}$$

UC1606 supports four bias ratios for each MR (Mux Rate) setting as illustrated below.

| Mux Rate | Bias Ratio (BR[1:0]) | | | |
|----------|----------------------|------|------|------|
| | 00 | 01 | 10 | 11 |
| 65 | 7.33 | 8.0 | 8.66 | 9.33 |
| 49 | 6.0 | 6.67 | 7.33 | 8.0 |
| 33/25 | 4.67 | 5.33 | 6.0 | 6.66 |

Table 1: BR vs. Mux Rates

BR can be selected either by software program or by hardware pin wiring.

V_B GENERATION

V_B is generated internally by UC1606. The value of V_B is determined by three control registers: *GN* (Gain), *PM* (Potential Meter), *TC* (Temperature Compensation) with the following relationship:

$$V_B = Gain \times V_{PM}$$

where V_{PM} is the output of an internal Electronic Potential Meter.

The value of V_{PM} is given by:

$$V_{PM} = \frac{600 + PM}{1200} \times V_{REF}$$

The value of *Gain* is controlled by *GN*[2:0]. Their relationship is shown below:

| Gain | GN[2:0] | | | | | | | |
|------|---------|------|------|------|------|------|------|------|
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| Gain | 1.43 | 1.58 | 1.72 | 1.89 | 2.08 | 2.28 | 2.49 | 2.72 |

Table 2: Gain vs. GN value

V_{REF} Temperature Compensation

V_{REF} is a temperature compensated reference voltage. V_{REF} increases automatically as ambient temperature cools down.

Four (4) different temperatures compensated V_{REF} can be selected via pin wiring. The compensation coefficient is given by the following table:

| TC[1:0] | 00 | 01 | 10 | 11 |
|----------|-----|-------|-------|-------|
| % per °C | 0.0 | -0.05 | -0.10 | -0.20 |

Table 3: Temperature Compensation

For all TC values, V_{REF} are normalized to 1.25V at 25 °C. When selecting TC, make sure V_{B+} and V_{LCD} stays within specified UC1606 ratings across entire operating temperature range.

V_{LCD} SELECTION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by *PC*[2:1].

When V_{LCD} is generated internally its value has the following relationship with V_B :

$$V_{LCD} = BiasRatio \times V_B$$

Given $V_{REF} = 1.25V$ at 25 °C, V_{LCD} becomes:

$$V_{LCD} \cong BiasRatio \times Gain \times \frac{600 + PM}{1200} \times 1.25 \quad (1)$$

When *PM*=0, then equation (1) becomes:

$$V_{LCD} \cong BiasRatio \times Gain / 1.6 \quad (1b)$$

LOAD DRIVING STRENGTH

UC1606's drivers and power supply circuits are designed to handle capacitance load of >2.5pF per pixel at $V_{LCD}=10.5V$ when $V_{DD2} > 2.4V$.

UC1606 load driving strength is sensitive to ITO impedance of power supply circuits (V_{DD} , V_{SS} , $V_{B0/B1}$, V_{LCD} .) Be sure to minimize these ITO trace resistance for COG applications.

POWER SUPPLY CONFIGURATION

UC1606 has built-in charge pump with on-chip pumping capacitors. The number of pump stages can be programmed by setting *PC*[2:1] register. Make sure the chip is in Reset mode before changing the value of *PC*[2:0].

Given the same display quality, the lower *PC*[2:1] setting the more efficient is UC1606, but the weaker is the driving strength. In application,

designers are recommended to verify the design with the highest setting first before trying lower settings to achieve better efficiency.

Due to the use of fully embedded power supply, built-in power ready detector, and drain circuit, there is no rigid power up or power down sequences for UC1606

controllers when using internal V_{LCD} generator.

On the other hand, caution must be exercised when external V_{LCD} source is used. The general rule of thumb is to make sure Display Enable is OFF before connecting or disconnecting external V_{LCD} sources.

Hi-V GENERATOR AND BIAS REFERENCE CIRCUIT

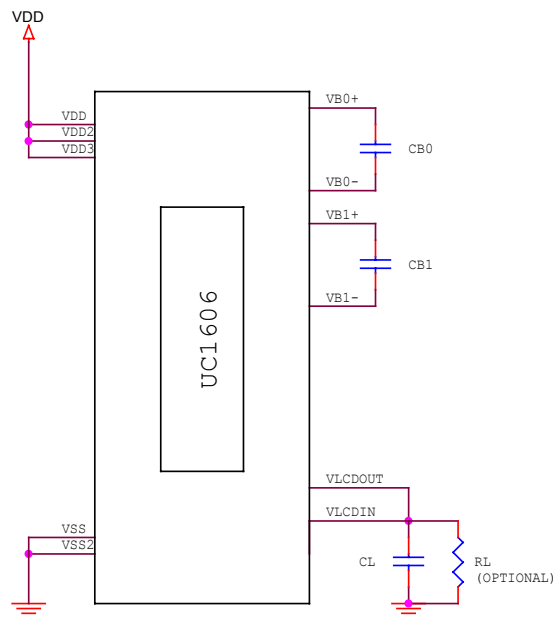


FIGURE 1: Reference circuit using internal Hi-V generator circuit

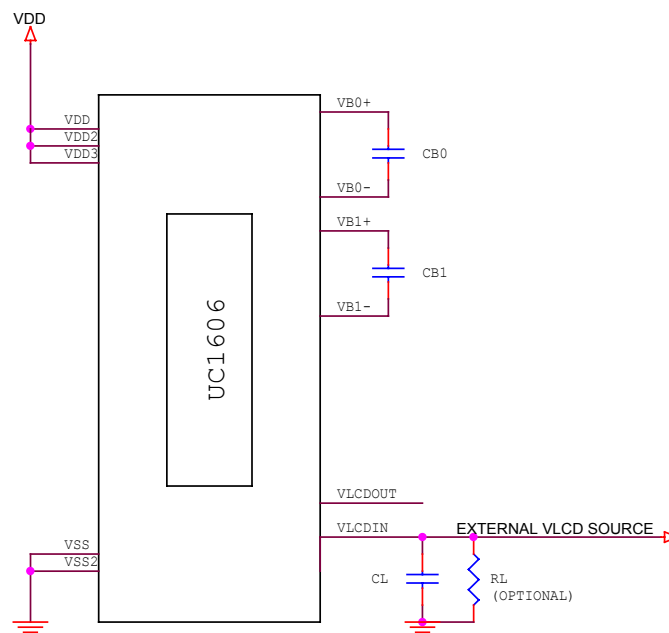


FIGURE 2: Reference circuit using external Hi-V source

Note

- Recommended component values:
 - C_B : $\sim 100 \times$ LCD load capacitance or $1.0 \mu\text{F}$ (2V), whichever is higher.
 - C_L : $5 \text{ nF} \sim 20 \text{ nF}$ (16V) is appropriate for most applications.
 - R_L : $10 \text{ M}\Omega$. Acts as a draining circuit when the power is abnormally shut down.
- The illustrated resistor values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1606 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in Idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in Idle mode, their outputs are connected to V_{SS} .

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where $x=1\sim 65$, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is the same for all MR, MX and MY settings. When MR is not 65, then COM(x) ~ COM65 ($X = MR+1$) should be left open circuit.

Display Controls

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command.

When DC[2] is set to OFF (logic "0"), both SEG and COM drivers will become idle and UC1606 will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1606 will first exit from Sleep mode, restore the power (V_{LCD} , V_{BIAS} etc.) and then turn on COM drivers and proper SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all active SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

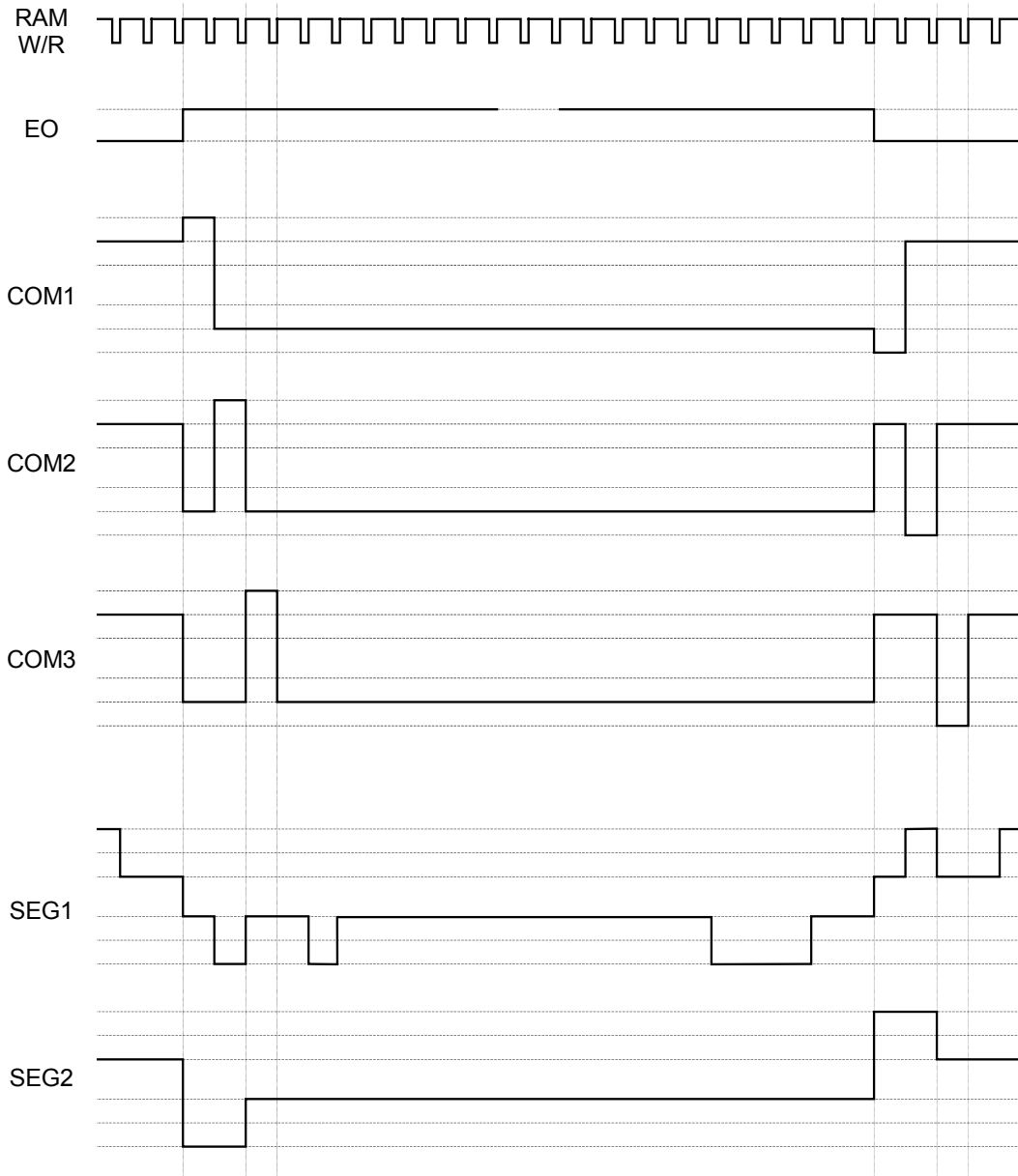


Figure 3: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1606 supports two 8-bit parallel bus protocols and two serial bus protocols. Designers can choose either

the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

| Bus Type | | 8080 | 6800 | SPI (S8) | SPI(S9) | |
|---------------------|---------|-----------------------|-------------------|----------|----------------|--|
| Control & Data Pins | PS[1:0] | 10b | 11b | 00b | 01b | |
| | CS[1:0] | Chip Select | | | | |
| | CD | Control/Data | | | | |
| | WR0 | \overline{WR} | R/ \overline{W} | 0 | 0 | |
| | WR1 | \overline{RD} | EN | 0 | 0 | |
| | Access | Read/Write | | | Write Only | |
| | D[7:0] | 8-bit bus (Tri-state) | | | D0=SCK, D2=SDA | |

* Connect unused control pins to V_{DD} or V_{SS} .

Table 4: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1606 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in

parallel mode or serial mode, by either *Set CA* or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

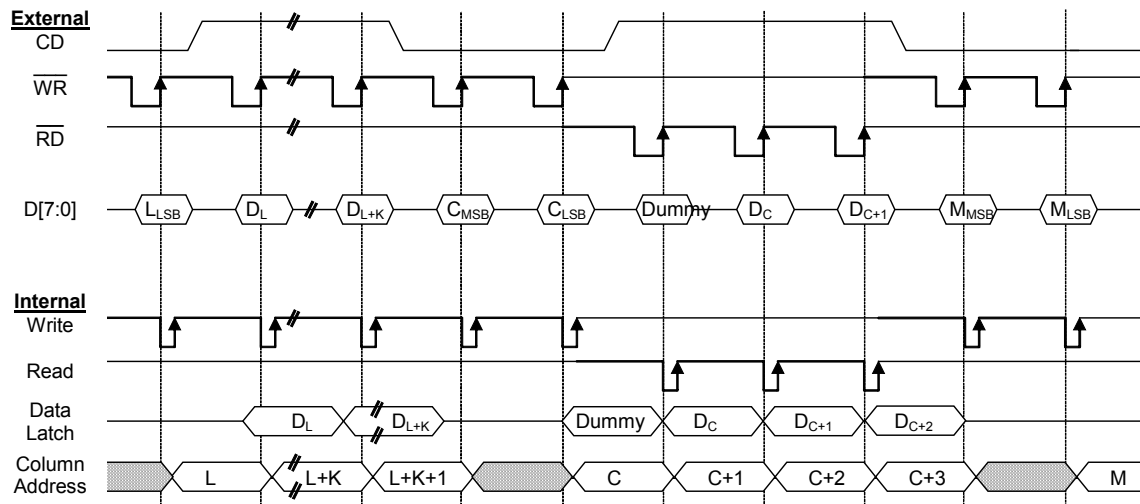


Figure 4: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1606 supports two serial modes, 4-wire mode (PS="LL"), and 3-wire mode (PS="LH"). The mode of interface is determined during power-up process by the value of PS[1:0].

4-WIRE SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each

write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

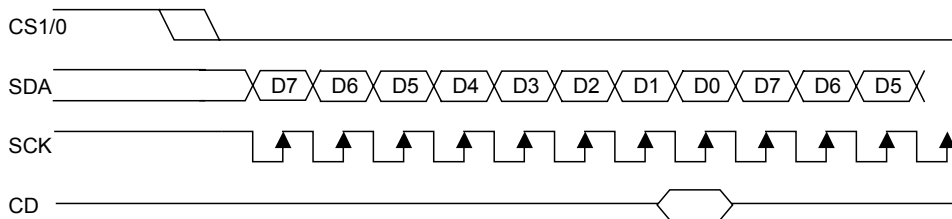


Figure 5.a: 4-wire Serial Interface (S8)

3-WIRE SERIAL INTERFACE (S9)

Only write operations are supported in 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data

and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}.

The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

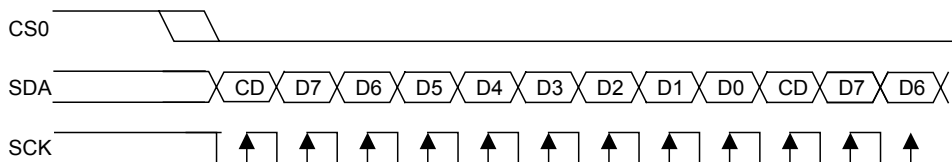


Figure 5.b: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

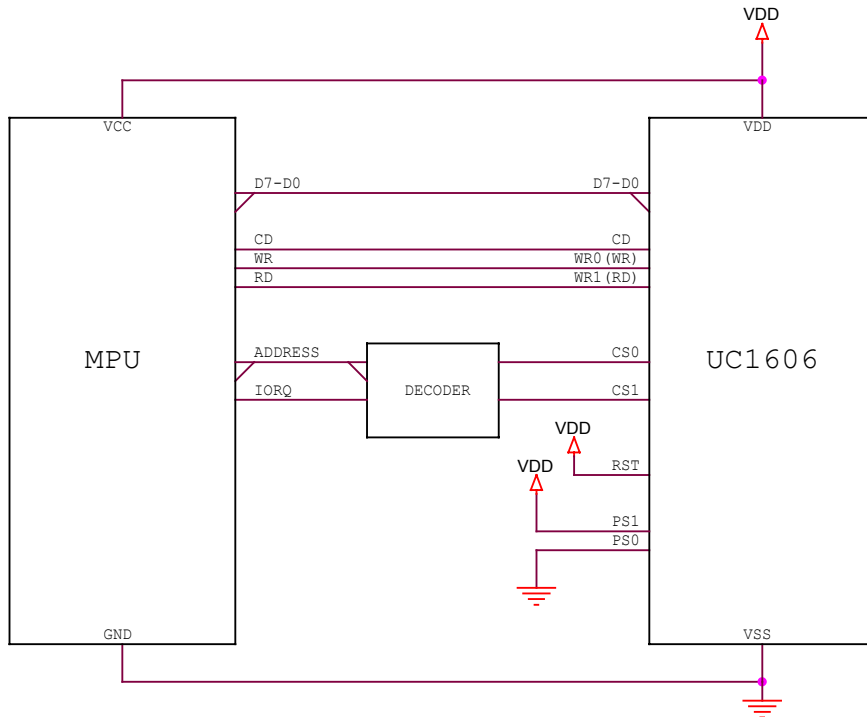


FIGURE 6: 8080/8bit parallel mode reference circuit

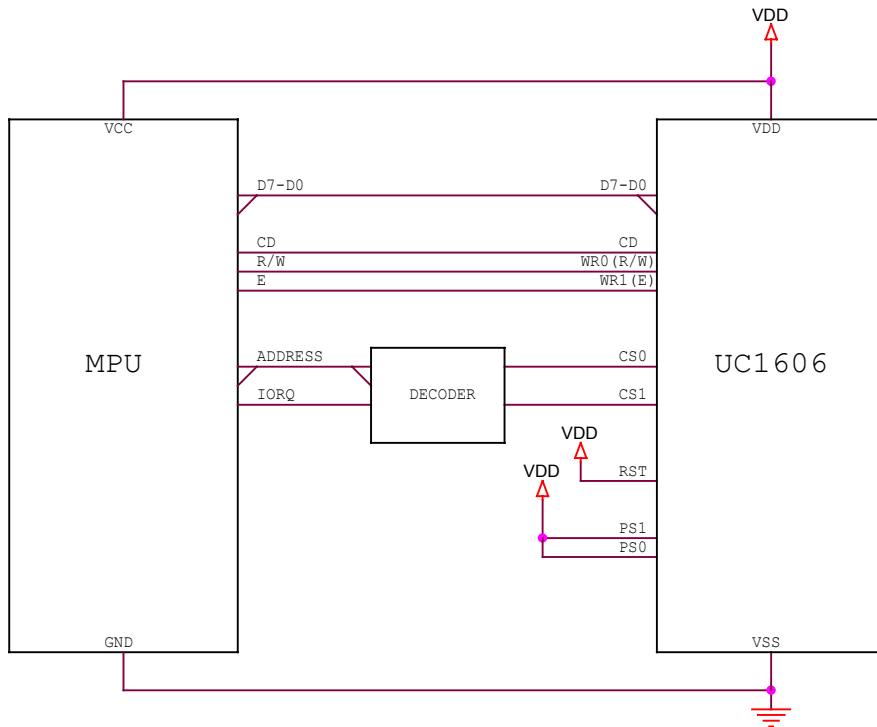


FIGURE 7: 6800/8bit parallel mode reference circuit

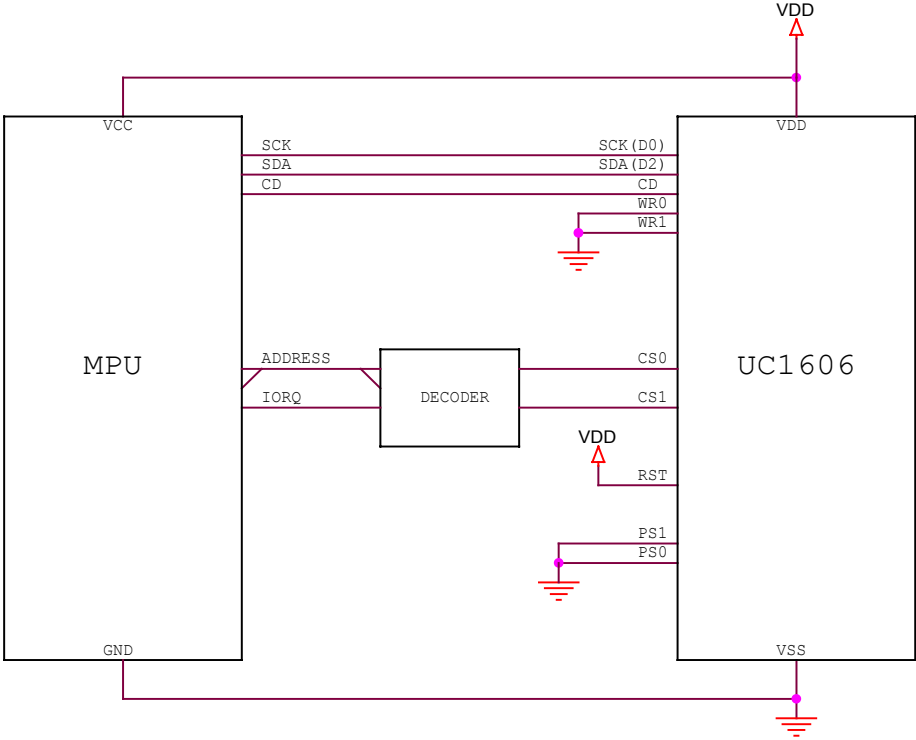


FIGURE 8: Serial-8 serial mode reference circuit

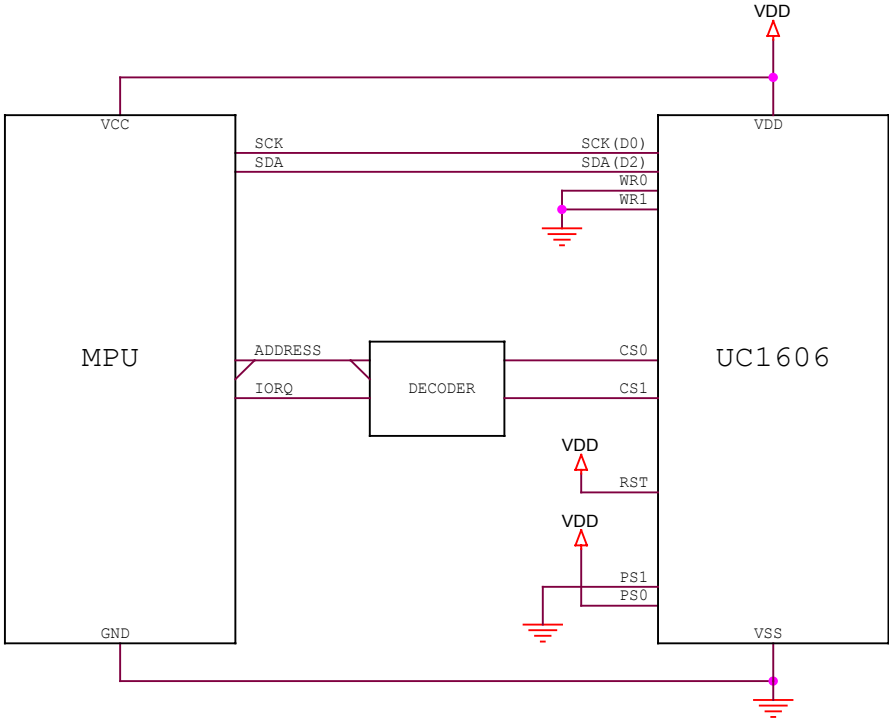


FIGURE 9: Serial-9 serial mode reference circuit

Note: RST pin is optional. When RST pin is not used, connect the pin to VDD.

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is 1-bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 65 x 132 for UC1606. This array of data bits is further organized into pages of 8 bit slices to facilitate parallel bus interface.

When Mirror X (MX, LC[2]) is OFF, the 1st column of LCD pixels will correspond to the bits of the first byte of each page, the 2nd column of LCD pixels correspond to the bits of the second byte of each page, etc.

MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated in next page.

DISPLAY DATA RAM ACCESS

The memory used in UC1606 Display Data RAM (RAM) is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of page , and system programmers need to set the values of PA and CA explicitly.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (64-CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

Row SCANNING

For each field, the scanning starts at COM1 through COMx, where x depends on the setting of MR.

COM electrode scanning (row scanning) orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of COM1 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display up by SL rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed Row scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

$$Line = SL$$

Otherwise

$$Line = \text{Mod}(Line+1, 64)$$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 64.

Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

$$Line = \text{Mod}(SL + MUX-1, 64)$$

where MUX = 25, 33, 49, or 65.

Otherwise

$$Line = \text{Mod}(Line-1, 64)$$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1606 has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~20mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1606 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1606 has three operating modes (OM): Reset, Normal, Sleep.

| Mode | Reset | Sleep | Normal |
|------------------|--------|--------|--------|
| OM | 00 | 10 | 11 |
| Host Interface | Active | Active | Active |
| Clock | OFF | OFF | ON |
| LCD Drivers | OFF | OFF | ON |
| Charge Pump | OFF | OFF | ON |
| Draining Circuit | ON | OFF | OFF |

Table 5: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0} , C_{B1} , and C_L . To drain these

capacitors, use Reset command to activate the on-chip draining circuit.

| Action | Mode | OM |
|--|--------|----|
| Set Driver Enable to "0" | Sleep | 10 |
| Set Driver Enable to "1" | Normal | 11 |
| Reset command or RST_ pin pulled "L" Power ON Reset | Reset | 00 |

Table 6: OM changes

Even though UC1606 consumes very little energy in Sleep mode (typically 5uA or less), since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1606 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1606 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1606 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 20~30 ms before the CPU starting to issue commands to UC1606. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

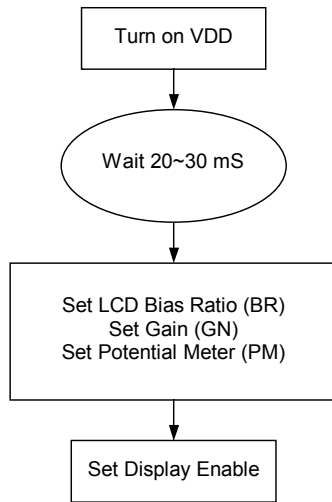


Figure 10: Reference Power-up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+} , C_{BX-} , and C_L from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+} . It is recommended to wait $3 \times RC$ for V_{LCD} and $1.5 \times RC$ for V_{B+} . For example, if C_L is 10nF, then the draining time required for V_{LCD} is 3~5mS.

When internal V_{LCD} is not used, UC1606 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD} .

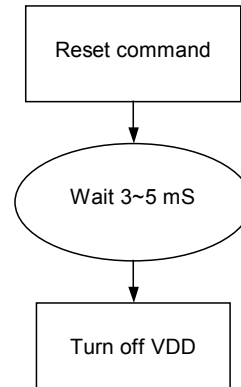


Figure 11: Reference Power-Down Sequence

SAMPLE POWER COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required

Customer: These items are not necessary if customer parameters are the same as default

Advanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

POWER-UP

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|------|-----|-----|----|----|----|----|----|----|----|----|---------------------------|--|
| R | - | - | - | - | - | - | - | - | - | - | Automatic Power-ON Reset. | Wait ~30ms after V_{DD} is ON |
| C | 0 | 0 | 1 | 1 | 0 | 0 | # | # | 0 | # | (16) Set LCD Mapping | Set up LCD specific parameters such as format, MX, MY, MSF, etc. |
| C | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | (19) Set Bias Ratio | |
| R | 0 | 0 | 0 | 0 | 1 | 0 | 0 | # | # | # | (5) Set Gain | |
| R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (10) Set PM | |
| C | 1 | 0 | # | # | # | # | # | # | # | # | Write display RAM | Set up display image |
| . | . | . | . | . | . | . | . | . | . | . | | |
| . | . | . | . | . | . | . | . | . | . | . | | |
| 1 | 0 | # | # | # | # | # | # | # | # | # | | |
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | (15) Set Display Enable | |

POWER-DOWN

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|------|-----|-----|----|----|----|----|----|----|----|----|--------------------|--------------------------------|
| R | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | (17) System Reset | |
| R | - | - | - | - | - | - | - | - | - | - | Draining capacitor | Wait 3~5ms before V_{DD} OFF |

BRIEF DISPLAY-OFF

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|------|-----|-----|----|----|----|----|----|----|----|----|--------------------------|---|
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (15) Set Display Disable | |
| C | 1 | 0 | # | # | # | # | # | # | # | # | Write display RAM | Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.) |
| | . | . | . | . | . | . | . | . | . | . | | |
| | 1 | 0 | # | # | # | # | # | # | # | # | | |
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | (15) Set Display Enable | |

* This is only recommended for very brief display OFF (under 10mS).
 If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action | Comments |
|------|-----|-----|----|----|----|----|----|----|----|----|-------------------------|---|
| R | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | (17) System Reset. | C _{B1} , C _{B1} , C _{LCD} discharged. |
| - | - | - | - | - | - | - | - | - | - | - | | Extended display OFF Z z z z . . . |
| - | - | - | - | - | - | - | - | - | - | - | | System waking up |
| C | 0 | 0 | 1 | 1 | 0 | 0 | # | # | 0 | # | (16) Set LCD Mapping | Set up LCD specific parameters such as format, MX, MY, MSF, etc. |
| C | 1 | 0 | # | # | # | # | # | # | # | # | Write display RAM | Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.) |
| | . | . | . | . | . | . | . | . | . | . | | |
| | 1 | 0 | # | # | # | # | # | # | # | # | | |
| C | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | # | # | (19) Set Bias Ratio | |
| R | 0 | 0 | 0 | 0 | 1 | 0 | 0 | # | # | # | (5) Set Gain | |
| R | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (10) Set PM | |
| | 0 | 0 | # | # | # | # | # | # | # | # | | |
| R | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | (17) Set Display Enable | |

* The sequence is basically the same as the power up sequence, except *Power-ON RESET* is replaced by *System RESET* command, and an extended idle time in between.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|-------------------------------|------|-----------------------|------|
| V _{DD} | Logic Supply voltage | -0.3 | +5.5 | V |
| V _{DD2} | LCD Generator Supply voltage | -0.3 | +5.5 | V |
| V _{DD3} | Analog Circuit Supply voltage | -0.3 | +5.5 | V |
| V _{LCD} | LCD Generated voltage | -0.3 | +15.5 | V |
| V _{IN} | Any Input Voltage | -0.3 | V _{DD} + 0.3 | V |
| T _{OPR} | Operating temperature range | -30 | +85 | °C |
| T _{STR} | Storage temperature | -55 | +125 | °C |

Notes

1. V_{DD} based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS
DC CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------|----------------------------|------------------------------------|-------------|------|-------------|-----------|
| V_{DD} | Supply for digital circuit | | 2.4 | 3.0 | 5.0 | V |
| $V_{DD2/3}$ | Supply for bias & pump | | 2.4 | 3.0 | 5.0 | V |
| V_{LCD} | Charge pump output | $V_{DD2/3} \geq 2.4V, 25^{\circ}C$ | | 9.5 | 13.5 | V |
| V_D | LCD data voltage | $V_{DD2/3} \geq 2.4V, 25^{\circ}C$ | | | 1.2 | V |
| V_{IL} | Input logic LOW | | | | $0.2V_{DD}$ | V |
| V_{IH} | Input logic HIGH | | $0.8V_{DD}$ | | | V |
| V_{OL} | Output logic LOW | | | | $0.2V_{DD}$ | V |
| V_{OH} | Output logic HIGH | | $0.8V_{DD}$ | | | V |
| I_{IL} | Input leakage current | | | | 1.5 | μA |
| $R_{0(SEG)}$ | SEG output impedance | $V_{LCD} = 9V$ | | 3 | 4 | $k\Omega$ |
| $R_{0(COM)}$ | COM output impedance | $V_{LCD} = 9V$ | | 3.5 | 4.5 | $k\Omega$ |
| f_{CLK} | Internal clock frequency | | 183 | 190 | 196 | kHz |

POWER CONSUMPTION

$V_{DD} = 2.8$, Bias Ratio = 9.33, Gain = 1.43, PM = 32, PL = Regular LCD loading, MR = 65, Bus mode = 6800, $C_L = 20nF$, CB = 1 μF . All outputs are open-circuit.

| Display Pattern | Conditions | Typ. (μA) | Max. (μA) |
|-----------------|------------|------------------|------------------|
| All-OFF | Bus = idle | 249 | 600 |
| 2-pixel checker | Bus = idle | 451 | 600 |

AC CHARACTERISTICS

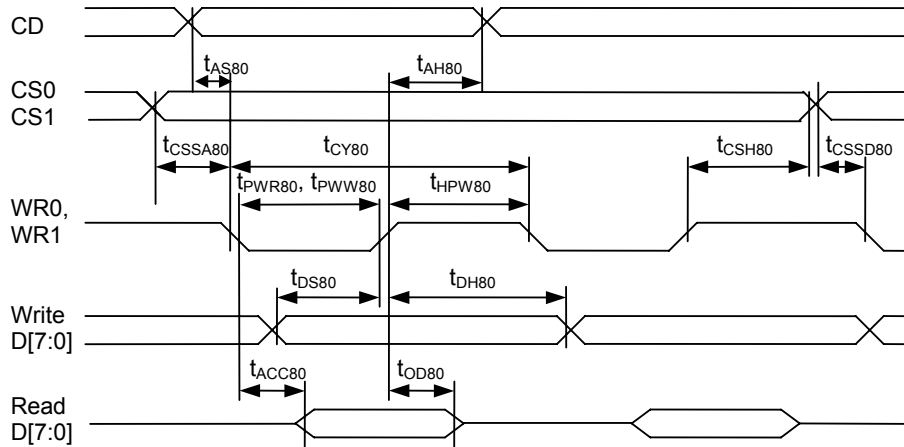


Figure 12: Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|----------|---|---------------|----------------|------------|-------|
| t_{AS80} t_{AH80} | CD | Address setup time Address hold time | | 25 50 | - | ns |
| t_{CY80} | | System cycle time | | 300 | - | ns |
| t_{PWR80} | WR1 | Pulse width (read) | | 85 | - | ns |
| t_{PWW80} | WR0 | Pulse width (write) | | 85 | - | ns |
| t_{HPW80} | WR0, WR1 | High pulse width | | 85 | - | ns |
| t_{DS80} t_{DH80} | D0~D7 | Data setup time Data hold time | | 40 15 | - | ns |
| t_{ACC80} t_{OD80} | | Read access time Output disable time | $C_L = 100pF$ | - 10 | 140 100 | ns |
| t_{CSSA80} t_{CSSD80} t_{CSH80} | CS1/CS0 | Chip select setup time | | 15 15 30 | | ns |

(VDD=3.0V to 4.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---|----------|---|---------------|----------------|----------|-------|
| t_{AS80} t_{AH80} | CD | Address setup time Address hold time | | 20 45 | - | ns |
| t_{CY80} | | System cycle time | | 166 | - | ns |
| t_{PWR80} | WR1 | Pulse width (read) | | 65 | - | ns |
| t_{PWW80} | WR0 | Pulse width (write) | | 65 | - | ns |
| t_{HPW80} | WR0, WR1 | High pulse width | | 65 | - | ns |
| t_{DS80} t_{DH80} | D0~D7 | Data setup time Data hold time | | 30 10 | - | ns |
| t_{ACC80} t_{OD80} | | Read access time Output disable time | $C_L = 100pF$ | - 10 | 65 45 | ns |
| t_{CSSA80} t_{CSSD80} t_{CSH80} | CS1/CS0 | Chip select setup time | | 10 10 20 | | ns |

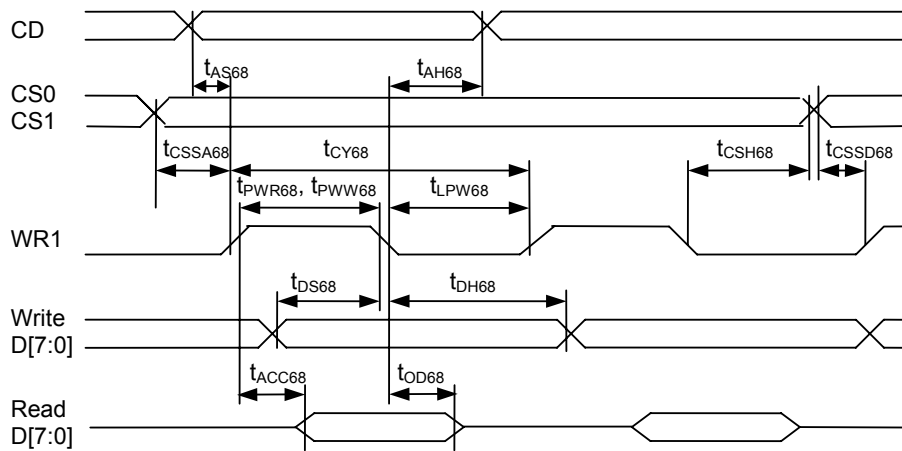


Figure 13: Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---------------------|---------|------------------------|------------------------|------|------|-------|
| t _{AS68} | CD | Address setup time | | 25 | – | ns |
| t _{AH68} | | Address hold time | | 50 | – | ns |
| t _{CY68} | | System cycle time | | 300 | – | ns |
| t _{PWR68} | WR1 | Pulse width (read) | | 85 | – | ns |
| t _{PWW68} | | Pulse width (write) | | 85 | – | ns |
| t _{LPW68} | | Low pulse width | | 85 | – | ns |
| t _{DS68} | D0~D7 | Data setup time | | 40 | – | ns |
| t _{DH68} | | Data hold time | | 15 | – | ns |
| t _{ACC68} | | Read access time | C _L = 100pF | – | 140 | ns |
| t _{OD68} | | Output disable time | | 10 | 100 | ns |
| T _{CSSA68} | CS1/CS0 | Chip select setup time | | 15 | | ns |
| T _{CSSD68} | | | | 15 | | ns |
| T _{CSH68} | | | | 30 | | ns |

(VDD=3.0V to 4.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|---------------------|---------|------------------------|------------------------|------|------|-------|
| t _{AS68} | CD | Address setup time | | 20 | – | ns |
| t _{AH68} | | Address hold time | | 45 | – | ns |
| t _{CY68} | | System cycle time | | 166 | – | ns |
| t _{PWR68} | WR1 | Pulse width (read) | | 65 | – | ns |
| t _{PWW68} | | Pulse width (write) | | 65 | – | ns |
| t _{LPW68} | | Low pulse width | | 65 | – | ns |
| t _{DS68} | D0~D7 | Data setup time | | 30 | – | ns |
| t _{DH68} | | Data hold time | | 10 | – | ns |
| t _{ACC68} | | Read access time | C _L = 100pF | – | 70 | ns |
| t _{OD68} | | Output disable time | | 10 | 50 | ns |
| T _{CSSA68} | CS1/CS0 | Chip select setup time | | 10 | | ns |
| T _{CSSD68} | | | | 10 | | ns |
| T _{CSH68} | | | | 20 | | ns |

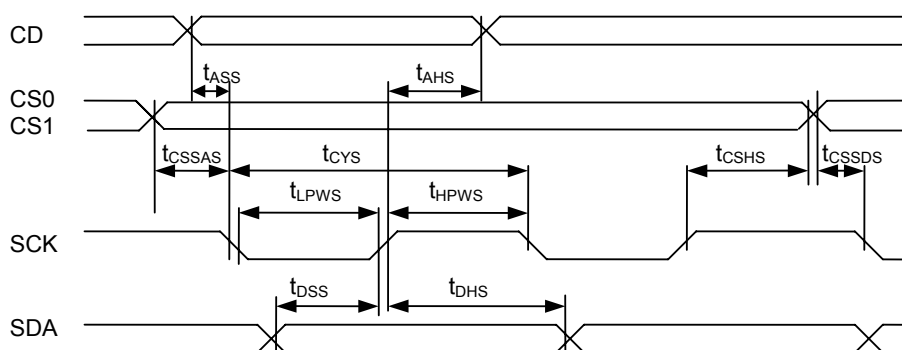


Figure 14: Serial Bus Timing Characteristics

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|-------------|---------|------------------------|-----------|------|------|-------|
| t_{ASS} | CD | Address setup time | | 15 | – | ns |
| t_{AHS} | | Address hold time | | 40 | – | ns |
| t_{CYS} | SCK | System cycle time | | 250 | – | ns |
| t_{LPWS} | | Low pulse width | | 100 | – | ns |
| t_{HPWS} | | High pulse width | | 100 | – | ns |
| t_{DSS} | SDA | Data setup time | | 90 | – | ns |
| t_{DHS} | | Data hold time | | 90 | – | ns |
| t_{CSSAS} | CS1/CS0 | Chip select setup time | | 10 | | ns |
| t_{CSSDS} | | | | 10 | | |
| t_{CSHS} | | | | 150 | | |

(VDD=3.0V to 4.0V, Ta= -30 to +85°C)

| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|-------------|---------|------------------------|-----------|------|------|-------|
| t_{ASS} | CD | Address setup time | | 10 | – | ns |
| t_{AHS} | | Address hold time | | 20 | – | ns |
| t_{CYS} | SCK | System cycle time | | 200 | – | ns |
| t_{LPWS} | | Low pulse width | | 75 | – | ns |
| t_{HPWS} | | High pulse width | | 75 | – | ns |
| t_{DSS} | SDA | Data setup time | | 50 | – | ns |
| t_{DHS} | | Data hold time | | 50 | – | ns |
| t_{CSSAS} | CS1/CS0 | Chip select setup time | | 10 | | ns |
| t_{CSSDS} | | | | 10 | | |
| t_{CSHS} | | | | 100 | | |

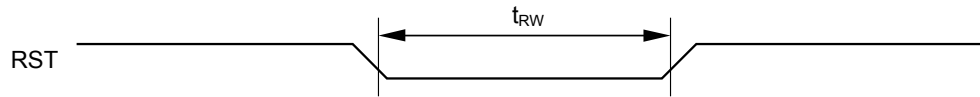


Figure 15: Reset Characteristics

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

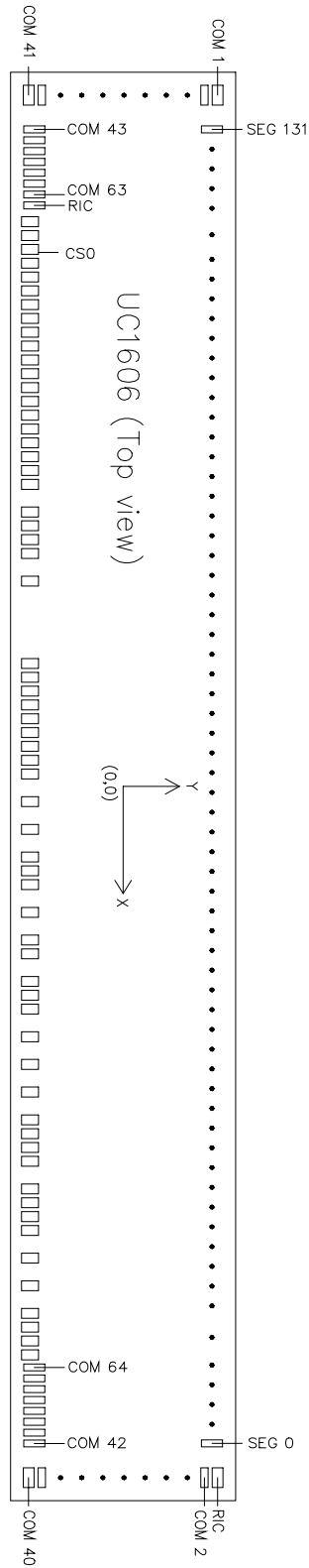
| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|----------|--------|-----------------------|-----------|------|------|-------|
| t_{RW} | RST | Reset low pulse width | | 240 | – | ns |

(VDD=3.0V to 4.0V, Ta= -30 to +85°C)

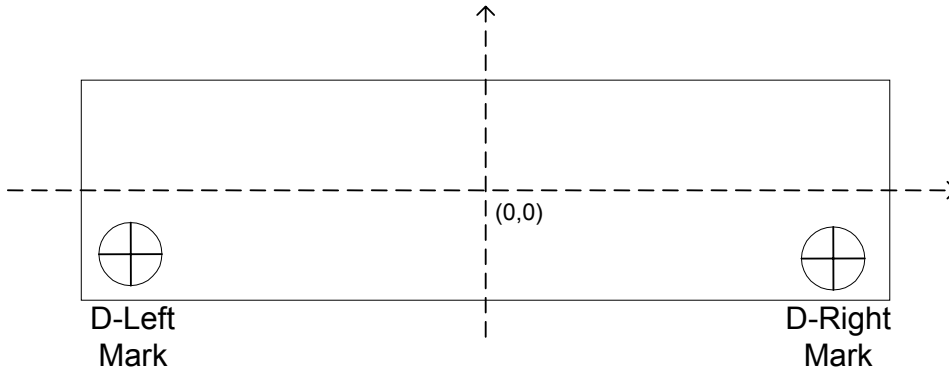
| Symbol | Signal | Description | Condition | Min. | Max. | Units |
|----------|--------|-----------------------|-----------|------|------|-------|
| t_{RW} | RST | Reset low pulse width | | 200 | – | ns |

PHYSICAL DIMENSIONS

| |
|--|
| <p>DIE SIZE: 9.862 mm x 1.647 mm</p> <p>DIE THICKNESS: 0.625mm</p> <p>BUMP HEIGHT: 17µm ±1µm (within die)</p> <p>AU BUMP SIZE: 86 x 46µm² (Typ.) 66 x 49µm² (Typ.)</p> <p>MINIMUM BUMP PITCH: 70µm (Typ.)</p> <p>MINIMUM BUMP GAP: 24µm (Typ.)</p> <p>COORDINATE ORIGIN: Chip center</p> <p>PAD REFERENCE: Pad center</p> <p>(Drawings and coordinates are in the circuit/bump view)</p> |
|--|



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

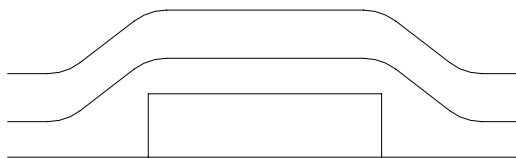
COORDINATES:

| D-Left Mark Center | | D-Right Mark Center | |
|--------------------|--------|---------------------|--------|
| X | Y | X | Y |
| -4610.0 | -430.7 | 4610.0 | -430.7 |

SIZE:

R: 18.0 μm ; r: 9.0 μm

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

| # | Name | X | Y | W | H |
|----|-------|-------|------|----|----|
| 1 | COM1 | -4813 | 698 | 86 | 46 |
| 2 | COM3 | -4813 | 628 | 86 | 46 |
| 3 | COM5 | -4813 | 558 | 86 | 46 |
| 4 | COM7 | -4813 | 488 | 86 | 46 |
| 5 | COM9 | -4813 | 418 | 86 | 46 |
| 6 | COM11 | -4813 | 348 | 86 | 46 |
| 7 | COM13 | -4813 | 278 | 86 | 46 |
| 8 | COM15 | -4813 | 208 | 86 | 46 |
| 9 | COM17 | -4813 | 138 | 86 | 46 |
| 10 | COM19 | -4813 | 68 | 86 | 46 |
| 11 | COM21 | -4813 | -2 | 86 | 46 |
| 12 | COM23 | -4813 | -72 | 86 | 46 |
| 13 | COM25 | -4813 | -142 | 86 | 46 |
| 14 | COM27 | -4813 | -212 | 86 | 46 |
| 15 | COM29 | -4813 | -282 | 86 | 46 |
| 16 | COM31 | -4813 | -352 | 86 | 46 |
| 17 | COM33 | -4813 | -422 | 86 | 46 |
| 18 | COM35 | -4813 | -492 | 86 | 46 |
| 19 | COM37 | -4813 | -562 | 86 | 46 |
| 20 | COM39 | -4813 | -632 | 86 | 46 |
| 21 | COM41 | -4813 | -702 | 86 | 46 |
| 22 | COM43 | -4612 | -706 | 46 | 86 |
| 23 | COM45 | -4542 | -706 | 46 | 86 |
| 24 | COM47 | -4472 | -706 | 46 | 86 |
| 25 | COM49 | -4402 | -706 | 46 | 86 |
| 26 | COM51 | -4332 | -706 | 46 | 86 |
| 27 | COM53 | -4262 | -706 | 46 | 86 |
| 28 | COM55 | -4192 | -706 | 46 | 86 |
| 29 | COM57 | -4122 | -706 | 46 | 86 |
| 30 | COM59 | -4052 | -706 | 46 | 86 |
| 31 | COM61 | -3982 | -706 | 46 | 86 |
| 32 | COM63 | -3912 | -706 | 46 | 86 |
| 33 | CIC | -3842 | -706 | 46 | 86 |
| 34 | NC | -3764 | -706 | 46 | 86 |
| 35 | EO | -3694 | -706 | 46 | 86 |
| 36 | VDDX | -3624 | -706 | 46 | 86 |
| 37 | CS0 | -3554 | -706 | 46 | 86 |
| 38 | CS1 | -3484 | -706 | 46 | 86 |
| 39 | TST4 | -3414 | -706 | 46 | 86 |
| 40 | RST | -3344 | -706 | 46 | 86 |
| 41 | CD | -3274 | -706 | 46 | 86 |
| 42 | WR0 | -3204 | -706 | 46 | 86 |
| 43 | WR1 | -3134 | -706 | 46 | 86 |
| 44 | D0 | -3064 | -706 | 46 | 86 |
| 45 | D1 | -2994 | -706 | 46 | 86 |
| 46 | D2 | -2924 | -706 | 46 | 86 |
| 47 | D3 | -2854 | -706 | 46 | 86 |
| 48 | D4 | -2784 | -706 | 46 | 86 |
| 49 | D5 | -2714 | -706 | 46 | 86 |

| # | Name | X | Y | W | H |
|----|------|-------|------|----|----|
| 50 | D6 | -2644 | -706 | 46 | 86 |
| 51 | D7 | -2574 | -706 | 46 | 86 |
| 52 | VDD | -2394 | -723 | 86 | 46 |
| 53 | VDD | -2287 | -723 | 86 | 46 |
| 54 | VDD | -2180 | -723 | 86 | 46 |
| 55 | VDD | -2074 | -723 | 86 | 46 |
| 56 | VDD | -1967 | -723 | 86 | 46 |
| 57 | VDD2 | -1769 | -723 | 86 | 46 |
| 58 | VDD2 | -1663 | -723 | 86 | 46 |
| 59 | VDD2 | -1556 | -723 | 86 | 46 |
| 60 | VDD2 | -1449 | -723 | 86 | 46 |
| 61 | VDD3 | -1343 | -723 | 86 | 46 |
| 62 | VSS | -1054 | -723 | 86 | 46 |
| 63 | VSS | -947 | -723 | 86 | 46 |
| 64 | VSS | -841 | -723 | 86 | 46 |
| 65 | VSS | -734 | -723 | 86 | 46 |
| 66 | VSS | -627 | -723 | 86 | 46 |
| 67 | VSS2 | -430 | -723 | 86 | 46 |
| 68 | VSS2 | -323 | -723 | 86 | 46 |
| 69 | VSS2 | -216 | -723 | 86 | 46 |
| 70 | VSS2 | -110 | -723 | 86 | 46 |
| 71 | VB1+ | 125 | -723 | 86 | 46 |
| 72 | VB1+ | 231 | -723 | 86 | 46 |
| 73 | VB1+ | 338 | -723 | 86 | 46 |
| 74 | TP3 | 436 | -724 | 66 | 49 |
| 75 | TP2 | 526 | -724 | 66 | 49 |
| 76 | TP1 | 616 | -724 | 66 | 49 |
| 77 | PS0 | 764 | -706 | 46 | 86 |
| 78 | PS1 | 904 | -706 | 46 | 86 |
| 79 | VDDX | 974 | -706 | 46 | 86 |
| 80 | MR0 | 1114 | -706 | 46 | 86 |
| 81 | MR1 | 1254 | -706 | 46 | 86 |
| 82 | VB1- | 1394 | -706 | 46 | 86 |
| 83 | VB1- | 1464 | -706 | 46 | 86 |
| 84 | VB1- | 1534 | -706 | 46 | 86 |
| 85 | VB1- | 1604 | -706 | 46 | 86 |
| 86 | VB0- | 1744 | -706 | 46 | 86 |
| 87 | VB0- | 1814 | -706 | 46 | 86 |
| 88 | VB0- | 1884 | -706 | 46 | 86 |
| 89 | VB0- | 1954 | -706 | 46 | 86 |
| 90 | BR0 | 2094 | -706 | 46 | 86 |
| 91 | BR1 | 2234 | -706 | 46 | 86 |
| 92 | VDDX | 2304 | -706 | 46 | 86 |
| 93 | TC0 | 2444 | -706 | 46 | 86 |
| 94 | TC1 | 2584 | -706 | 46 | 86 |
| 95 | VB0+ | 2724 | -706 | 46 | 86 |
| 96 | VB0+ | 2794 | -706 | 46 | 86 |
| 97 | VB0+ | 2864 | -706 | 46 | 86 |
| 98 | VB0+ | 2934 | -706 | 46 | 86 |

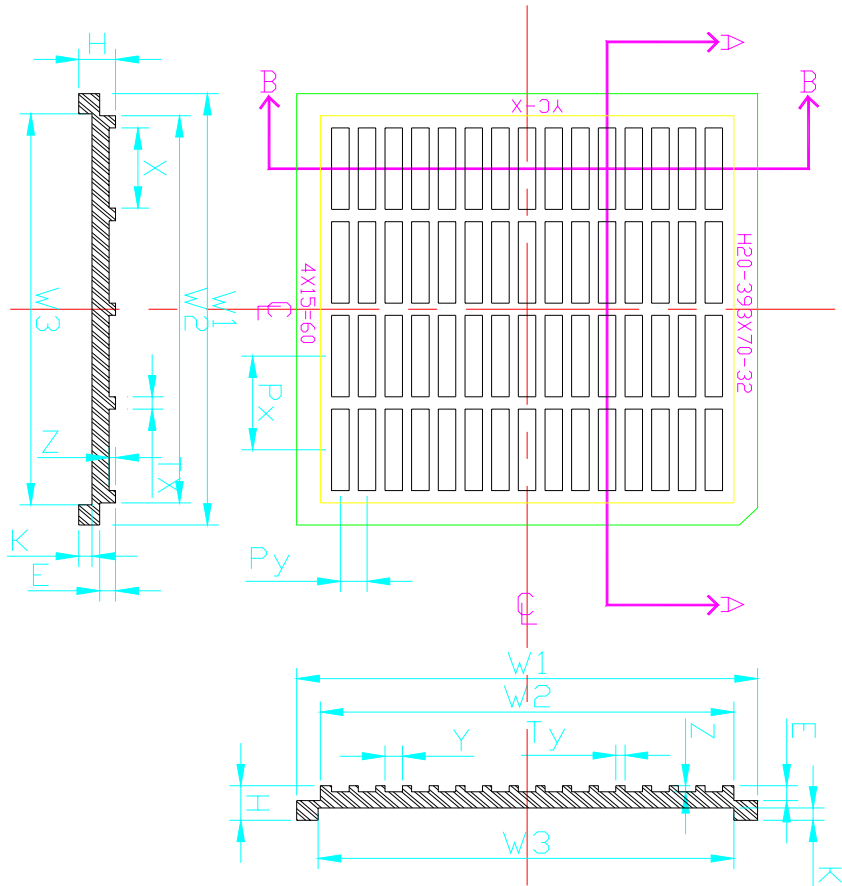
| # | Name | X | Y | W | H |
|-----|---------|------|------|----|----|
| 99 | TST1 | 3074 | -706 | 46 | 86 |
| 100 | TST2 | 3144 | -706 | 46 | 86 |
| 101 | TST3 | 3214 | -706 | 46 | 86 |
| 102 | VLCDIN | 3354 | -706 | 46 | 86 |
| 103 | VLCDOUT | 3424 | -706 | 46 | 86 |
| 104 | VLCDIN | 3494 | -706 | 46 | 86 |
| 105 | VLCDOUT | 3634 | -706 | 46 | 86 |
| 106 | VDD2 | 3704 | -706 | 46 | 86 |
| 107 | VDD2 | 3774 | -706 | 46 | 86 |
| 108 | COM64 | 3844 | -706 | 46 | 86 |
| 109 | COM62 | 3914 | -706 | 46 | 86 |
| 110 | COM60 | 3984 | -706 | 46 | 86 |
| 111 | COM58 | 4054 | -706 | 46 | 86 |
| 112 | COM56 | 4124 | -706 | 46 | 86 |
| 113 | COM54 | 4194 | -706 | 46 | 86 |
| 114 | COM52 | 4264 | -706 | 46 | 86 |
| 115 | COM50 | 4334 | -706 | 46 | 86 |
| 116 | COM48 | 4404 | -706 | 46 | 86 |
| 117 | COM46 | 4474 | -706 | 46 | 86 |
| 118 | COM44 | 4544 | -706 | 46 | 86 |
| 119 | COM42 | 4614 | -706 | 46 | 86 |
| 120 | COM40 | 4813 | -702 | 86 | 46 |
| 121 | COM38 | 4813 | -632 | 86 | 46 |
| 122 | COM36 | 4813 | -562 | 86 | 46 |
| 123 | COM34 | 4813 | -492 | 86 | 46 |
| 124 | COM46 | 4813 | -422 | 86 | 46 |
| 125 | COM30 | 4813 | -352 | 86 | 46 |
| 126 | COM28 | 4813 | -282 | 86 | 46 |
| 127 | COM26 | 4813 | -212 | 86 | 46 |
| 128 | COM24 | 4813 | -142 | 86 | 46 |
| 129 | COM22 | 4813 | -72 | 86 | 46 |
| 130 | COM20 | 4813 | -2 | 86 | 46 |
| 131 | COM18 | 4813 | 68 | 86 | 46 |
| 132 | COM16 | 4813 | 138 | 86 | 46 |
| 133 | COM14 | 4813 | 208 | 86 | 46 |
| 134 | COM12 | 4813 | 278 | 86 | 46 |
| 135 | COM10 | 4813 | 348 | 86 | 46 |
| 136 | COM8 | 4813 | 418 | 86 | 46 |
| 137 | COM6 | 4813 | 488 | 86 | 46 |
| 138 | COM4 | 4813 | 558 | 86 | 46 |
| 139 | COM2 | 4813 | 628 | 86 | 46 |
| 140 | CIC | 4813 | 698 | 86 | 46 |
| 141 | SEG1 | 4585 | 706 | 46 | 86 |
| 142 | SEG2 | 4515 | 706 | 46 | 86 |
| 143 | SEG3 | 4445 | 706 | 46 | 86 |
| 144 | SEG4 | 4375 | 706 | 46 | 86 |
| 145 | SEG5 | 4305 | 706 | 46 | 86 |
| 146 | SEG6 | 4235 | 706 | 46 | 86 |
| 147 | SEG7 | 4165 | 706 | 46 | 86 |
| 148 | SEG8 | 4095 | 706 | 46 | 86 |
| 149 | SEG9 | 4025 | 706 | 46 | 86 |

| # | Name | X | Y | W | H |
|-----|-------|------|-----|----|----|
| 150 | SEG10 | 3955 | 706 | 46 | 86 |
| 151 | SEG11 | 3885 | 706 | 46 | 86 |
| 152 | SEG12 | 3815 | 706 | 46 | 86 |
| 153 | SEG13 | 3745 | 706 | 46 | 86 |
| 154 | SEG14 | 3675 | 706 | 46 | 86 |
| 155 | SEG15 | 3605 | 706 | 46 | 86 |
| 156 | SEG16 | 3535 | 706 | 46 | 86 |
| 157 | SEG17 | 3465 | 706 | 46 | 86 |
| 158 | SEG18 | 3395 | 706 | 46 | 86 |
| 159 | SEG19 | 3325 | 706 | 46 | 86 |
| 160 | SEG20 | 3255 | 706 | 46 | 86 |
| 161 | SEG21 | 3185 | 706 | 46 | 86 |
| 162 | SEG22 | 3115 | 706 | 46 | 86 |
| 163 | SEG23 | 3045 | 706 | 46 | 86 |
| 164 | SEG24 | 2975 | 706 | 46 | 86 |
| 165 | SEG25 | 2905 | 706 | 46 | 86 |
| 166 | SEG26 | 2835 | 706 | 46 | 86 |
| 167 | SEG27 | 2765 | 706 | 46 | 86 |
| 168 | SEG28 | 2695 | 706 | 46 | 86 |
| 169 | SEG29 | 2625 | 706 | 46 | 86 |
| 170 | SEG30 | 2555 | 706 | 46 | 86 |
| 171 | SEG31 | 2485 | 706 | 46 | 86 |
| 172 | SEG32 | 2415 | 706 | 46 | 86 |
| 173 | SEG33 | 2345 | 706 | 46 | 86 |
| 174 | SEG34 | 2275 | 706 | 46 | 86 |
| 175 | SEG35 | 2205 | 706 | 46 | 86 |
| 176 | SEG36 | 2135 | 706 | 46 | 86 |
| 177 | SEG37 | 2065 | 706 | 46 | 86 |
| 178 | SEG38 | 1995 | 706 | 46 | 86 |
| 179 | SEG39 | 1925 | 706 | 46 | 86 |
| 180 | SEG40 | 1855 | 706 | 46 | 86 |
| 181 | SEG41 | 1785 | 706 | 46 | 86 |
| 182 | SEG42 | 1715 | 706 | 46 | 86 |
| 183 | SEG43 | 1645 | 706 | 46 | 86 |
| 184 | SEG44 | 1575 | 706 | 46 | 86 |
| 185 | SEG45 | 1505 | 706 | 46 | 86 |
| 186 | SEG46 | 1435 | 706 | 46 | 86 |
| 187 | SEG47 | 1365 | 706 | 46 | 86 |
| 188 | SEG48 | 1295 | 706 | 46 | 86 |
| 189 | SEG49 | 1225 | 706 | 46 | 86 |
| 190 | SEG50 | 1155 | 706 | 46 | 86 |
| 191 | SEG51 | 1085 | 706 | 46 | 86 |
| 192 | SEG52 | 1015 | 706 | 46 | 86 |
| 193 | SEG53 | 945 | 706 | 46 | 86 |
| 194 | SEG54 | 875 | 706 | 46 | 86 |
| 195 | SEG55 | 805 | 706 | 46 | 86 |
| 196 | SEG56 | 735 | 706 | 46 | 86 |
| 197 | SEG57 | 665 | 706 | 46 | 86 |
| 198 | SEG58 | 595 | 706 | 46 | 86 |
| 199 | SEG59 | 525 | 706 | 46 | 86 |
| 200 | SEG60 | 455 | 706 | 46 | 86 |

| # | Name | X | Y | W | H |
|-----|--------|-------|-----|----|----|
| 201 | SEG61 | 385 | 706 | 46 | 86 |
| 202 | SEG62 | 315 | 706 | 46 | 86 |
| 203 | SEG63 | 245 | 706 | 46 | 86 |
| 204 | SEG64 | 175 | 706 | 46 | 86 |
| 205 | SEG65 | 105 | 706 | 46 | 86 |
| 206 | SEG66 | 35 | 706 | 46 | 86 |
| 207 | SEG67 | -35 | 706 | 46 | 86 |
| 208 | SEG68 | -105 | 706 | 46 | 86 |
| 209 | SEG69 | -175 | 706 | 46 | 86 |
| 210 | SEG70 | -245 | 706 | 46 | 86 |
| 211 | SEG71 | -315 | 706 | 46 | 86 |
| 212 | SEG72 | -385 | 706 | 46 | 86 |
| 213 | SEG73 | -455 | 706 | 46 | 86 |
| 214 | SEG74 | -525 | 706 | 46 | 86 |
| 215 | SEG75 | -595 | 706 | 46 | 86 |
| 216 | SEG76 | -665 | 706 | 46 | 86 |
| 217 | SEG77 | -735 | 706 | 46 | 86 |
| 218 | SEG78 | -805 | 706 | 46 | 86 |
| 219 | SEG79 | -875 | 706 | 46 | 86 |
| 220 | SEG80 | -945 | 706 | 46 | 86 |
| 221 | SEG81 | -1015 | 706 | 46 | 86 |
| 222 | SEG82 | -1085 | 706 | 46 | 86 |
| 223 | SEG83 | -1155 | 706 | 46 | 86 |
| 224 | SEG84 | -1225 | 706 | 46 | 86 |
| 225 | SEG85 | -1295 | 706 | 46 | 86 |
| 226 | SEG86 | -1365 | 706 | 46 | 86 |
| 227 | SEG87 | -1435 | 706 | 46 | 86 |
| 228 | SEG88 | -1505 | 706 | 46 | 86 |
| 229 | SEG89 | -1575 | 706 | 46 | 86 |
| 230 | SEG90 | -1645 | 706 | 46 | 86 |
| 231 | SEG91 | -1715 | 706 | 46 | 86 |
| 232 | SEG92 | -1785 | 706 | 46 | 86 |
| 233 | SEG93 | -1855 | 706 | 46 | 86 |
| 234 | SEG94 | -1925 | 706 | 46 | 86 |
| 235 | SEG95 | -1995 | 706 | 46 | 86 |
| 236 | SEG96 | -2065 | 706 | 46 | 86 |
| 237 | SEG97 | -2135 | 706 | 46 | 86 |
| 238 | SEG98 | -2205 | 706 | 46 | 86 |
| 239 | SEG99 | -2275 | 706 | 46 | 86 |
| 240 | SEG100 | -2345 | 706 | 46 | 86 |
| 241 | SEG101 | -2415 | 706 | 46 | 86 |
| 242 | SEG102 | -2485 | 706 | 46 | 86 |
| 243 | SEG103 | -2555 | 706 | 46 | 86 |
| 244 | SEG104 | -2625 | 706 | 46 | 86 |
| 245 | SEG105 | -2695 | 706 | 46 | 86 |
| 246 | SEG106 | -2765 | 706 | 46 | 86 |
| 247 | SEG107 | -2835 | 706 | 46 | 86 |
| 248 | SEG108 | -2905 | 706 | 46 | 86 |
| 249 | SEG109 | -2975 | 706 | 46 | 86 |
| 250 | SEG110 | -3045 | 706 | 46 | 86 |
| 251 | SEG111 | -3115 | 706 | 46 | 86 |

| # | Name | X | Y | W | H |
|-----|--------|-------|-----|----|----|
| 252 | SEG112 | -3185 | 706 | 46 | 86 |
| 253 | SEG113 | -3255 | 706 | 46 | 86 |
| 254 | SEG114 | -3325 | 706 | 46 | 86 |
| 255 | SEG115 | -3395 | 706 | 46 | 86 |
| 256 | SEG116 | -3465 | 706 | 46 | 86 |
| 257 | SEG117 | -3535 | 706 | 46 | 86 |
| 258 | SEG118 | -3605 | 706 | 46 | 86 |
| 259 | SEG119 | -3675 | 706 | 46 | 86 |
| 260 | SEG120 | -3745 | 706 | 46 | 86 |
| 261 | SEG121 | -3815 | 706 | 46 | 86 |
| 262 | SEG122 | -3885 | 706 | 46 | 86 |
| 263 | SEG123 | -3955 | 706 | 46 | 86 |
| 264 | SEG124 | -4025 | 706 | 46 | 86 |
| 265 | SEG125 | -4095 | 706 | 46 | 86 |
| 266 | SEG126 | -4165 | 706 | 46 | 86 |
| 267 | SEG127 | -4235 | 706 | 46 | 86 |
| 268 | SEG128 | -4305 | 706 | 46 | 86 |
| 269 | SEG129 | -4375 | 706 | 46 | 86 |
| 270 | SEG130 | -4445 | 706 | 46 | 86 |
| 271 | SEG131 | -4515 | 706 | 46 | 86 |
| 272 | SEG132 | -4585 | 706 | 46 | 86 |

TRAY INFORMATION



Remark:
 1. UC1606 Die Size : 9.862*1.647*0.635mm³ (after wafer sawing, include scribe line dimension)
 2. Surface resistivity: $1 * 10^5 \sim 10^6 \Omega / \text{cm}^2$

SECTION B-B

| | Spec |
|----|------------------|
| | mm (mil) |
| W1 | 50.70±0.2 (1996) |
| W2 | 45.50±0.2 (1791) |
| W3 | 45.95±0.2 (1809) |
| H | 4.05±0.2 (160) |
| E | 1.75±0.2 (69) |
| K | 1.45±0.2 (57) |
| Tx | 1.10±0.05 (43) |
| Ty | 1.17±0.05 (46) |
| Px | 11.1±0.05 (437) |
| Py | 2.95±0.05 (116) |
| X | 10.0±0.1 (393) |
| Y | 1.78±0.1 (70) |
| Z | 0.81±0.1 (32) |
| N | 60 |

| | | | | | | | |
|----------------------------|--------------------|-----------------|-----------|------------------------|-------------|----------|--------|
| Unless Otherwise Specified | | Scale | | N/A | | Proj. | |
| Unit | mm | Package Code | | | | | |
| General Roughness | N/A | ULTRA CHIP INC. | | 品名半導體 | | | |
| Tolerance | | UC1606 IC Tray | | Type:H20-393*70-32(60) | | Material | |
| Dimension | see drawing detail | Drawn | Checked | Approved | Drawing No | Rev. | |
| Angle | N/A | By | Iris Chen | Alvin Chang | Alvin Chang | Sheet | 1 of 1 |
| | | Date | 07-04-02 | 07-04-02 | 07-04-02 | Size | A4 |

REVISION HISTORY

| Version | Contents | Date of Rev. |
|---|--|---------------|
| 1.0 | First release | Jul. 06, 2001 |
| 1.1 | Frame rate increased, AC/DC Characteristics update, Product naming rule added | Oct. 30, 2001 |
| 1.2 | Operation Voltage up to 5.0V | Dec. 18, 2001 |
| 1.3 | Over All revision | Aug. 16, 2002 |
| | (1) Recommended C_L value is adjusted to 5nF ~ 20nF (Page 5) | |
| | (2) VDD1 is renamed to VDD (Page 5) | |
| | (3) TP3 is renamed to TST4 (Page 7) | |
| | (4) TP[2:0] is renamed to TP[3:1] (Page 7) | |
| | (5) C[0:131] is renamed to SEG[1:132] (Page 7) | |
| | (6) R[1~64] is renamed to COM[1~64] (Page 7) | |
| | (7) RIC is renamed to CIC (Page 7) | |
| | (8) Application circuits are added. (Page 18, 23, 24) | |
| | (9) Alignment Mark Information is presented (Page 39) | |
| | (10) Tray Information is presented. (Page 43) | |
| (11) Power Consumption table is presented (Page 33) | | |
| 1.31 | (1) The direction on dealing with unused bus pins is corrected as leaving open-circuit; instead of connecting to V_{DD}/V_{SS} . (Section "Pin Description", page 6; "Host Interface", page 21.) | Jun. 18, 2003 |
| | (2) Figures 8 and 9, reference circuit for S8/S9, are corrected to present SDA=D2, instead of D3. (Section "Host interface reference circuit", Page 24) | |
| | (3) "Power Consumption" table is filled with data. (Section "Specifications", Page 33) | |
| | (4) Figures 12, 13 and 14 are patched by adding pulse CS1. (Section "AC Characteristics", Pp 33-35) | |

| Version | Contents | Date of Rev. |
|---------|---|---------------|
| 1.32 | (1) Section "Table of Revision History" is renamed as "Revision History" and moved to the rear of the datasheet. | Sep. 24, 2003 |
| | (2) Recommended CB value has been modified: ~ 100x → 150 ~ 250x (Section "Pin Description", page 4) | |
| | (3) In the "Bits" column, number of bit is updated from "PIN" to "2" (Section "Control Registers" – "MR" entry, page 7) | |
| | (4) In the "Default" column, the default values are updated: "00H" → "0H" (Section "Control Registers" – entries "DC", "AC", and "LC", page 8) | |
| | (5) In the "Default value" column, the default value is updated: "0011b" → "011b" (Section "Command Table" – (5) Set Gain, page 9) | |
| | (6) Description of PC[2:1] is modified: 00b: 4x → 01b: 4x (Section "Control Register", page 9; "Command Description", page 11) | |
| | (7) The description for MX is updated: MX: Status of register LC[1] → LC[2] (Section "Command Description" – (3) Get Status, page 10) | |
| | (8) In the Action column, pin specifying is updated: Set APC[1:0] → APC[0] (Section "Command Description" – (7) Set Advance Product Configuration, page 11) | |
| | (9) The value of pins D[7:4] is corrected: 0110 → 1011 (Section "Command Description" – (9) Set Page Address, page 11) | |
| | (10) The values of WR0/WR1 of SPI(S8)/SPI(S9) are updated: "-" → "0" (Section "Host Interface" - Table 4, page 20) | |
| | (11) Figure 6/7: 8080/8bit and 6800/8bit parallel mode reference circuit is modified by showing RST pin. Figure 8/9: Serial-8/9 serial mode reference circuit is modified as following: SDA(D3) → SDA(D2) (Section "Host interface reference circuit", Pp 22 - 23) | |
| | (12) Power consumption table is added. (Section "Specifications", page 32) | |
| | (13) Die Size is updated. (Section "Physical Dimensions", page 37) | |
| | (14) Alignment Mark Information is updated. (Section "Alignment Mark Dimension", page 38) | |