Modulation PLL for GSM, DCS and PCS Systems

Description

The U2896B is a monolithic integrated circuit. It is realized using TEMIC's advanced silicon bipolar UHF5S technology. The device integrates a mixer, an I/Q modulator, a phase-frequency detector (PFD) with two synchronous programmable dividers, and a charge pump. The U2896B is designed for cellular phones such as GSM900, DCS1800, and PCS1900, applying a transmitter architecture at which the VCO operates at the TX output frequency. No duplexer is needed since the out-of-band noise is very low. The U2896B exhibits low power consumption. Broadband operation gives high flexibility for multi-band frequency mappings. The IC is available in a shrinked small-outline 36-pin package (SSO36).

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Supply voltage range 2.7 V to 5.5 V
- Current consumption 50 mA
- Power-down functions
- High-speed PFD and charge pump (CP)
- Small CP saturation voltages (0.5/0.6 V)
- Programmable dividers and CP polarity
- Low-current standby mode

Benefits

- Novel TX architecture saves filter costs
- Extended battery operating time without duplexer
- Less board space (few external components)
- VCO control without voltage doubler
- Small SSO36 package
- One device for all GSM bands

Block Diagram

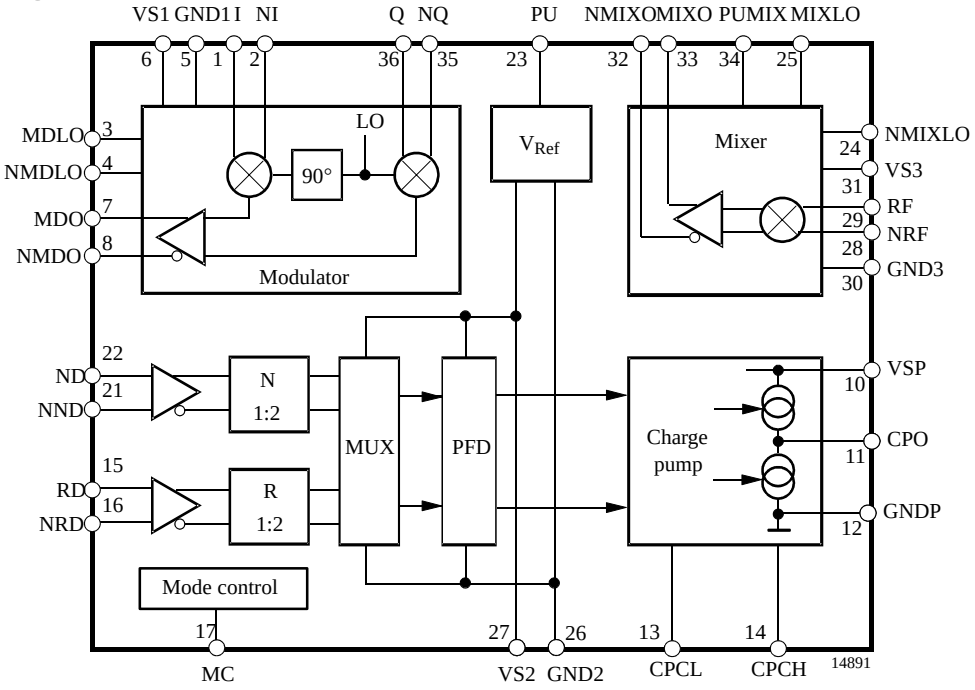


Figure 1. Block diagram

Preliminary Information

Ordering Information

Extended Type Number	Package	Remarks
U2896B-MFCG3	SSO36	Taped and reeled

Pin Description

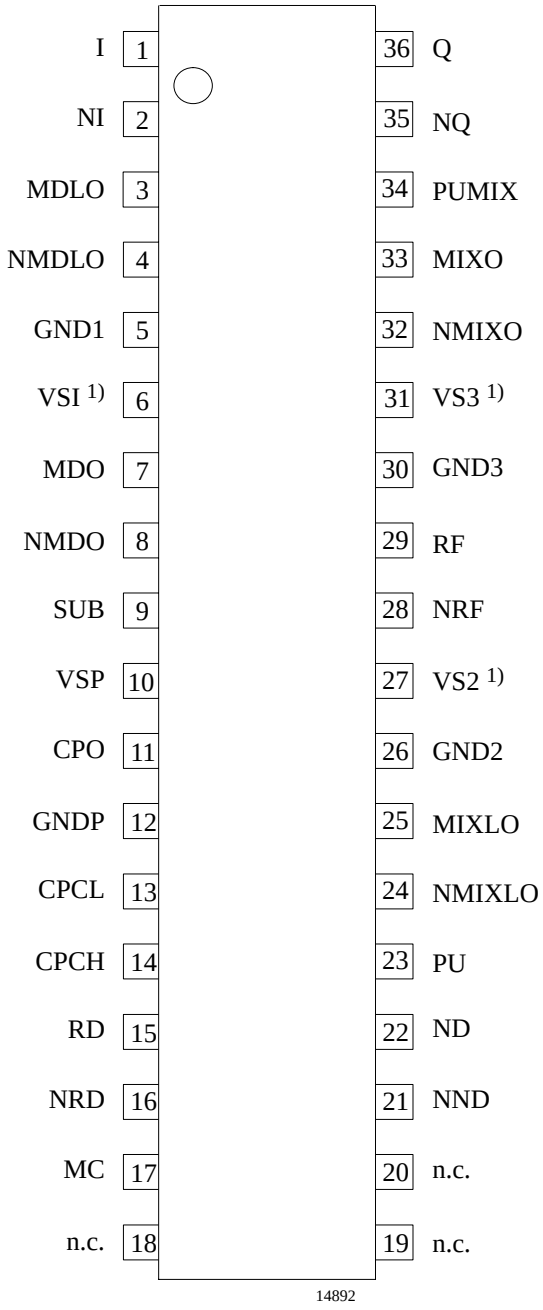


Figure 2. Pinning

Pin	Symbol	Function
1	I	In-phase base band-input
2	NI	Complementary to I
3	MDLO	I/Q-modulator LO input
4	NMDLO	Complementary to MDLO
5	GND1	Ground
6	VS1 1)	Supply I/Q modulator
7	MDO	I/Q modulator
8	NMDO	Complementary to MDO
9	SUB	Substrate, connected to GND
10	VSP	Supply charge pump
11	CPO	Charge pump output
12	GNDP	Ground
13	CPCL	Charge pump current control GSM1800
14	CPCH	Charge pump current control GSM900
15	RD	R-divider input
16	NRD	Complementary to RD
17	MC	Mode control
18	n.c.	Not connected
19	n.c.	Not connected
20	n.c.	Not connected
21	NND	Complementary to ND
22	ND	N-divider input
23	PU	Power-up. whole chip, except mixer
24	NMIXLO	Complementary to MIXLO
25	MIXLO	Mixer LO input
26	GND2	Ground
27	VS2 1)	Supply (MISC)
28	NRF	Complementary to RF
29	RF	Mixer RF input
30	GND3	Ground
31	VS3 1)	Supply mixer
32	NMIXO	Complementary to MIXO
33	MIXO	Mixer output
34	PUMIX	Power-up mixer
35	NQ	Complementary to Q
36	Q	Quad-phase base-band input

1) Between the Pins VS1, VS2 and VS3 the allowed maximum voltage is ≤ 200 mV

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage VS1, VS2, VS3	$V_{VS\#}$	$\leq V_{VSP}$	V
Supply voltage charge pump VSP	V_{VSP}	5.5	V
Voltage at any input	$V_{Vi\#}$	$-0.5 \leq V_{Vi\#} \leq V_{VS\#} +5.5$	V
Current at any input / output pin except CPC	$\mid I_{I\#} \mid \quad \mid I_{O\#} \mid$	2	mA
CPC output currents	$\mid I_{CPC} \mid$	5	mA
Ambient temperature	T_{amb}	–20 to +85	°C
Storage temperature	T_{stg}	–40 to +125	°C

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	$V_{VS\#}$	2.7 to 5.5	V
Supply voltage	V_{VSP}	2.7 to 5.5	V
Ambient temperature	T_{amb}	–20 to +85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO36	R_{thJA}	130	K/W

Electrical Characteristics

V_S = 2.7 to 5.5 V, T_{amb} = –20°C to +85°C, final test at 25°C

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply voltages VS#	$V_{VS1} = V_{VS2} = V_{VS3}$	$V_{VS\#}$	2.7		5.5	V
Supply voltage VSP		V_{VSP}	$V_{VS\#} - 0.3$		5.5	V
Supply current I_{VS1}	Active (V_{PU} = VS)	I_{VS1A}		17	22	mA
	Standby (V_{PU} = 0)	I_{VS1Y}			20	µA
Supply current I_{VS2}	Active (V_{PU} = VS)	I_{VS2A}		17	22	mA
	Standby (V_{PU} = 0)	I_{VS2Y}			20	µA
Supply current I_{VS3}	Active (V_{PUMIX} = VS)	I_{VS3A}		13	17	mA
	Standby (V_{PUMIX} = 0)	I_{VS3Y}			30	µA
Supply current I_{VSP} [1]	Active (V_{PU} = VS, CPO open)	I_{VSPA}		1.4	1.8	mA
	Standby (V_{PU} = 0)	I_{VSPY}			20	µA
N & R divider inputs ND, NND & RD, NRD						
N:1 divider frequency	50-Ω source	f_{ND}	100		600	MHz
R:1 divider frequency	50-Ω source	f_{RD}	100		600	MHz
Input impedance	Active & standby	Z_{RD}, Z_{ND}	1			kΩ
Input sensitivity	50-Ω source	V_{RD}, V_{ND}	5 [2]		200	mV_{rms}
Input capacitance	Active & standby	C_{RD}, C_{ND}			0.5	pF

1) Mean value, measured with F_{ND} = 151 MHz, F_{RD} = 150 MHz, current vs. time, see page 6, figure 3
2) For optimized noise performance this voltage level may be higher

Electrical Characteristics (continued)

V_S = 2.7 to 5.5 V, T_{amb} = –20°C to +85°C, final test at 25°C

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Phase-frequency detector (PFD)						
PFD operation	f_{ND} = 600 MHz, N = 2 f_{RD} = 600 MHz, R = 2	f_{PFD}	50		300	MHz
Frequency comparison only [4]	f_{ND} = 600 MHz, N = 2 f_{RD} = 450 MHz, R = 2	f_{FD}			400	MHz
I/Q modulator baseband inputs I, NI & Q, NQ						
DC voltage	Referred to GND	V_I, V_{NI}, V_Q, V_{NQ}	1.35	VS1/2	VS1/2 + 0.1	V
MD_IQ	Frequency range	f_{IO}	0		1	MHz
AC voltage [5]	Referred to GND	AC_I, AC_{NI}, AC_Q, AC_{NQ}		200		mV_{pp}
AC voltage	Differential (preferres)	AC_{DI}, AC_{DQ}		400		mV_{pp}
I/Q modulator LO input MDLO						
MDLO	Frequency range	f_{MDLO}	100		450	MHz
Input impedance	Active & standby	Z_{MDLO}		3		kΩ
Input level	50-Ω source	P_{MDLO}	–14	–11	–5	dBm
I/Q modulator outputs MDO, NMDO						
DC current	V_{MDO}, V_{NMDO} = VS	I_{MDO}, I_{NMDO}		0.8		mA
Internal pull-up resistor		R_{MDO}, R_{NMDO}		615		Ω
Voltage compliance	V_{MDO}, V_{NMDO} = VC	VC_{MDO}, VC_{NMDO}	V_S – 0.7		5.5	V
MDO output level (differential)	615 Ω to VS [6] 1.5 pF external load	P_{MDO}	40		60	mV_{rms}
Carrier suppression [6]		CS_{MDO}	–32	–35		dBc
Sideband suppression [6]		SS_{MDO}	–35	–40		dBc
IF spurious [6]	$f_{LO} \pm 3 \times f_{mod}$	SP_{MDO}		–50	–45	dBc
Noise [6]	@ 400 kHz off carrier	N_{MDO}			–115	dBc/Hz
Frequency range		f_{MDO}	100		450	MHz
Mixer (900 MHz)						
RF input level	900 MHz	$P9_{RF}$	–23		–17	dBm
Output resistance		R_{MIXO}, R_{NMIXO}		650		Ω
LO-spurious at RF/NRF port	@ $P9_{MIXLO}$ = –10 dBm @ $P9_{RF}$ = –15 dBm	$SP9_{RF}$			–40	dBm
MIXLO input level	0.05 to 2 GHz	$P9_{MIXLO}$	–22		–12	dBm
MIXO	Frequency range	f_{MIXO}	50		450	MHz
Output level [7] differential	@ $P9_{MIXLO}$ = –15 dBm	$P9_{MIXO}$		80		mV_{rms}
Carrier suppression	@ $P9_{MIXLO}$ = –15 dBm	$CS9_{MIXO}$	–20			dBc

4) PFD can be used as a frequency comparator until 300 MHz for loop acquisition
5) Single-ended operation (complementary baseband input is AC-grounded) leads to reduced linearity (degrading suppression of odd harmonics)
6) With typical drive levels at MDLO- & I/Q-inputs
7) –1 dB compression point C = 1.5 pF to GND

Electrical Characteristics (continued)

V_S = 2.7 to 5.5 V, T_{amb} = –20°C to +85°C, final test at 25°C

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Mixer (1900 MHz)						
Output resistance		R_{MIXO}, R_{NMIXO}		650		Ω
RF input level	0.5 to 2 GHz	$P19_{RF}$	–23		–17	dBm
LO-spurious at RF/NRF ports	@ $P19_{MIXLO}$ = –10 dBm @ $P19_{RF}$ = –15 dBm	$SP19_{RF}$			–40	dBm
MIXLO input level	0.05 to 2 GHz	$P19_{MIXLO}$	–22		–12	dBm
MIXO						
Output level [8] differential	@ $P19_{MIXLO}$ = –17 dBm	$P19_{MIXO}$		70		mVrms
Carrier suppression	@ $P19_{MIXLO}$ = –17 dBm	$CS19_{MIXO}$	–20			dBc
Charge-pump output CPO (V_{VSP} = 5 V; V_{CPO} = 2.5 V)						
Pump-current pulse	R_{CPCH} [9] = 4.7 kΩ	$\lvert I_{CPO\_H} \rvert$	1.4	2	2.6	mA
	R_{CPCL} [10] = 2.4 kΩ	$\lvert I_{CPO\_L} \rvert$	3	4	5	mA
Sensivity to V_{VSP}	$\lvert\frac{\Delta I_{CPO}}{I_{CPO}}\rvert \Big/ \lvert\frac{\Delta V_{VSP}}{V_{VSP}}\rvert$	S_{ICPO}			0.1	–
V_{CPO} voltage range	$\lvert I_{CPO} \rvert$ degradation < 10% (V_{VSP} = 2.7 V to 5 V)	V_{CPO}	0.5		V_{VSP}–0.6	V
Mode control						
Sink current	V_{MC} = VS	I_{MC}		60		µA
Power-up input PU (power-up for all functions, except mixer)						
Settling time	Output power within 10% of steady state values	S_{PU}		5	10	µs
High level	Active	V_{PUH}	2.0			V
Low level	Standby	V_{PUL}	0		0.4	V
High-level current	Active, V_{PUH} = 2.2 V	I_{PUH}			70	µA
Low-level current	Standby, V_{PUL} = 0.4 V	I_{PUL}	–1		20	µA
Power-up input PUMIX (power-up for mixer only)						
Settling time	Output power within 10% of steady state values	t_{setl}		5	10	µs
High level	Active	V_{PUMIXH}	2.0			V
Low level	Standby	V_{PUMIXL}	0		0.4	V
High-level current	Active, V_{PUMIXH} = 2.2 V	I_{PUMIXH}	0.1		70	µA
Low-level current	Standby, V_{PUMIXL} = 0.4 V	I_{PUMIXL}	–1		20	µA

8) – 1 dB compression point C = 1.5 pF to GND

9) R_{CPCH}: external resistor to GND for charge-pump current control (MODE 1, 5, only Pin 14 active)

10) R_{CPCL}: external resistor to GND for charge-pump current control (MODE 2, 3, 4, only Pin 13 active)

Supply Current of the Charge Pump I_{VSP} vs. Time

Due to the pulsed operation of the charge pump, the current into the charge-pump supply pin VSP is not constant. Depending on I (see figure 5) and the phase difference at the phase detector inputs, the current I_{VSP} over time varies. Basically, the total current is the sum of the quiescent current, the charge-/discharge current, and – after each phase comparison cycle – a current spike (see figure 3).

Internal current $|I_{CPC}|$ vs. R_{CPC}

R_{CPC}	$\|I_{CPCO}\|$
19.2 kΩ	0.5 mA
9.6 kΩ	1 mA
4.8 kΩ	2 mA
2.4 kΩ	4 mA

(typical values)

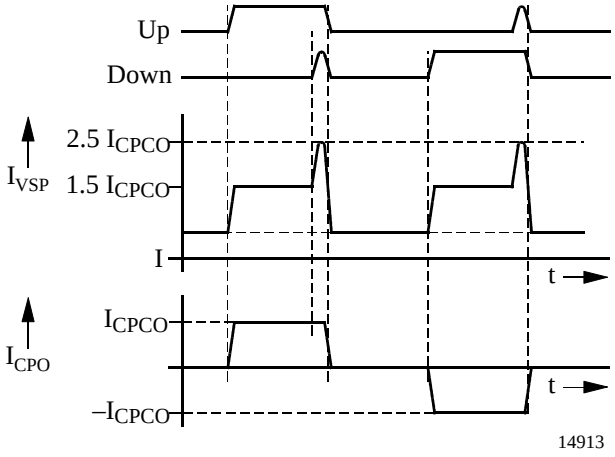


Figure 3. Supply current of the charge pump

Mode Selection

The device can be programmed to different modes via an external resistor RMODE (including short, open) from Pin MC to VS2. The mode is distinguished from specific N-, R-divider ratios, and the polarity of the charge-pump selection.

Mode Selection		N-Divider	R-Divider	CPO Current Polarity [4]		Application	CPCH active	CPCL active
Mode	Resistance between Pin MC and Pin VS2			$f_n < f_R$ [1]	$f_n > f_R$ [1]			
1	0 (<50 Ω)	1:1	1:1	sink	source	t.b.d.	x	
2	2.7 kΩ (±5%)	1:1	1:1	source	sink	t.b.d.		x
3	10 kΩ (±5%)	1:1	2:1	source	sink	t.b.d.		x
4	47 kΩ (±5%)	2:1	2:1	source	sink	PCN/ PCS [2]		x
5	∞ (> MΩ)	2:1	2:1	sink	source	GSM [3]	x	

1) Frequencies referred to PFD input
2) LO frequencies below VCO frequency
3) LO frequencies above VCO frequency
4) Sink current into Pin CPO. Source: current out from Pin CPO.

Equivalent Circuits at the IC's Pins

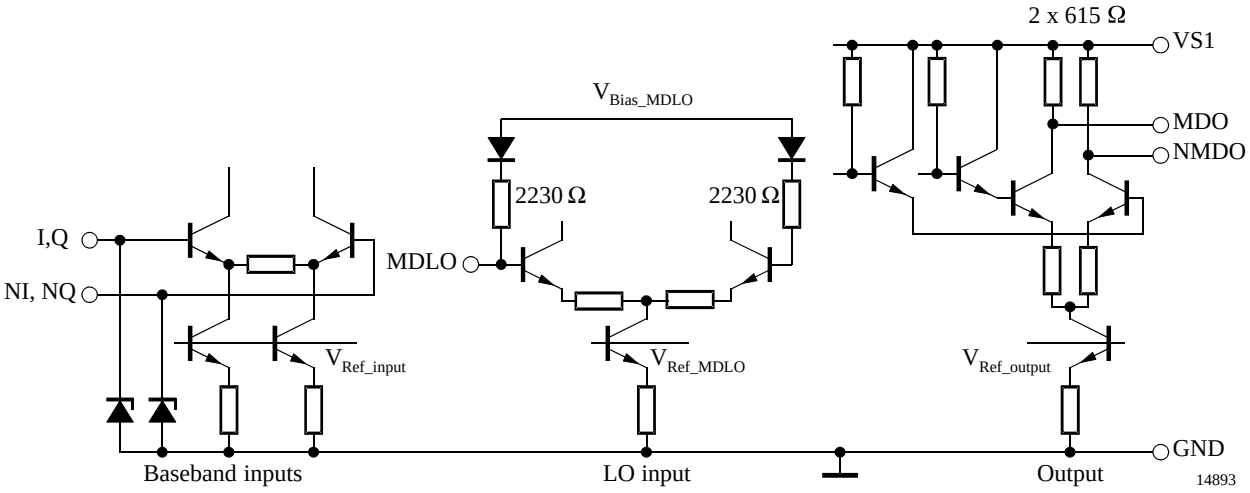


Figure 4. I/Q modulator

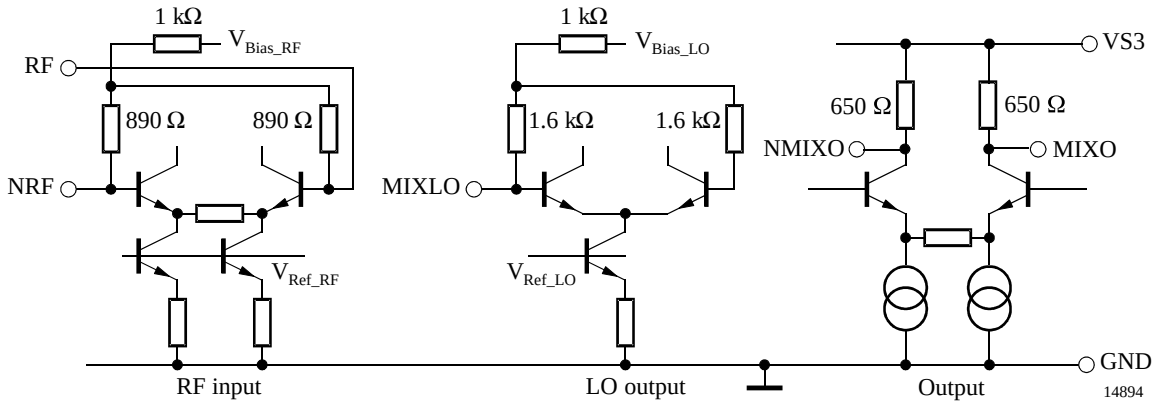


Figure 5. Mixer

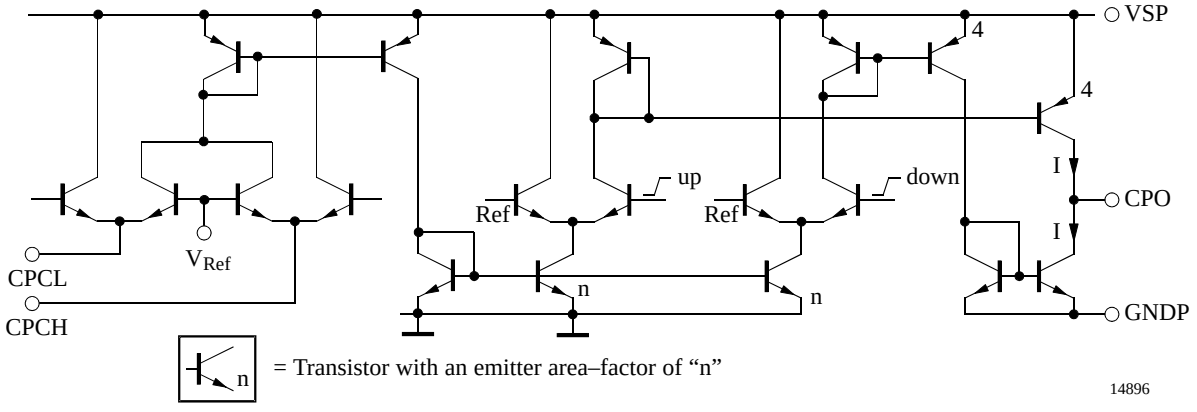


Figure 6. Charge pump

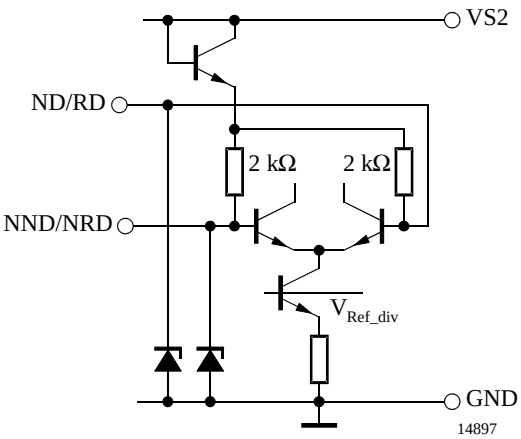


Figure 7. Dividers

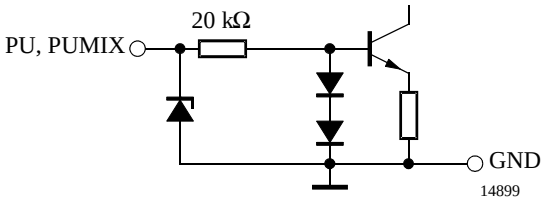


Figure 8. Power-up

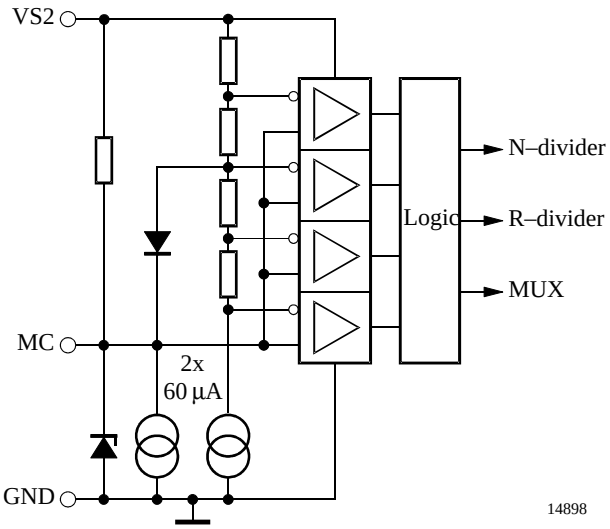
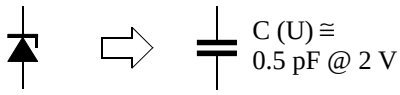


Figure 9. Mode control



C (U) is a non-linear junction capacitance

14900

Figure 10. ESD-protection diodes

Application Hints

Interfacing

For some of the baseband ICs it may be necessary to reduce the I/Q voltage swing so that it can be handled by the U2896B. In those cases, the following circuitry can be used.

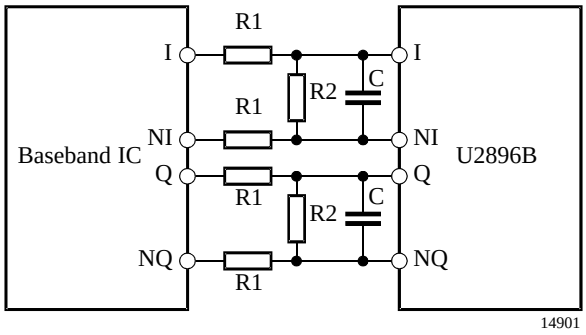


Figure 11. Interfacing the U2896B to I/Q baseband circuits

Due to a possible current offset in the differential baseband inputs of the U2896B the best values for the carrier suppression of the I/Q modulator can be achieved with voltage driven I/NI-, and Q/NQ-inputs. A value of $R_{source} = R2/2*R_S \leq 1.5\ k\Omega$ should be realized. R_S is the sum of R1 (above drawing) and the output resistance of the baseband IC.

Mode Control

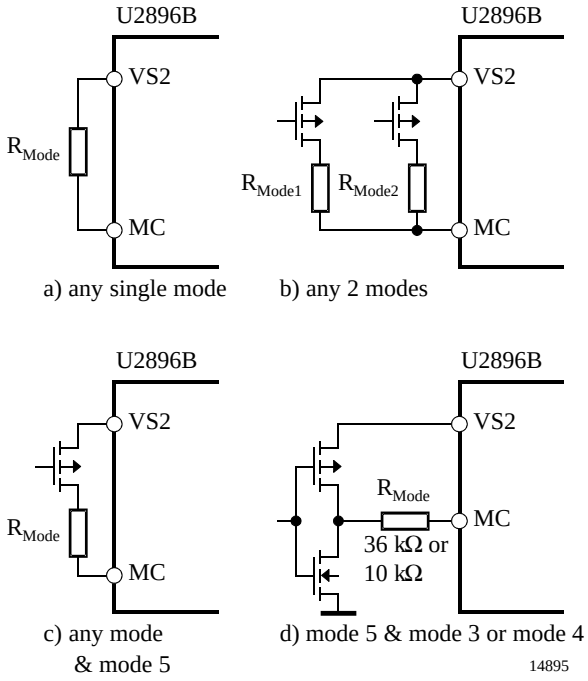


Figure 12. Application examples for programming different modes

Test Circuit

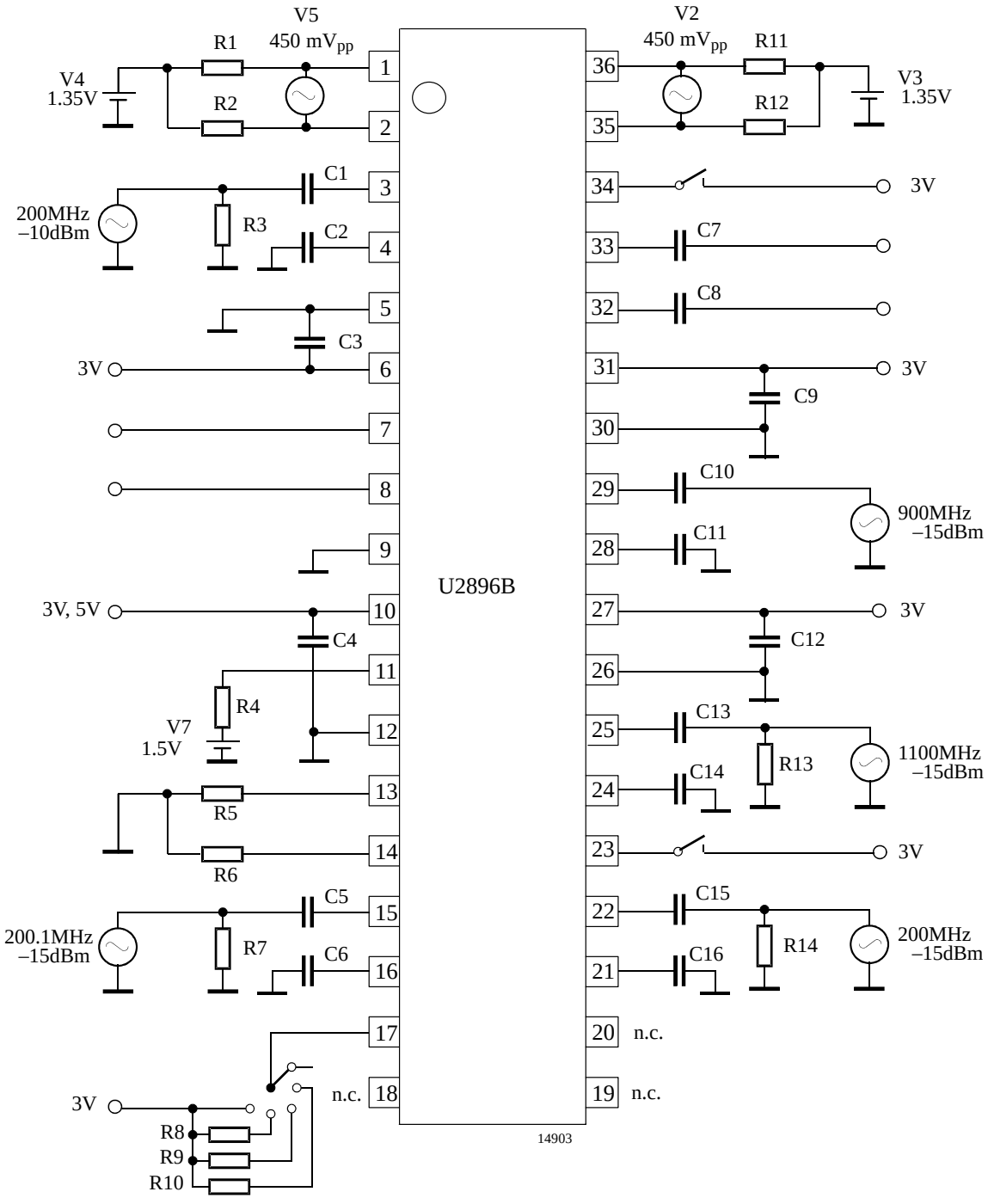


Figure 13. Test circuit

Application Circuit for DCS1800 (1710 – 1785 MHz)

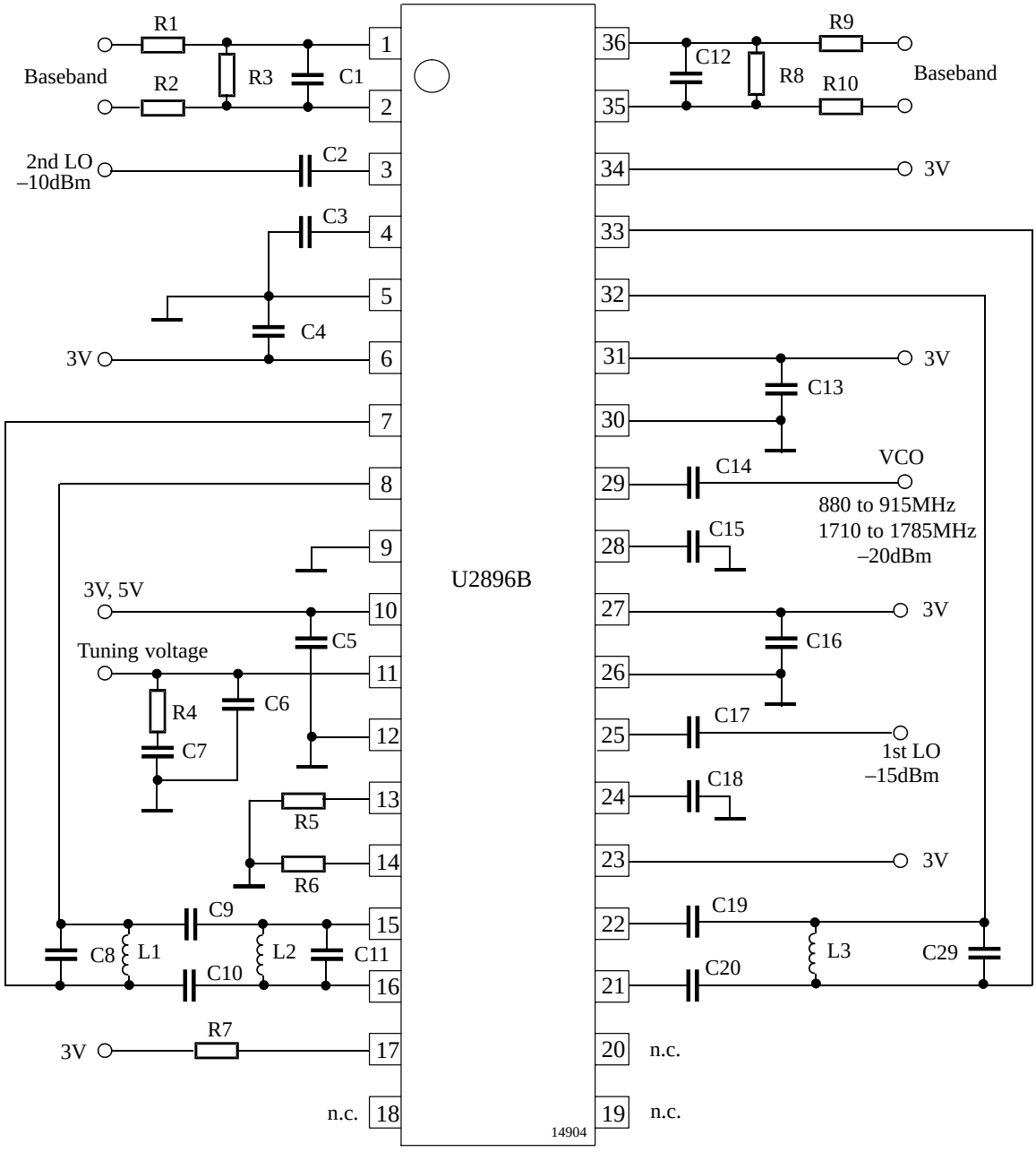


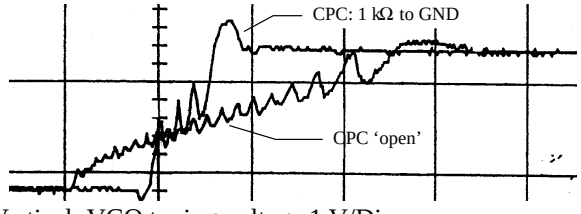
Figure 14. Application circuit

Measurements

Modulation-Loop Settling Time

As valid for all PLL loops the settling time depends on several factors. The following figure is an extraction from measurements performed in an arrangement like the application circuit. It shows that a loop settling time of a few µs can be achieved.

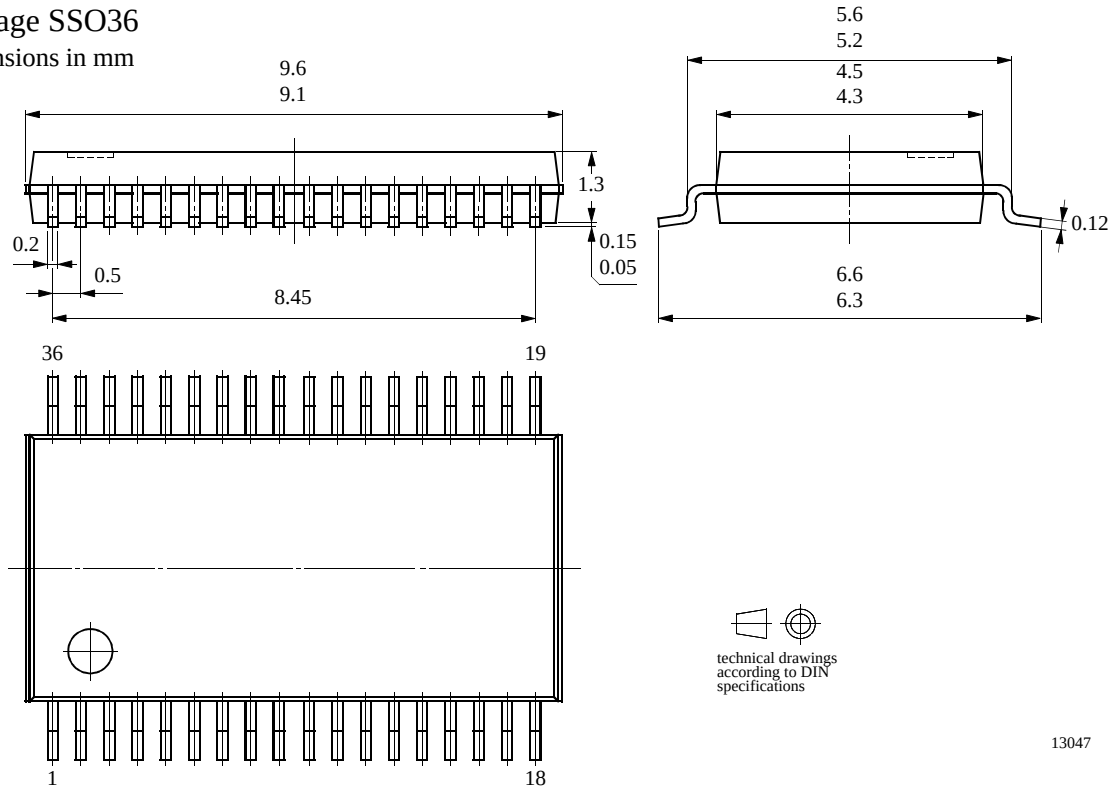
Modulation Spectrum & Phase Error



Vertical: VCO tuning voltage 1 V/Div
Horizontal: Time 1 µs/Div

Package Information

Package SSO36
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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