



TSM2N7002ED

50V Dual N-Channel Enhancement Mode MOSFET

SOT-363



Pin assignment:

- | | |
|---------------|---------------|
| 1. Source (2) | 6. Drain (2) |
| 2. Gate (2) | 5. Gate (1) |
| 3. Drain (1) | 4. Source (1) |

$V_{DS} = 50V$

$R_{DS(on)}, V_{GS} @ 10V, I_{DS} @ 250mA = 3\Omega$

$R_{DS(on)}, V_{GS} @ 5V, I_{DS} @ 50mA = 4\Omega$

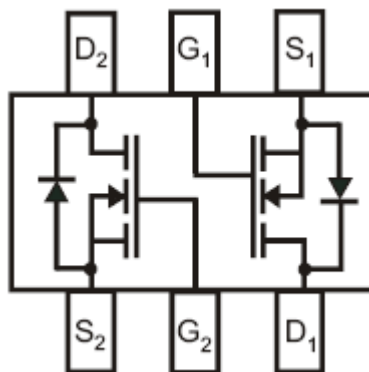
Features

- ◇ Dual N-channel in package.
- ◇ Advanced trench process technology
- ◇ High density cell design for ultra low on-resistance
- ◇ High input impedance
- ◇ High speed switching
- ◇ No minority carrier storage time
- ◇ CMOS logic compatible input
- ◇ No secondary breakdown
- ◇ Compact and low profile SOT-363 package

Ordering Information

Part No.	Packing	Package
TSM2N7002EDCU6	T & R (3kpcs/Reel)	SOT-363

Block Diagram



Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	50	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	250	mA	
Pulsed Drain Current	I_{DM}	1.0	A	
Maximum Power Dissipation		$T_a = 25^\circ C$	200	mW
		$T_a = 75^\circ C$	150	
Operating Junction Temperature	T_J	+150	$^\circ C$	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ C$	

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	5	S
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	625	$^\circ C/W$

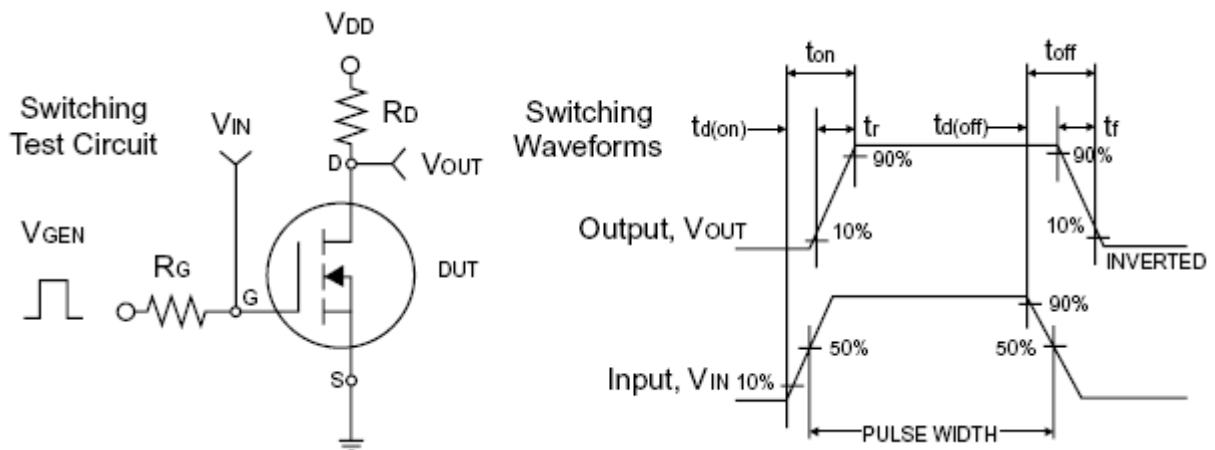
Note: Surface mounted on FR4 board $t \leq 5$ sec.



Electrical Characteristics (Single Channel)						
T _j = 25 °C unless otherwise noted						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 10uA	BV _{DSS}	50	--	--	V
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 250mA	R _{DS(ON)}	--	--	3	Ω
Drain-Source On-State Resistance	V _{GS} = 5V, I _D = 50mA	R _{DS(ON)}	--	--	4	
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250uA	V _{GS(TH)}	1.0	2.0	2.5	V
Zero Gate Voltage Drain Current	V _{DS} = 50V, V _{GS} = 0V	I _{DSS}	--	--	1.0	uA
Gate Body Leakage	V _{GS} = ± 20V, V _{DS} = 0V	I _{GSS}	--	--	± 100	nA
On-State Drain Current	V _{DS} ≥ 7V, V _{GS} = 10V	I _{D(ON)}	500	--	--	mA
Forward Transconductance	V _{DS} = 7V, I _D = 200mA	g _{fs}	80	--	--	mS
Dynamic *						
Turn-On Delay Time	V _{DD} = 30V, I _D = 100mA, V _{GEN} = 10V, R _G = 10Ω	T _{D(ON)}	--	7.5	20	nS
Turn-On Rise Time		t _r	--	6	--	
Turn-Off Delay Time		T _{D(OFF)}	--	7.5	20	
Turn-Off Fall Time		t _f	--	3	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	19	50	pF
Output Capacitance		C _{oss}	--	10	25	
Reverse Transfer Capacitance		C _{rss}	--	3	5	
Source-Drain Diode						
Max. Diode Forward Current		I _S	--	--	115	mA
Diode Forward Voltage	I _S = 115mA, V _{GS} = 0V	V _{SD}	--	0.76	1.5	V

Note : pulse test: pulse width ≤ 300uS, duty cycle ≤ 2%

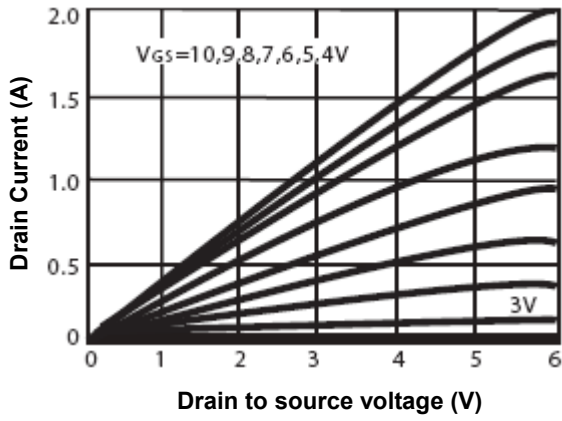
* Guaranteed by design, not subject to production testing.



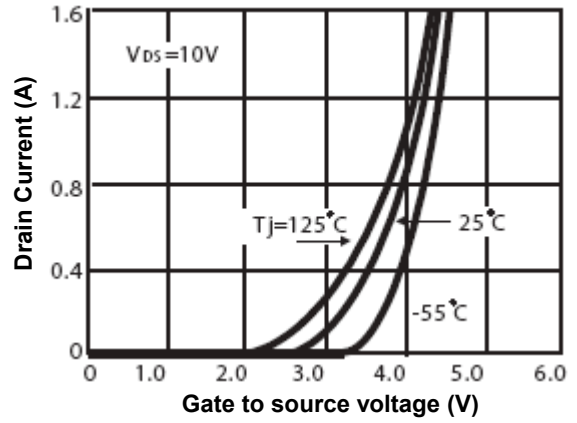


Typical Characteristics Curve - Single Channel ($T_a = 25^\circ\text{C}$ unless otherwise noted)

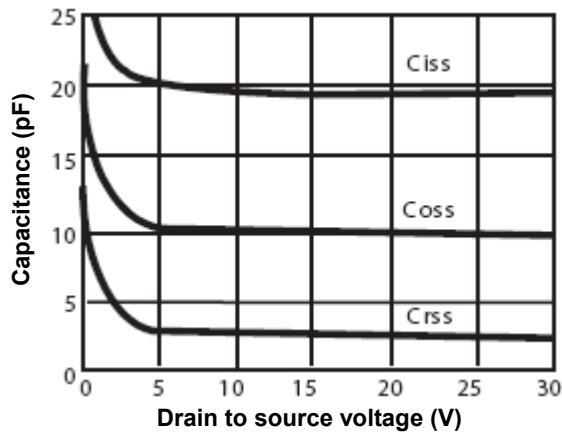
Output Characteristic



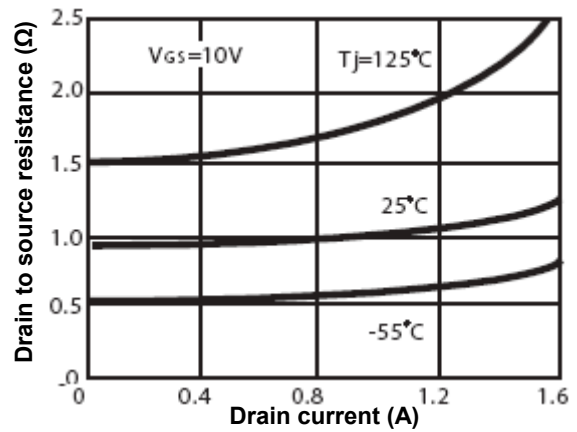
Transfer Characteristics



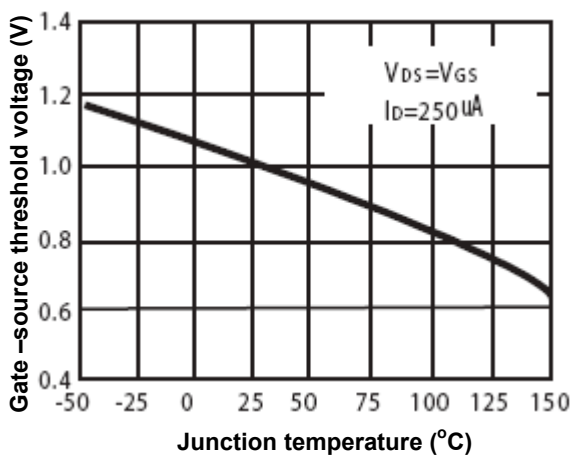
Capacitance



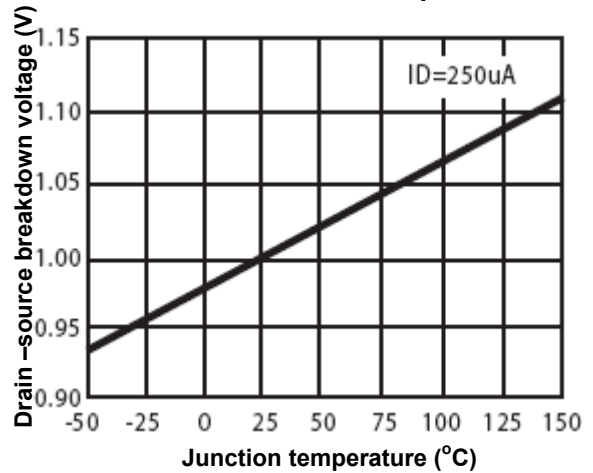
Rds(on) Variation with Drain Current



Vgs(th) with Temperature



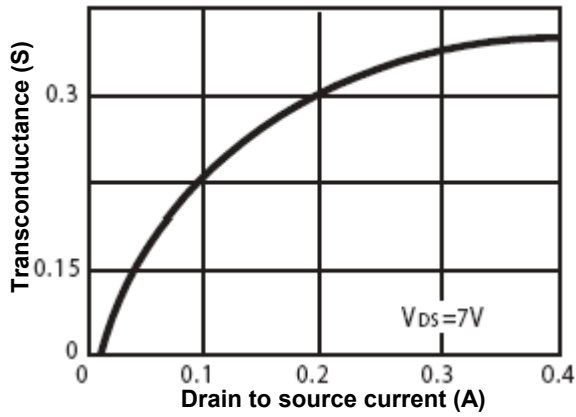
Vds breakdown with Temperature



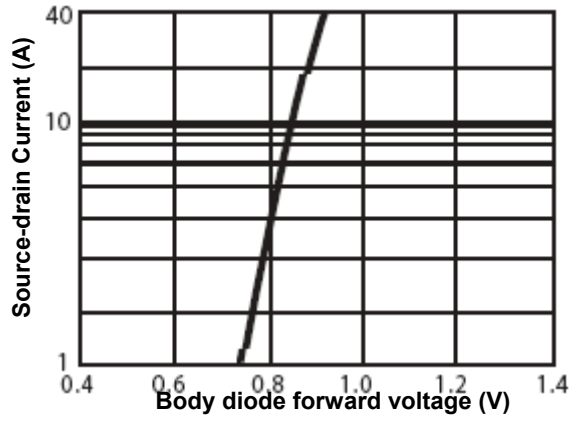


Typical Characteristics Curve ($T_a = 25^\circ\text{C}$ unless otherwise noted)

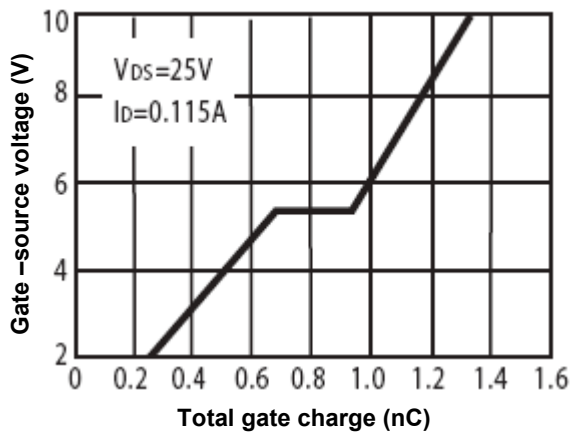
Transconductance Variation



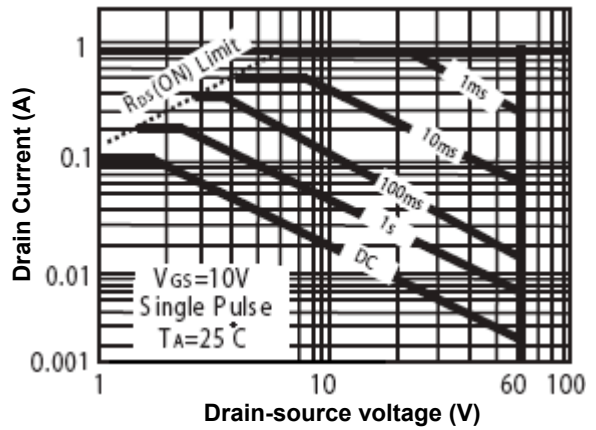
Body Diode Forward Voltage



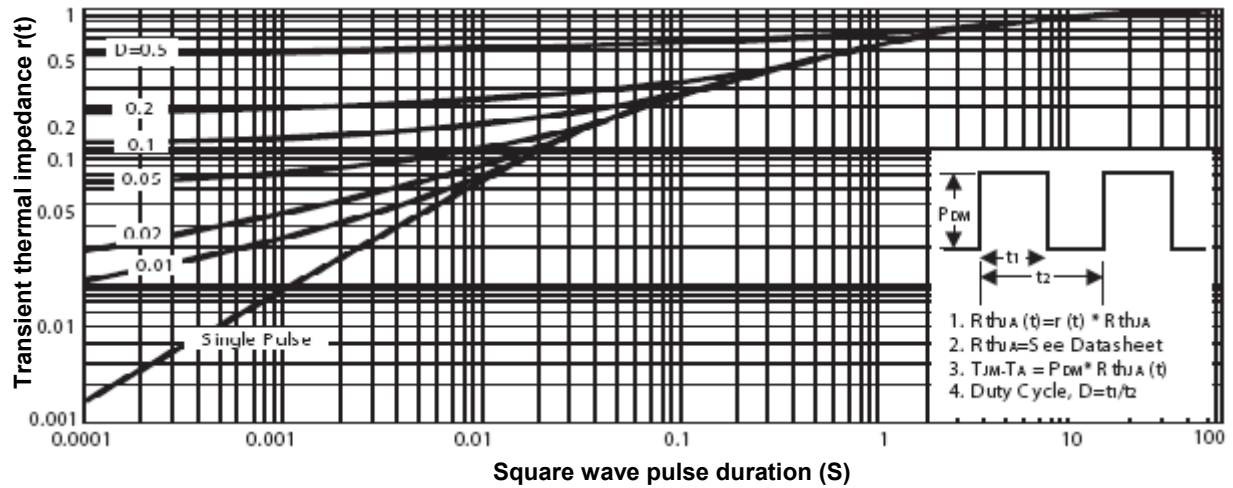
Gate Charge



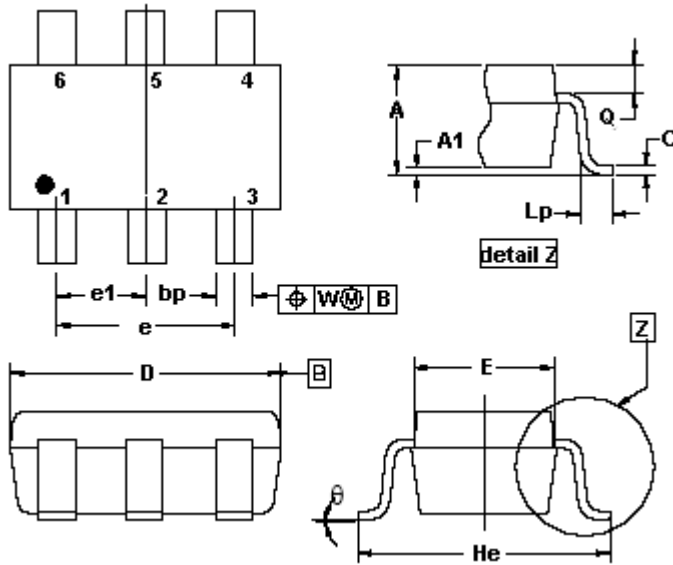
Maximum Safe Operating Area



Normalized Thermal Transient Impedance Curve



SOT-363 Mechanical Drawing



SOT-363 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.10	0.031	0.043
A1	--	0.10	--	0.004
bp	0.10	0.30	0.004	0.012
C	0.10	0.25	0.004	0.010
D	1.80	2.20	0.071	0.087
E	1.15	1.35	0.045	0.053
e	1.30 (typ)		0.052 (typ)	
e1	0.65 (typ)		0.026 (typ)	
He	2.00	2.20	0.079	0.087
Lp	0.10	0.3	0.004	0.012
Q	0.20 (typ)		0.008 (typ)	
W	0.20 (typ)		0.008 (typ)	
Theta	10° (typ)		10° (typ)	