TSM121

SINGLE CHIP PWM & HOUSEKEEPING IC FOR HALF BRIDGE SMPS

- **HOUSEKEEPING CIRCUIT :**
- Over voltage protection for 3.3V, 5V and 12V without external components
- Additional Over voltage protection (-5V and/ or -12V, or Primary Over Power control) with external components
- Under voltage protection for 3.3V, 5V and 12V without external components
- Over current protection for 3.3V, 5V and 12V with internal threshold voltage
- Externally adjustable Inrush Current blanking during transients
- Externally adjustable Under voltage blanking during Power Up
- Power Good output
- Externally adjustable PG delay
- Remote input
- Externally adjustable Remote delay
- Internal Precision Voltage Reference (Vref1)
- **PWM GENERATOR :**
- Error Amplifier (easy compensation)
- Oscillator (adjustable frequency)
- PWM generation
- Soft Start & Dead Time Control (adjustable)
- Open collector outputs for indirect Pulse Transformer driving
- Precision Voltage Reference (Vref2) (Uncommitted with Vref1)

DESCRIPTION

The TSM121 integrated circuit incorporates all sensing circuit to regulate and protect from over voltage, under voltage and over current a multiple output power supply (12V, 5V, 3.3V).

TSM121 incorporates all the necessary functions for proper PWM generation and pulse transformer drive to be adapted easily in the PC SMPS power supplies, and all the Housekeeping features which allow safe operation in all conditions, and very high integration.

TSM121 integrates two independent Voltage References which are uncommitted to ensure safe Regulation and Protection by the same chip.

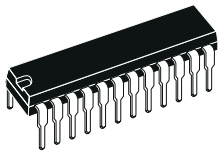
APPLICATION

- Primary PWM and secondary housekeeping in PC/Server SMPS using Half Bridge topology

ORDER CODE

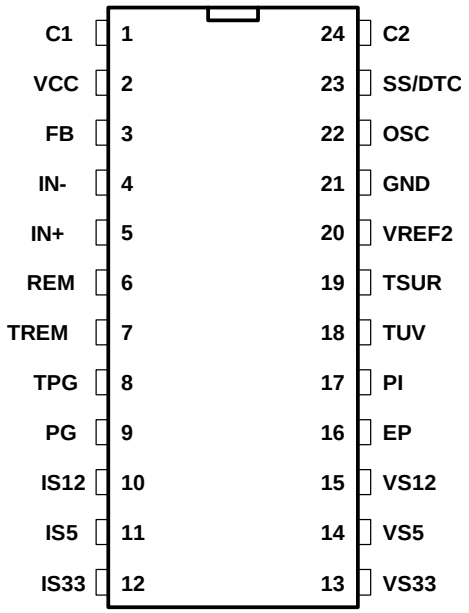
Part Number	Temperature Range	Package	Marking
		N	
TSM121C	0 to 85°C	•	TSM121C

N = Dual in Line Package (DIP)



N
DIP24 shrink
(Plastic Package)

PIN CONNECTIONS (top view)



PIN DESCRIPTION

Name	Pin #	Type	Function
Vcc	2	Power Supply	Positive Power Supply line.
Gnd	21	Power Supply	Ground. 0V Reference for all voltages.
Housekeeping			
Vs12	15	Analog input	Over & under voltage sense input dedicated to the 12V line
Vs5	14	Analog input	Over & under voltage sense input dedicated to the 5V line
Vs33	13	Analog input	Over & under voltage sense input dedicated to the 3.3V line
Tuv	18	Timing capacitor	Adjustable Under voltage blanking delay at Power Up (setting capacitor)
EP	16	Analog input	Extra Protection (Over voltage for -5V and/or -12V line or Primary OverPower protection). If this extra Protection circuit is not used, pin EP should be connected to Vref2
Is12	10	Analog input	Over current sense input dedicated to the 12V line
Is5	11	Analog input	Over current sense input dedicated to the 5V line
Is33	12	Analog input	Over current sense input dedicated to the 3.3V line
PI	17	Analog input	Power Good input. This pin detects the power conditions.
PG	9	Open Collector	Power Good output. PG output is High when the power conditions are OK.
Tpg	8	Timing capacitor	Adjustable Power Good delay (setting capacitor)
REM	6	TTL input	Input Remote control of the complete system by the motherboard (µController). Remote is active high. Switch OFF/ON of the Power Supply. Reset of the complete system after a FAULT activation.
Trem	7	Timing capacitor	Adjustable Remote delay (setting capacitor)
Tsur	19	Analog input	Inrush Current Blank (surge) setting resistor and capacitor input. Avoids that the Housekeeping protection latches on normal start up surge conditions.
PWM			
Vref2	20	Voltage Reference	Voltage Reference for all the PWM section. Vref2 is uncommitted to Vref1 (Housekeeping section). Vref2 should be connected to a decoupling capacitor (0.1µF)
IN+	5	Opamp input	Positive Input of the error amplifier
IN-	4	Opamp input	Negative Input of the error amplifier
FB	3	Feedback	Feedback input of the error amplifier
OSC	22	Timing capacitor	Frequency setting capacitor input
SS/DTC	23	Analog input	Soft Start. Imposes progressive increase of the switching duty cycle to avoid current inrush at power up. When SS/DTC is high, duty cycle is low. When SS/DTC is low, duty cycle is high. Dead Time Control. Limits the maximum duty cycle to a programmable level using appropriate external bridge resistor.
C1	1	Open Collector	Output Drive (to Pulse Transformer. Open Collector 1)
C2	24	Open Collector	Output Drive (to Pulse Transformer. Open Collector 2)

ABSOLUTE MAXIMUM RATINGS

Symbol	DC Supply Voltage	Value	Unit
Vcc	DC Supply voltage pin 2 [1)]	25	V
Iout	Output current Power Good and Fault	30	mA
Co	Collector Output Current	50	mA
Top	Operating Free Air Temperature Range	-55 to 125	°C
Pd	Power dissipation	1	W
Tstg	Storage temperature	-55 to 125	°C
Tuv	Adjustable Under voltage blanking delay at Power Up	5	V
EP	Extra Protection	5	V
PI	Power Good input	5	V
PG	Power Good output	5	V
Tpg	Adjustable Power Good delay	5	V
REM	Remote control	5	V
Trem	Adjustable Remote delay	5	V
Tsur	Adjustable Inrush Current Blank (surge)	5	V
IN+	Positive Input of the error amplifier	5	V
IN-	Negative Input of the error amplifier	5	V
FB	Feedback input of the error amplifier	5	V
OSC	Frequency setting capacitor input	5	V

1. All voltages values , except differential voltage , are with respect to network ground terminal .

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage [1)]	14 to 24	V
Co	Collector Output Current	up to 30	mA
Freq	Oscillator Frequency	<200	kHz
Toper	Operating Free Air Temperature Range	0 to 85	°C

1. The TSM121 starts working properly before 14V, but the 12V line over current protection can be reliable only when Vcc has reached a sufficient level: t(he DC supply voltage must be higher than the voltage applied on the Is12 input (12V line protection) plus 2V. For example, if 13.2V is present on the IS12 input, the minimum required value on Vcc is 15.2V.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C and V_{cc} = 17V (unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Total Current Consumption						
Icc	Total Supply Current			7	12	mA
HOUSEKEEPING SECTION						
Voltage Reference (Vref1)						
Vref1	Internal Voltage Reference			2.5		V
Over Current, Over Voltage and Under Voltage Protection						
Vcs33	Over Current Sense Threshold 3.3V		46.5	50	53.5	mV
Vcs5	Over Current Sense Threshold 5V		46.5	50	53.5	mV
Vcs12	Over Current Sense Threshold 12V		60.5	65	69.5	mV
Vov33	Over Voltage Sense 3.3V		3.8	4	4.2	V
Vov5	Over Voltage Sense 5V		5.8	6.1	6.4	V
Vov12	Over Voltage Sense12V		13.4	14.2	15	V
Vuv33	Under Voltage Sense 3.3V		2.1	2.3	2.5	V
Vuv5	Under Voltage Sense 5V		3.7	4	4.3	V
Vuv12	Under Voltage Sense 12V		9.2	10	10.8	V
Vep	Extra Over voltage Protection Threshold			1.25		V
Tfault	Fault Delay Before Latching	Internally Fixed Delay		150		µs
Current Surge Blanking						
Vsur	Threshold Voltage			2.5		V
Tsur	Current Surge blank	Rsur = 33kΩ, Csur = 4.7µF		21		ms
Vsurth	Surge detection clamp voltage			6		V
Under Voltage Blanking During Power Up						
Tuv	Under Voltage Blanking During Power Up (Vcc rise)	Cuv = 2.2µF	100	300	500	ms
Thuv	Blanking Threshold			2.5		V
Power Good (PG)						
Vpgth	Power Good Voltage Threshold			2.5		V
Vpghyst	Power Good Voltage Threshold Hysteresis			150		mV
Vpgol	Low Output Open Collector Saturation Voltage	Collector Current = 15mA			0.4	V
Ipgoh	High Output Open Collector Leakage Current	PG Output = 5V			1	µA
Tpgr	Power Good Output Rise Time	Load Capacitor = 100pF		1		µs
Tpgf	Power Good Output Fall Time	Load Capacitor = 100pF		1		µs
Tpg	Power Good Adjustable Delay	Load Capacitor Cpg=2.2µF	100	300	500	ms
PIth	Power Input Detection Threshold			1.25		V
Remote Control (REM)						
Vremth	Remote ON/OFF Input Voltage Threshold		0.7	0.8	1	V
Vremih	High Input Remote Voltage		4.8	5		V
Iremil	Low Input Remote Saturation Current				0.5	mA
Trem1	Remote Adjustable Delay ON to OFF	Load Capacitor Crem=0.1µF	40	50	60	ms

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Trem2	Remote Adjustable Delay OFF to ON	Load Capacitor Crem=0.1µF	40	50	60	ms
PWM SECTION						
Voltage Reference (Vref2)						
Vref2	Voltage Reference	Iout = 0mA	2.46	2.5	2.54	V
Is	Current Stability = Load Regulation	Iout = 0mA to 10mA			20	mV
Ts	Temperature Stability				17	mV
Regline	Line Regulation	Iout <10mA, Vcc=14 to 24V			10	mV
Iout	Output Sourcing Current Capability		15	30		mA
Error Amplifier (IN+, IN-)						
Vio	Input Offset Voltage	Vout (Feedback) = 2.5V		0	3	mV
Iio	Input Offset Current	Vout (Feedback) = 2.5V			50	nA
Iib	Input Bias Current	Vout (Feedback) = 2.5V			200	nA
GBP	Gain Bandwidth Product	RL = 2kΩ, CL = 100pF		5		MHz
Vicm	Input Common Mode Voltage Range		-0.3		3.5	V
CMR	Common Mode Rejection Ratio			80		dB
Isink	Output Sink Current	Vout (Feedback) = 0.7V		1		mA
PWM Comparator						
∆max	Maximum Duty Cycle	Soft Start=0V	45	48	50	%
Vicmp	Input Common Mode Voltage Range		-0.3		3.5	V
Soft Start & Dead Time Control						
Vssth	Soft Start Voltage Threshold	Zero Duty Cycle Maximum Duty Cycle		2.5 0		V
Vicms	Input Common Mode Voltage Range		-0.3		3.5	V
Oscillator (OSC)						
Freq	Oscillator Frequency	Cf=220pF	70	100	140	kHz
Open Collector Outputs (C1, C2, Sink Current Only)						
Icoh	High Output Collector Leakage Current			0.5	2	µA
Vcol	Low Output Collector Saturation Voltage	Collector Current = 20mA		0.2	0.5	V
tr	C1, C2 rise time			1		µs
tf	C1, C2 fall time			1		µs

Figure 1 : Application Schematic. Power Supply Based On Half Bridge + Pulse Transformer Topology

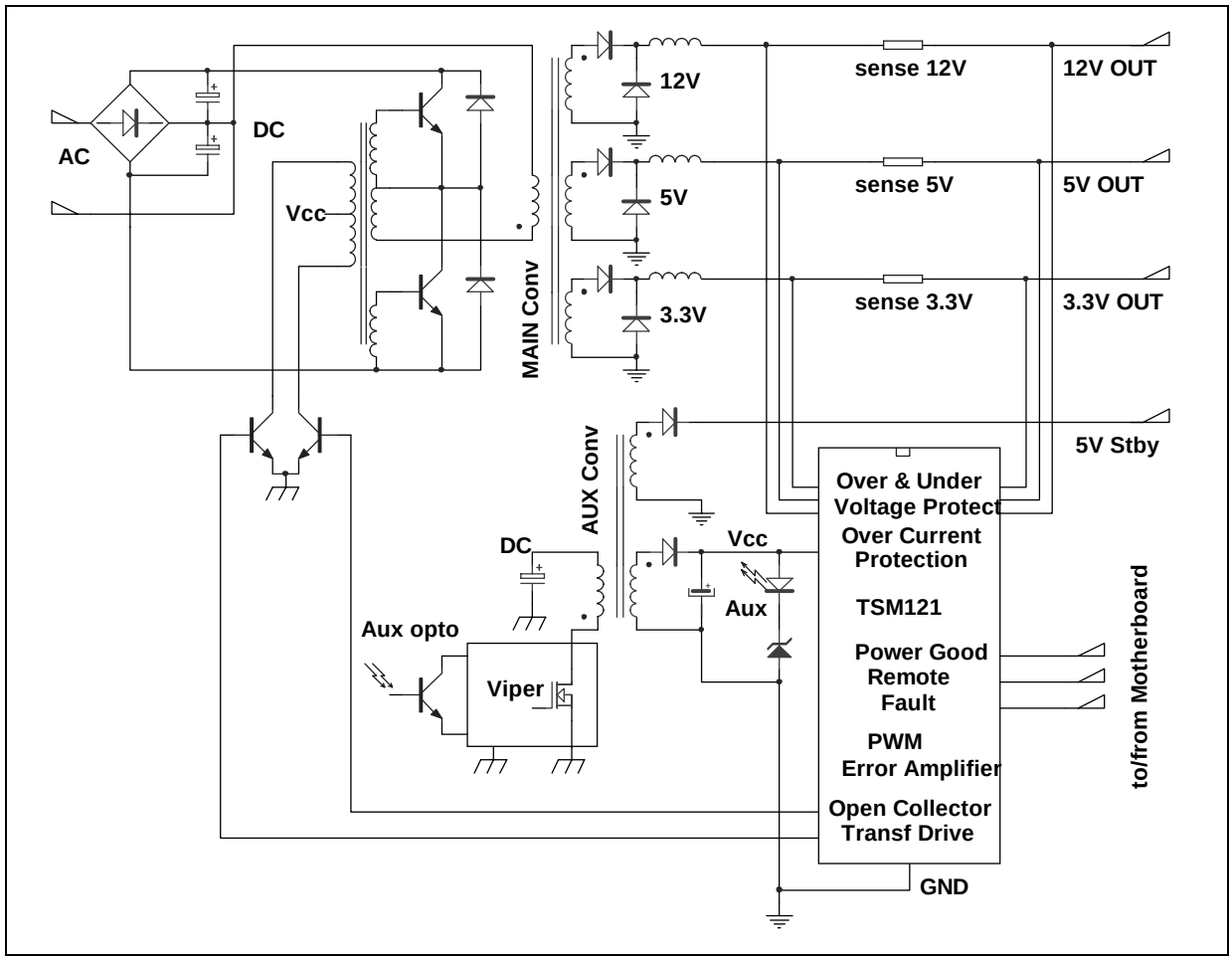


Figure 2 : Internal Schematic

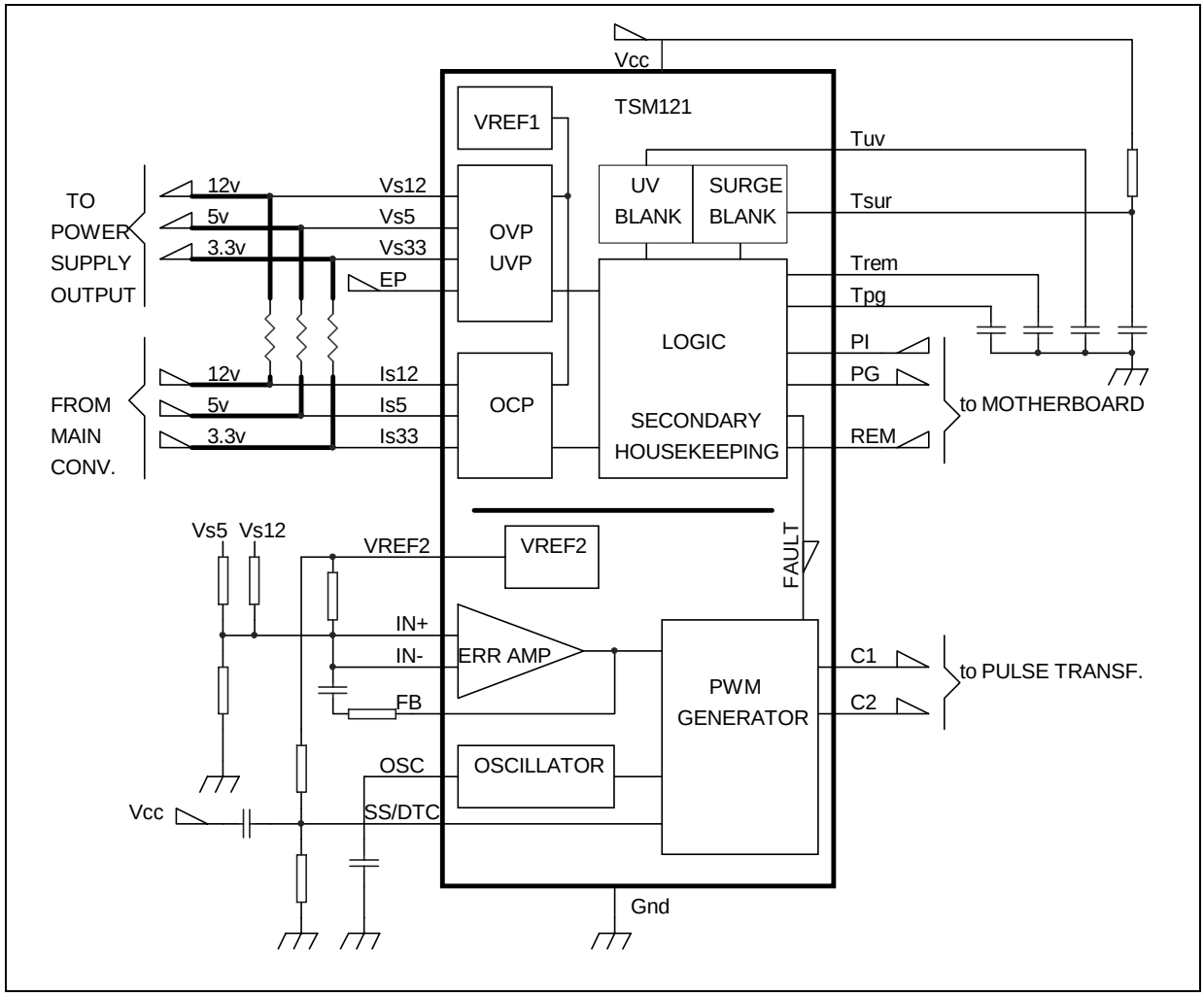
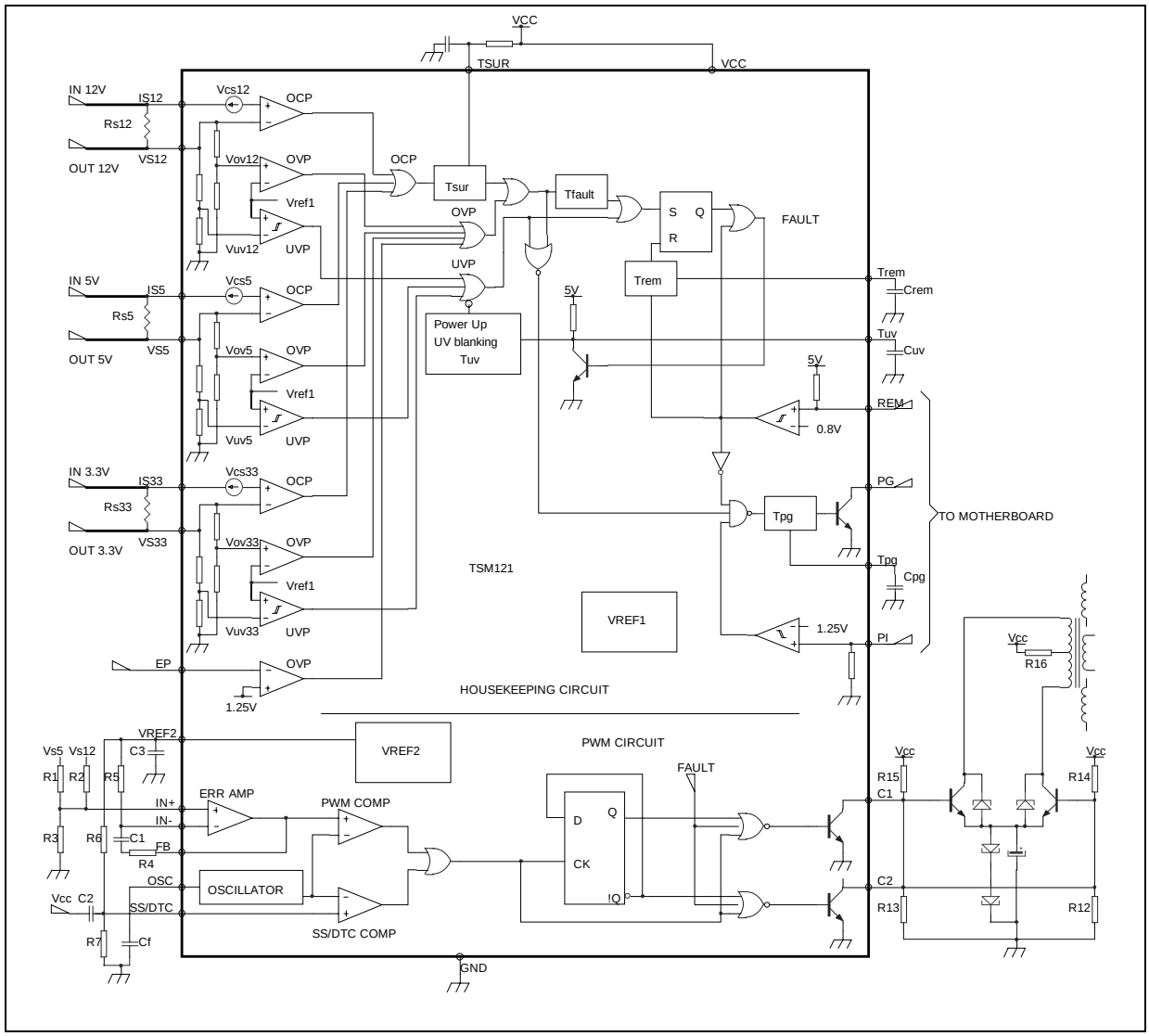


Figure 3 : Detailed Internal Schematic



PRINCIPLE OF OPERATION & APPLICATION HINTS

TSM121 is a one chip solution for all PC SMPS based on the half bridge topology: it integrates on the same chip the PWM circuitry (generating the appropriate signals for the power lines voltage regulations) as well as the HOUSEKEEPING circuitry (Over voltage, Over current, Under voltage protections as well as logic interface for proper communication with motherboard).

1. PWM Generator and Regulation Circuit:

The PWM Generator circuit is composed of an Error Amplifier, a Saw Tooth Oscillator, a PWM Comparator, a Soft Start/Dead Time Control Comparator, a D-Latch and two Open Collector Outputs.

1.1. Error Amplifier

The Error Amplifier delivers a signal proportional to the positive and negative inputs voltage difference (IN+, IN-). The output of this error amplifier can be compensated thanks to the Feedback (FB) pin with a compensation network inserted between the output (FB) and the negative input (IN-) (see figure 3). This error amplifier should be used to amplify the error between the middle point of a resistor bridge connected to the output power line(s) to be regulated (as an example), and the internal Voltage Reference Vref2 (as shown on figure 3).

The resistors should fit the following equation:

Vref2 / (R3 + VR1) = (Vs5 - Vref2) / R1 + (Vs12 - Vref2) / R2

Recommended values are: R3=4.7kΩ, R1=10kΩ, R2=39kΩ

VR1 is an optional potentiometer which can be used to obtain more accurate 5V and 12V lines. Its recommended range is 0 to 1kΩ.

To compensate the error amplifier, the recommended values are: C1=10nF, R4=43kΩ, R5=10kΩ. These values need to be adjusted according to the whole system.

1.2. Oscillator

The Oscillator frequency is to be fixed with an external capacitor (220pF for 100kHz typical) and gives a Saw Tooth Oscillation wave form with positive ramp (see figure 3).

1.3. PWM Comparator

The PWM Comparator takes both outputs from the Error Amplifier and the Saw Tooth Oscillator. The resulting signal is a square wave oscillation.

1.4. Soft Start & Dead Time Control

The Soft Start/Dead Time Control Comparator has two distinct functions.

The Soft Start function ensures that during start up (power up of the complete SMPS at mains switch ON) the switching duty cycle starts from 0% for safe operation during the charging of all output capacitive loads. This can be achieved by setting an R7/C2 couple to be connected to the SS/DTC input.

The Soft Start Time is determined by R7 and C2. In all cases, pay attention to the fact that the bypass capacitor C3 will degrade the Soft Start function. From this point of view, the value of the bypass capacitor should be chosen equal or lower than 100nF.

The Dead Time Control allows to reduce the maximum duty cycle limit in order to limit the maximum output power. This can be achieved by adding a resistor R6 between SS/DTC input and Vref 2. This additional resistor will form a resistor bridge with the previous resistor and lower the maximum duty cycle.

The maximum duty cycle is set by R6 and R7. The duty cycle DC fits the following equation:

DC (%) = (100 x R6 / (R6 + R7)) / 2

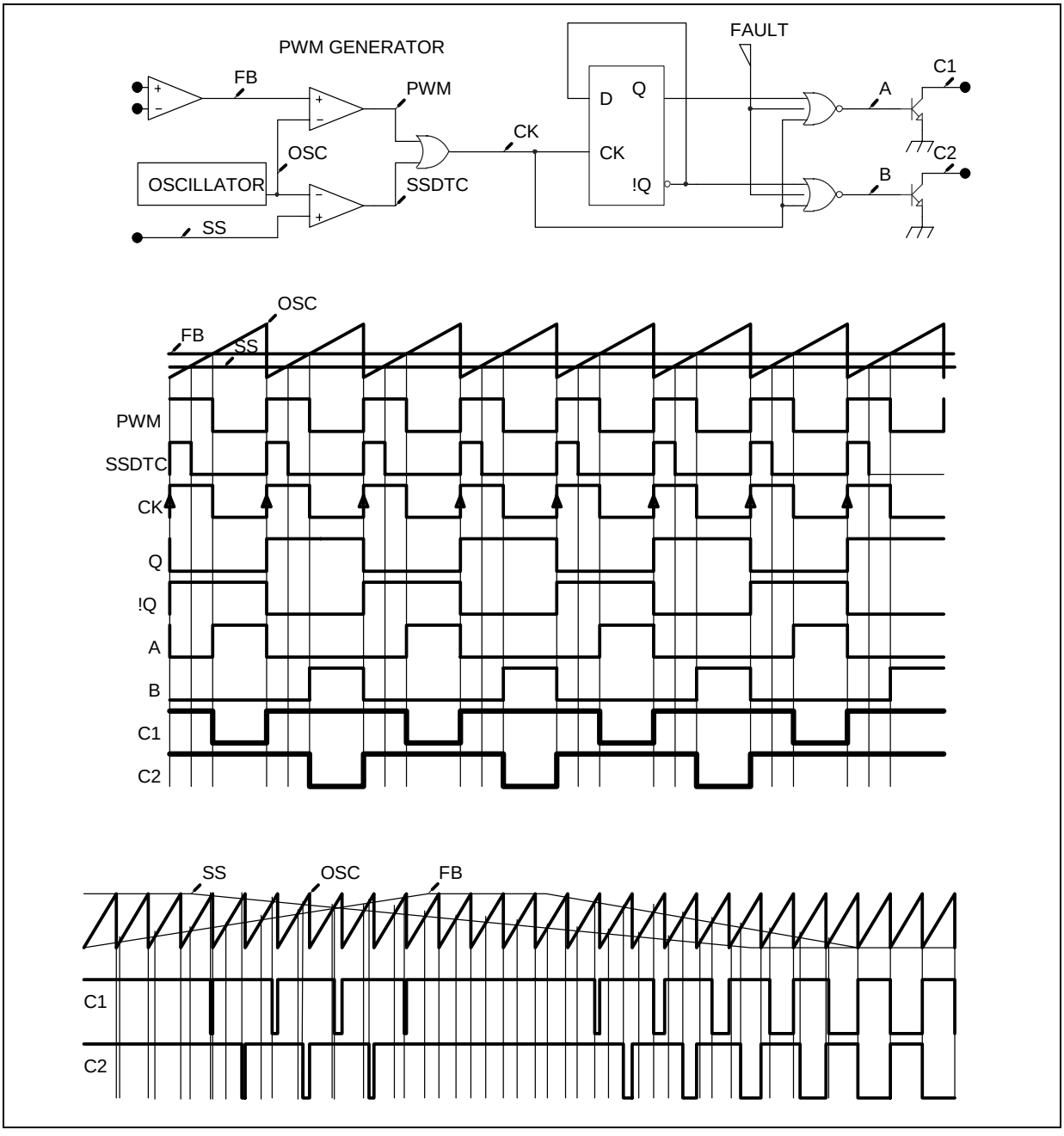
The PWM comparator and the Soft Start/Dead Time Ctrl Comparator are ORed to form the input Clock signal of the D-Latch. Using the Q and !Q outputs of the D-Latch, and combining them with some NOR logic will impose proper switching of the output Open Collector Transistors with Duty Cycle varying from 0% to 50% max (on each output, and depending on the Error Amplifier inputs & Soft Start/Dead Time Ctrl conditions).

Figure 4 summarizes all the oscillogram wave forms of the PWM Circuit.

When the Error Amplifier output (FB) is low, the C1 / C2 outputs duty cycle is high.
When the Error Amplifier output (FB) is high, the C1 / C2 outputs duty cycle is low.

When the Soft Start input (SS/DTC) is low, the C1 / C2 outputs duty cycle is high.
When the Soft Start input (SS/DTC) is high, the C1 / C2 outputs duty cycle is low.

Figure 4 :



1.5. Output Driver - Open Collectors

The typical driving current from the TSM121 is 25mA. The recommended values of R12 to R16 are:
R12=R13=3.9kΩ, R14=R15=7.5kΩ, R16=2kΩ

2. Housekeeping Circuit

The TSM121 Housekeeping Circuit is dedicated to 3.3V, 5V, and 12V power lines protection. It integrates a Precision Voltage reference (independent from the PWM generator circuit Voltage Reference), a triple Over current Protection circuit, a triple Over voltage Protection circuit, and a triple Under voltage Protection circuit, as well as all the necessary logic and transient timing management circuits for optimal and secure communication with the motherboard, during start up, switch off and stabilized conditions.

2.1. Over current protection circuit

The Over current protection circuit is made of 3 comparators with internal voltage thresholds requiring 3 different Sense resistors in series with the 3 different power lines. The thresholds are internally fixed to the Vcs33, Vcs5, Vcs12 values, and the sense resistors need to be chosen depending on the required over current limit. The outputs of these three comparators are ORed, and blanked by an internal delay circuitry (Surge Current Blanking - Tsur) which can be adjusted with external components (Rsur, Csur). Note that the three Over current protection circuits are blanked from current surges by the same delay circuit. This allows that during power up, large inrush currents are allowed during a short period of time corresponding to the charging of capacitive loads (see figure 3).
The maximum output currents of the 12V, 5V, and 3.3V lines are determined by Rs12, Rs5 and Rs33 respectively:
I12max = Vcs12 / Rs12
I5max = Vcs5 / Rs5
I33max = Vcs33 / Rs33

2.2. Over voltage protection circuit

The Over voltage protection circuit is made of three comparators with internal voltage thresholds (Vov33, Vov5, Vov12) which do not require any external components for proper operation. The outputs of these three comparators are ORed.

2.3. Under voltage protection circuit

The Under voltage protection circuit is made of three comparators with internal voltage thresholds (Vuv33, Vuv5, Vuv12) which do not require any external components for proper operation. The outputs of these three comparators are ORed, and blanked by an internal delay circuitry (Power Up UV Blanking - Tuv) which can be adjusted with external components (Cuv). This allows that during power up, the under voltage protection circuit is inhibited.

2.4. Logic Interface

The Over current, Over voltage and Under voltage circuits outputs are again ORed before activating a Latch. When activated, this latch commands the full switch OFF of the three main power lines (3.3V, 5V, 12V) by an internal link between the Housekeeping and the PWM circuits. Note that the Under voltage circuit, after power up UV blanking, bears no other delay to the Latch setting input whereas the Over current and Over voltage circuits both bear an additional Tfault delay time. This allows an efficient protection against Output Short Circuit Conditions.

The Over current, Over voltage and Under voltage circuits are all ORed to switch the Power Good output active (PG) to warn the motherboard that the voltage of at least one of the three power line is out of range. The PG activation bears an internal Tpg delay circuitry which can be adjusted with external components (Cpg)

Thanks to this information link to the motherboard, a resetting signal to the latch is achievable with the Remote pin (REM). When the Remote pin is active, the internal Fault link between Housekeeping circuit and the PWM generator is active (high: PWM off), the PG pin is active (high). Note that to reset effectively the Latch, a minimum width Remote pulse should be applied thanks to an internal delay circuitry (Trem) which can be adjusted with external components (Crem).

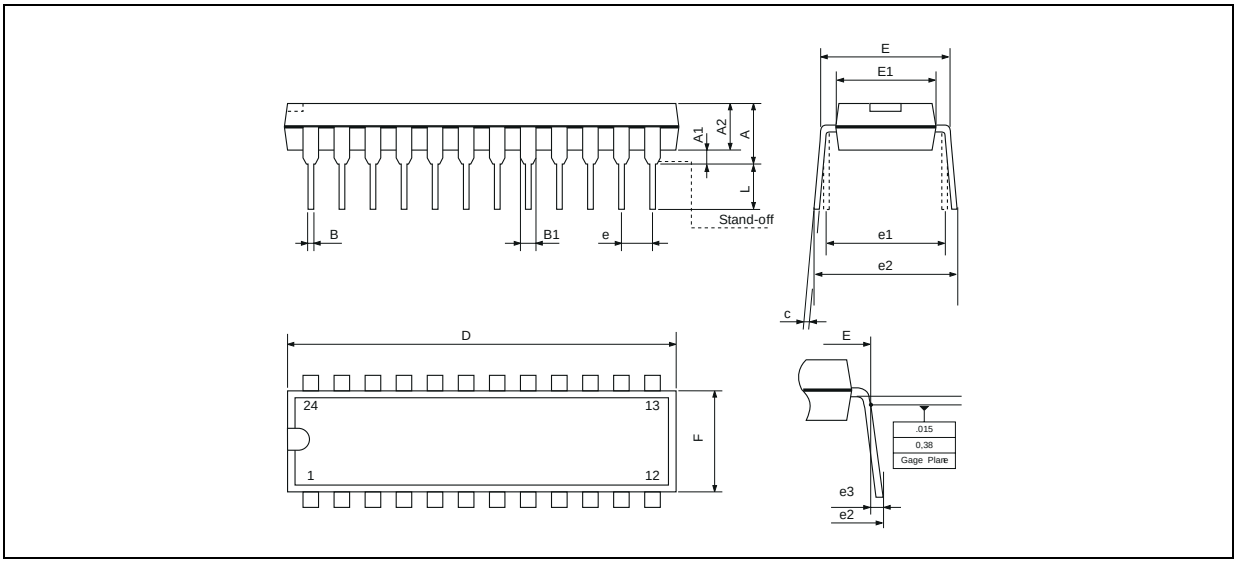
2.5. Additional circuits:

A Power Input (PI) is available for a supplementary power condition supervision. For example, the supervision of the Vcc power supply line.

An Extra Protection (EP) circuit is available for an additional input power protection. For example, this operator can be used for the supervision of the primary input power via an additional wiring at the foot of the power half bridge. This operator can also be used for the supervision of eventual negative power lines (ex: -5V or -12V).

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC PACKAGE



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060
L	2.54	3.30	3.81	0.10	0.130	0.150