TSA1401

14-BIT, 20MSPS, 85mW A/D CONVERTER

FEATURES

- **OPTIMWATT™ features [1]**
  - Ultra low power consumption: 85mW at 20Msps (using external references).
  - Adjustable consumption versus speed.
- **Single supply voltage: 2.5V**
- **Digital I/O supply voltage: 2.5V/3.3V compatible**
- **-90.5dBc SFDR and 73.1dBc SNR at Fin=10MHz when using external references (VINpp=2.5V)**
- **Differential analog input-driving**
- **Built-in reference voltage with external bias capabilities**
- **Digital output high impedance mode**

1) OPTIMWATT(TM) is a ST deposited trademark for products features allowing optimization of power efficiency at chip/application level.

DESCRIPTION

The TSA1401 is a 14-bit, 20MHz sampling frequency Analog to Digital Converter using deep submicron CMOS technology combining high performances with very low power consumption.The TSA1401 is based on a pipeline structure with digital error correction to provide excellent static linearity and dynamic performances.

Typically designed for multi-channel applications and high-end imaging equipment, where low consumption is a must, the TSA1401 only dissipates 85mW at 20Msps when using external references, 110mW using internal references. Its power consumption adapts relative to sampling frequency. Differential signals are applied on the inputs for optimum performance. The TSA1401 reaches an SFDR of -90.5dBc and an SNR of 73.1dBc at Fin=10MHz when increasing the input dynamic range to 2.5V by using the voltage reference, TS431 (1.24V).

A tri-state capability is available on the output buffers, enabling a Chip Select.The TSA1401 is available in the industrial temperature range of -40°C to +85°C and in a small 48-lead TQFP package.

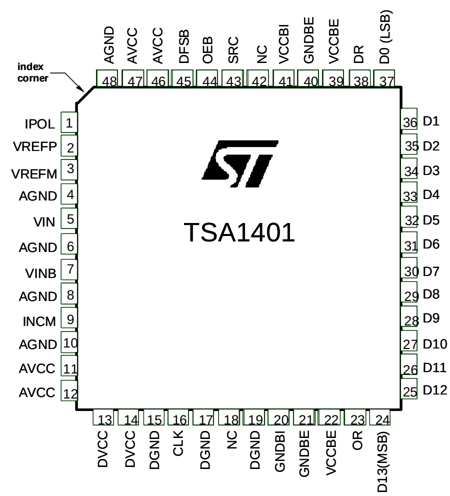
APPLICATIONS

- **High-end infra-red imaging**
- **X-Ray medical imaging**
- **High-end CCD cameras**
- **Scanners and digital copiers**
- **Test instrumentation**
- **Wireless communication**

ORDER CODES

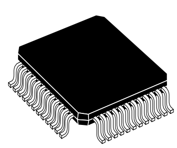
Part Number	Temperature Range	Package	Conditioning	Marking
TSA1401IF	-40°C to +85°C	TQFP48	Tray	SA1401
TSA1401IFT	-40°C to +85°C	TQFP48	Tape & Reel	SA1401
EVAL1401/AB	Evaluation board			

PIN CONNECTIONS (top view)



PACKAGE

7 x 7 mm TQFP48



1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
AVCC, DVCC, VCCBI	Analog, digital, digital buffer Supply voltage [1]	-0.3V to 3.3V	V
VCCBE	Digital buffer Supply voltage [1]	0V to 3.6V	V
VIN, VINB, VREFP, VREFM, VINCM	Analog inputs	-0.3V to AVCC+0.3V	V
IDout	Digital output current	-100mA to 100mA	mA
Tstg	Storage temperature	+150	°C
ESD	Electrical Static Discharge - HBM: Human Body Model[2] - CDM-JEDEC Standard	 2000 700	V
Latch-up	Class[3]	A	

1) All voltage values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must not exceed -0.3V or VCC

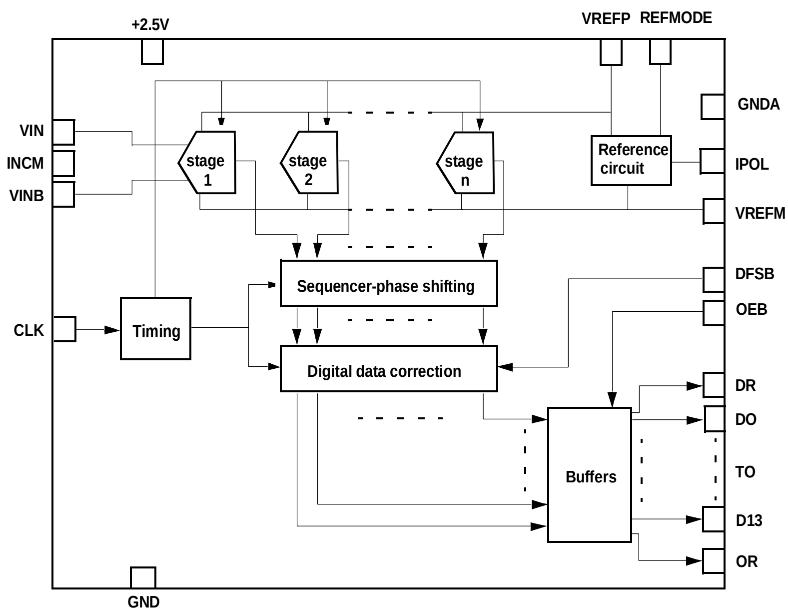
2) ElectroStatic Discharge pulse (ESD pulse) simulating a human body discharge of 100 pF through 1.5kΩ

3) ST Microelectronics Corporate procedure number 0018695

OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC	Analog Supply voltage		2.25	2.5	2.7	V
DVCC	Digital Supply voltage		2.25	2.5	2.7	V
VCCBI	Digital buffer Supply voltage		2.25	2.5	2.7	V
VCCBE	Digital buffer Supply voltage		2.25	2.5	3.3	V

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	I/O	No	Pin Description
IPOL	I	1	Analog bias current input - adjusts polarization current versus Fs.
VREFP	I/O	2	Top Reference Voltage - may be used as a voltage generator output or used as an input to adjust the input dynamic range (VIN-VINB=2x(VREFP-VREFM)).
VREFM	I	3	Bottom Reference Voltage. Usually connected to GND (see AN p12 for details)
AGND	I	4, 6, 8, 10, 48	Analog ground.
VIN	I	5	Positive Analog input.
VINB	I	7	Negative Analog Input.
INCM	I/O	9	Internal Common Mode - may be used as a voltage generator output for input signal common mode or used as an input to force the internal common mode (see AN p12 for more details).
AVCC	I	11, 12, 46, 47	Analog Power Supply (2.5V).
DVCC	I	13, 14	Digital Power Supply (2.5V) (Clock).
DGND	I	15, 17,19	Digital Ground (Clock).
CLK	I	16	CMOS Clock Input.
NC	NA	18, 42	Non Connected Pin.
GNDBI	I	20	Digital Ground (Internal Buffer).
GNDBE	I	21,40	Digital Ground (External Buffer).
VCCBE	I	22, 39	Digital Power Supply (External Buffer, 2.5V/3.3V).
OR	O	23	Over Range Indicator, if D0-D13='1' or '0', OR='1'.
D13(MSB)-D0(LSB)	O	24-37	Data CMOS Outputs (2.5V/3.3V).
DR	O	38	Data Ready Signal (2.5V/3.3V).
VCCBI	I	41	Digital Power Supply (Internal Buffers 2.5V).
REFMODE	I	43	REFMODE='VIL', internal references active. REFMODE='VIH', external references must be applied.
OEB	I	44	Output Enable Input. If OEB='VIH' then D0-D13 in 'High Z' state.
DFSB	I	45	Data Format Select Input - If DFSB='VIH' then D13 is standard binary output coding; if DFSB='VIL' then D13 is two's complemented.

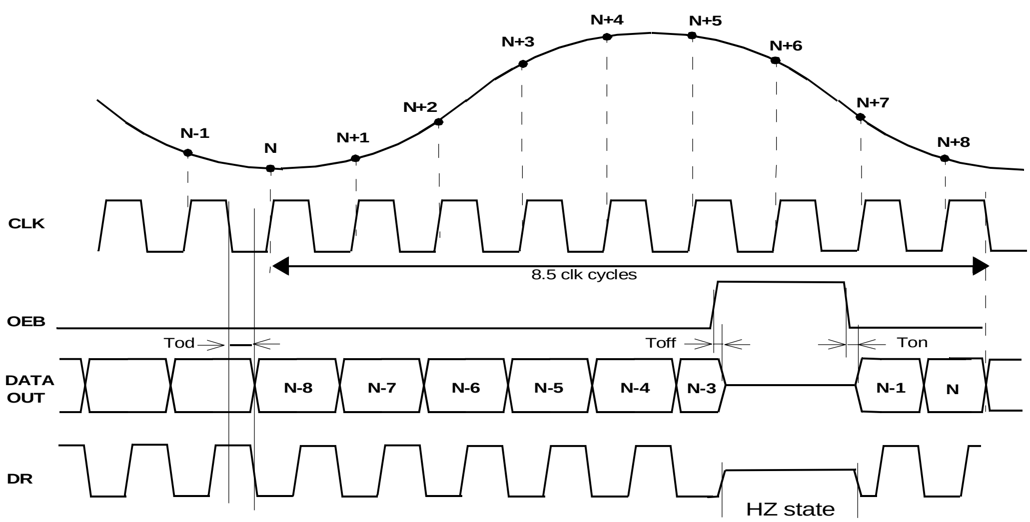
2 ELECTRICAL CHARACTERISTICS

AVCC = DVCC = VCCBI =VCCBE = 2.5V, Fs= 20MHz, Fin= 10MHz, VIN-VINB@ -1.0dBFS, VREFM= 0V, VREFP=1V, INCM=0.5V (external references), Tamb = 25°C (unless otherwise specified)

Timing Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FS	Sampling Frequency		0.5		20	MHz
DC	Clock Duty Cycle			50		%
TC1	Clock pulse width (high)			25		ns
TC2	Clock pulse width (low)			25		ns
Tod	Data Output Delay (Fall of Clock to Data Valid)	10pF load capacitance	6	7.5	11	ns
Tpd	Data Pipeline delay			8.5		cycles
Ton	Falling edge of OEB to digital output valid data			1		ns
Toff	Rising edge of OEB to digital output tri-state			1		ns

Timing Diagram



Dynamic Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR[1]	Spurious Free Dynamic Range	**Fin=10MHz, VREFP=1V**		**-89**	-74	dBFS
		Fin=10MHz, VREFP=1.24V (TS431)		-91.5		
		Fin=10MHz, internal references		-91		
SNR[1]	Signal to Noise Ratio	**Fin=10MHz, VREFP=1V**	68	**71.5**		dBc
		Fin=10MHz, VREFP=1.24V (TS431)		73.1		
		Fin=10MHz, internal references		70		
THD[1]	Total Harmonic Distortion	**Fin=10MHz, VREFP=1V**		**-85**	-71	dBc
		Fin=10MHz, VREFP=1.24V (TS431)		-85.9		
		Fin=10MHz, internal references		-86		
SINAD[1]	Signal to Noise and Distortion Ratio	**Fin=10MHz, VREFP=1V**	66	**71**		dBc
		Fin=10MHz, VREFP=1.24V (TS431)		72.85		
		Fin=10MHz, internal references		69.9		
ENOB[1]	Effective Number of Bits	**Fin=10MHz, VREFP=1V**	10.9	**11.7**		bits
		Fin=10MHz, VREFP=1.24V (TS431)		12		
		Fin=10MHz, internal references		11.5		

1) Typical values have been measured using the evaluation board on a dedicated test bench.

Accuracy

Symbol	Parameter	Min	Typ	Max	Unit
OE	Offset Error		-3		LSB
GE	Gain Error		0.04		%
DNL	Differential Non Linearity		±0.8		LSB
INL	Integral Non Linearity		±2		LSB
-	Monotonicity and no missing codes	Guaranteed			

Analog Inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIN-VINB	Analog Input Voltage, Differential			2		Vpp
Cin	Analog Input capacitance			4.0		pF
Zin	Analog Input impedance	Fs=20MHz		3.3		kΩ
BW	Analog Input Bandwidth (-3dB)	Full power, VIN-VINB=2.0Vpp, Fs=20MHz		1000		MHz

Internal Reference Voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
REFP	Top internal reference voltage		0.75	0.84	0.9	V
REFM	Bottom internal reference voltage			0		V
INCM	Internal common mode voltage		0.4	0.44	0.5	V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
RrefO	Reference output impedance	REFMODE='0': int references		18.7		Ω

External Reference Voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VREFP	Forced Top reference voltage	REFMODE='1'	0.8		1.3	V
VREFM	Bottom reference voltage		0		0.2	V
VINCM	Forced common mode voltage		0.4		1	V
RrefI	Reference input impedance			7.5		kΩ
Vpol	Analog bias voltage	REFMODE='1'	1.22	1.27	1.34	V

Power Consumption

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ICCA	Analog Supply current	REFMODE='0' REFMODE='1'		40 30	 37	mA
ICCD	Digital Supply Current			595	700	µA
ICCBI	Digital Buffer Supply Current			1	1.5	mA
ICCBE	Digital Buffer Supply Current			2.3	6	mA
ICCBEZ	Digital Buffer Supply Current in High Impedance Mode			10	150	µA
Pd	Power consumption in normal operation mode	REFMODE='0' REFMODE='1'		110 85[1]	 110	mW
PdZ	Power consumption in High Impedance mode	REFMODE='0' REFMODE='1'		104 79[1]	 96	mW
Rthja	Thermal resistance (TQFP48)			80		°C/W

1) Typical values have been measured using the evaluation board on a dedicated test bench.

Digital Inputs and Outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock inputs						
VIL	Logic "0" voltage	DVCC=2.5V			0.8	V
VIH	Logic "1" voltage		2.0			V
IIL	Low input current			TBD		µA
IIH	High input current			TBD		µA
Digital inputs						
VIL	Logic "0" voltage	VCCBE=2.5V			0.25 VCCBE	V
VIH	Logic "1" voltage		0.75 VCCBE			V
IIL	Low input current			TBD		µA
IIH	High input current			TBD		µA
Digital Outputs						
VOL	Logic "0" voltage	VCCBE=2.5V, Iol=10µA			0.1	V
VOH	Logic "1" voltage	VCCBE=2.5V, Ioh=10µA	2.45			V

3 DEFINITIONS OF SPECIFIED PARAMETERS

3.1 Static Parameters

Static measurements are performed through the method of histograms on a 2MHz input signal, sampled at 20Msps, which is high enough to fully characterize the test frequency response. An input level of +1dBFS is used to saturate the signal.

Differential Non Linearity (DNL)

The average deviation of any output code width from the ideal code width of 1LSB.

Integral Non linearity (INL)

An ideal converter presents a transfer function as being the straight line from the starting code to the ending code. The INL is the deviation for each transition from this ideal curve.

3.2 Dynamic Parameters

Dynamic measurements are performed by spectral analysis, applied to an input sine wave of various frequencies and sampled at 20Msps.

Spurious Free Dynamic Range (SFDR)

The ratio between the amplitude of fundamental tone (signal power) and the power of the worst spurious signal (not always an harmonic) over the full Nyquist band. It is expressed in dBc.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to Noise Ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($F_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to Noise and Distortion Ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula:

$SINAD = 6.02 \times ENOB + 1.76$ dB.

When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$SINAD = 6.02 \times ENOB + 1.76 \text{ dB} + 20 \log (2A_0/FS)$

The ENOB is expressed in bits.

Analog Input Bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3dB. Higher values can be achieved with smaller input levels.

Effective Resolution Bandwidth (ERB)

The band of input signal frequencies that the ADC is intended to convert without loosing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output, on the output bus. Also called data latency. It is expressed as a number of clock cycles.

4 TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1: Linearity vs. Fin, Internal References
Fs=20MHz; Icca=40mA

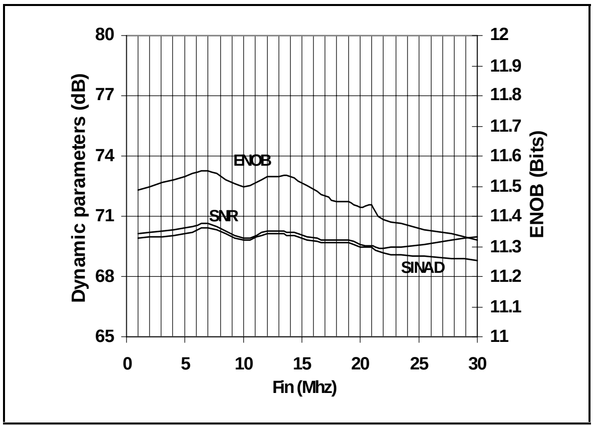


Fig. 2: Distortion vs. Fin, Internal References
Fs=20MHz; Icca=40mA; Internal references

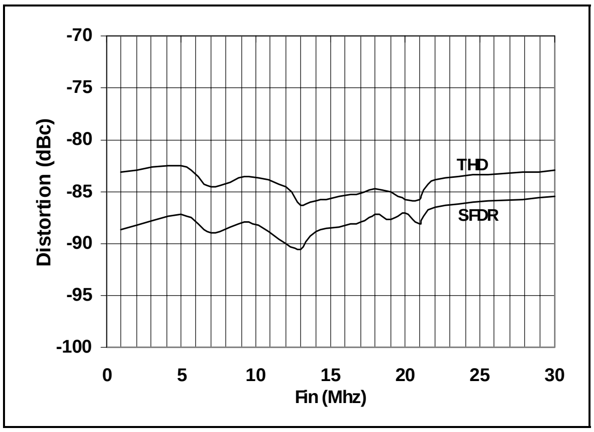


Fig. 3: 2nd. and 3rd. harmonic vs. Fin, Internal References, Fs=20MHz; Icca=40mA

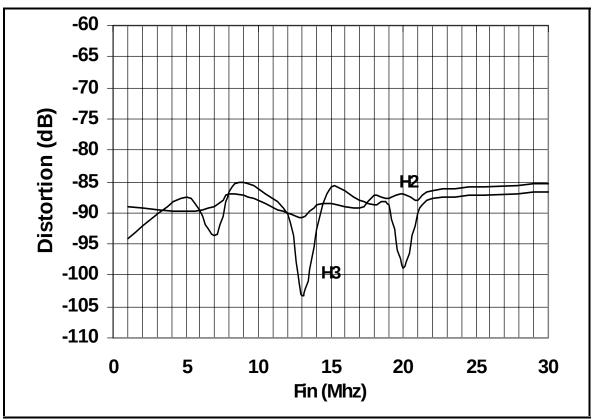


Fig. 4: Linearity vs. Fin, External References (REFP=1V) Fs=20MHz; Icca=28mA

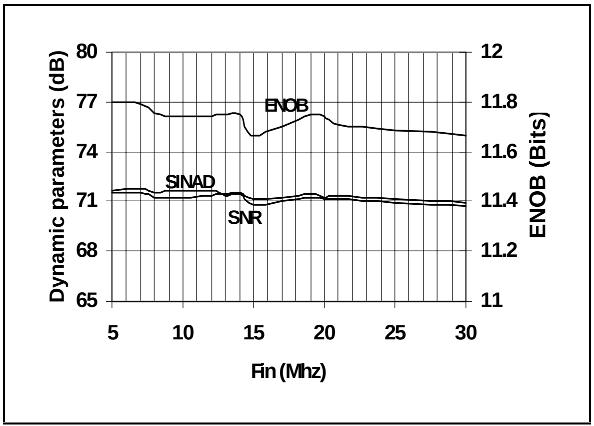


Fig. 5: Distortion vs. Fin, External References (RefP=1V) Fs=20MHz; Icca=28mA

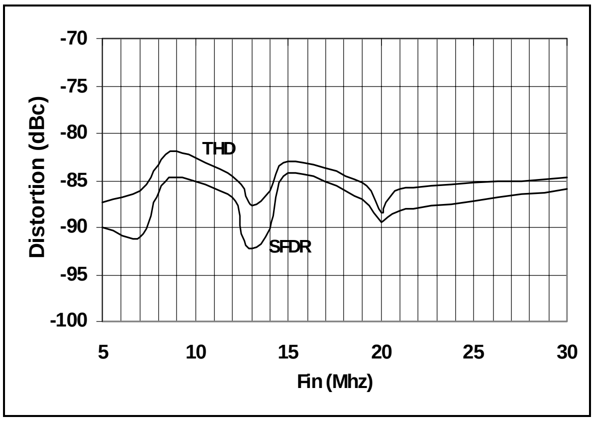


Fig. 6: 2nd. and 3rd. harmonic vs. Fin, External References (REFP=1V) Fs=20MHz; Icca=28mA

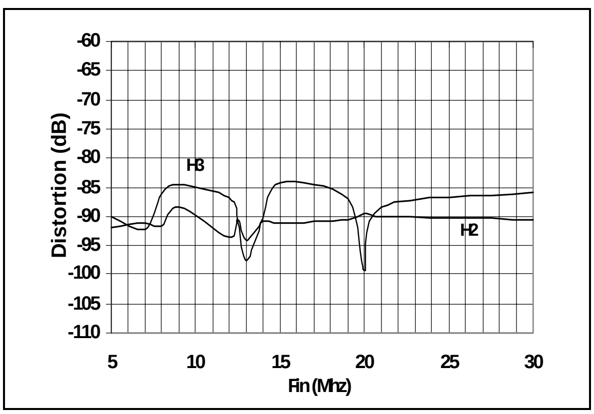


Fig. 7: SFDR vs. input amplitude (FS=2x0.86V)

Fs=20Msps; Fin=5Mhz;Icca=40mA,

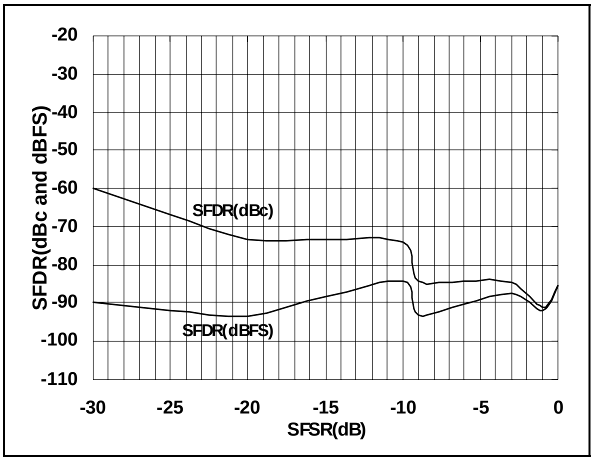


Fig. 8: Single-tone 16K FFT at Fs=20 Msps, Internal references

Fin=5MHz, Icca=40mA,Vin@-1dBFS, SFDR=-89.3dBc, THD=-84.5dBc, SNR=70.5dB, SINAD=70.3dB, ENOB=11.5 bits

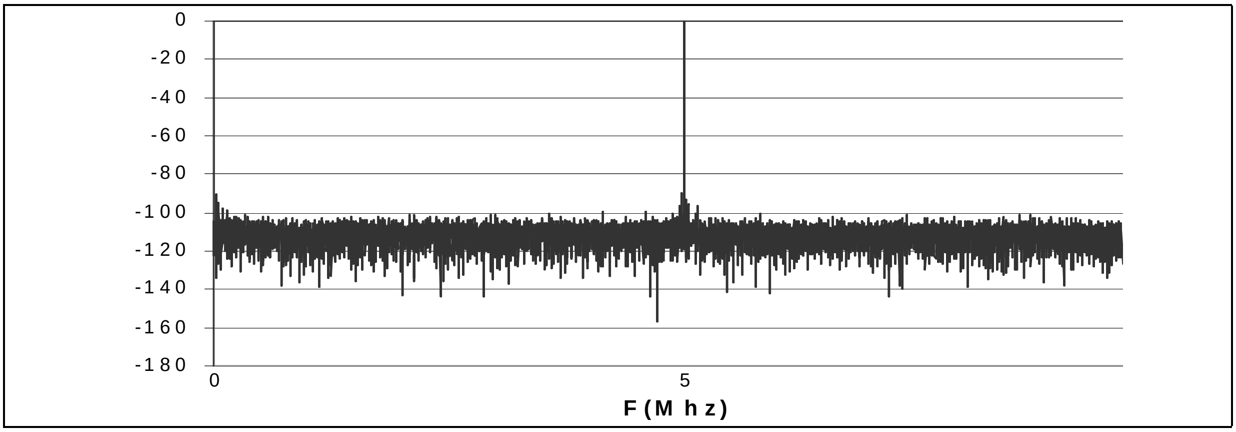
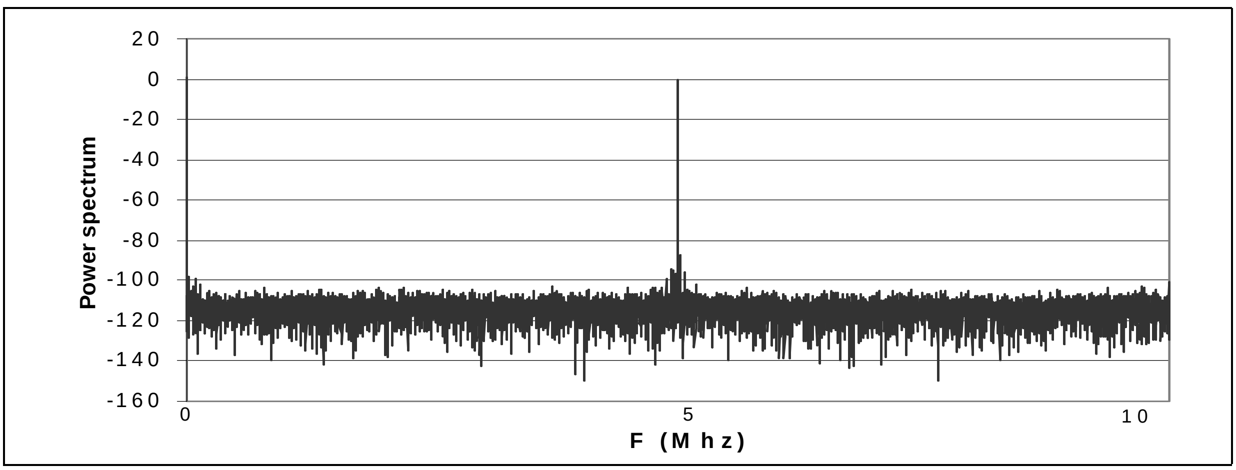
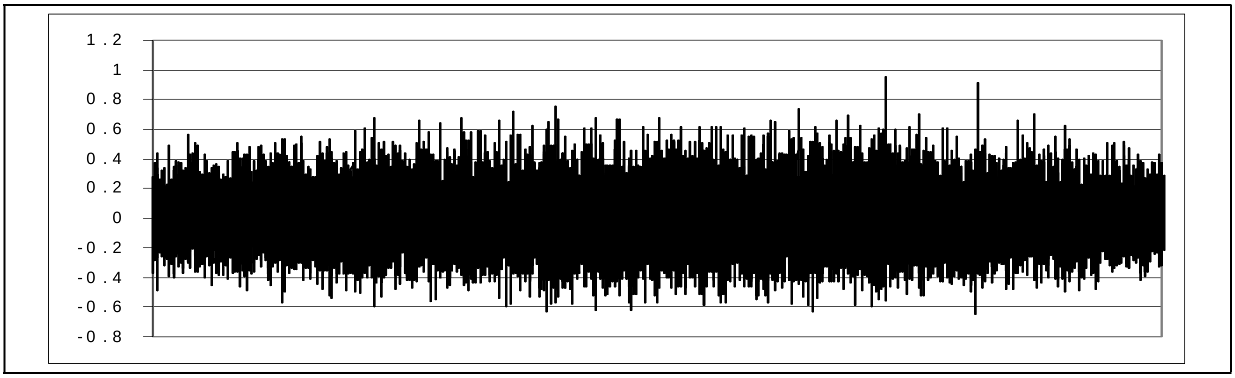


Fig. 9: Single-tone 16K FFT at Fs=20Msps, External References TS4041

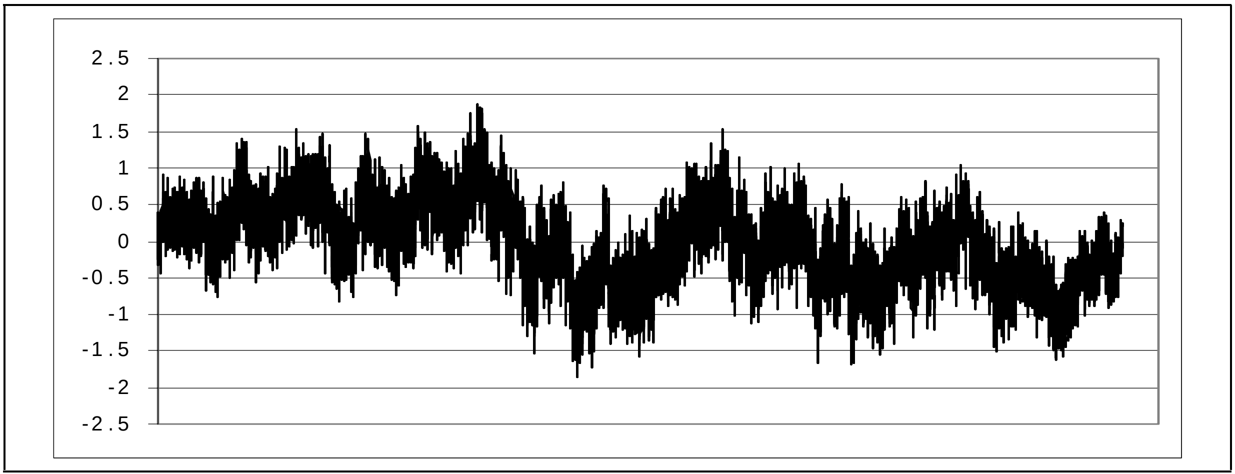
Fin=5MHz, Icca=40mA, Vin@-1dBFS, VREFP=1.225V
SFDR=-87.5dBc, THD=-85.4dBc, SNR=73.3dB, SINAD=73dB, ENOB=11.84 bits



Static parameter: Differential Non Linearity
Fs=20MSPS; Fin=1MHz; Icc=40mA;N=524288pts



Static parameter: Integral Non Linearity
Fs=20MSPS; Fin=1MHz; Icc=40mA; N=524288pts



5 APPLICATION INFORMATION

The TSA1401 is a High Speed Analog to Digital converter based on a pipeline architecture and the latest deep sub micron CMOS process to achieve the best performances in terms of linearity and power consumption.

The pipeline structure consists of 14 internal conversion stages in which the analog signal is fed and sequentially converted into digital data.

Each of the 14 stages consists of an Analog to Digital converter, a Digital to Analog converter, a Sample and Hold and an amplifier (gain=2). A 1.5-bit conversion resolution is achieved in each stage. Each resulting LSB-MSB couple is then time-shifted to recover from the delay caused by conversion. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple for each stage. The corrected data are outputted through the digital buffers.

Signal input is sampled on the rising edge of the clock while digital outputs are delivered on the falling edge of the clock.

The advantages of such a converter reside in the combination of pipeline architecture and the most advanced technologies. The highest dynamic performances are achieved while consumption remains at the lowest level.

5.1 Analog Input Configuration

5.1.1 Analog input level and references

To maximize the TSA1401's high-resolution and speed, it is advisable to drive the analog input differentially. The full scale of TSA1401 is adjusted through the voltage value of VREFP and VREFM:

VIN-VINB=2(VREFP-VREFM)

The differential analog input signal always presents a common mode voltage, CM:

CM=(VIN+VINB)/2

In order for the user to select the right full scale according to the application, a control pin, REFMODE, allows to switch from internal to external references.

Internal references, common mode:

When REFMODE is set to VIL level, TSA1401 operates with its own reference voltage generated by its internal bandgap. VREFM pin is connected externally to the Analog Ground while VREFP is set to its internal voltage (0.86V). The full scale of the ADC when using internal references is 1.8Vpp (to reduce the full scale if desired, VREFM may be forced externally).

In this case VREFP and INCM are low impedance outputs. INCM pin (voltage generator 0.46V) may be used to supply the common mode, CM of the analog input signal.

External references, common mode:

In applications requiring a different full scale magnitude, it is possible to force externally VREFP and INCM (REFM must be connected to analog ground or forced externally).

REFMODE set to VIH level will put in standby mode the internal references. In this case, VREFP, INCM are high impedance inputs and have to be forced by external references. TSA1401 shows better performances when the full scale is increased by the use of external references (see *Figure 10* and *11*).

Fig. 10: Linearity vs. VREFP

Fin=5MHz;Fs=20Mhz;Icca=26mA;INCM=0.45V

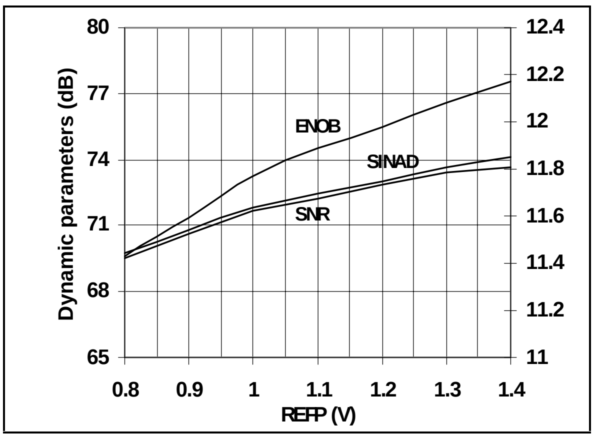
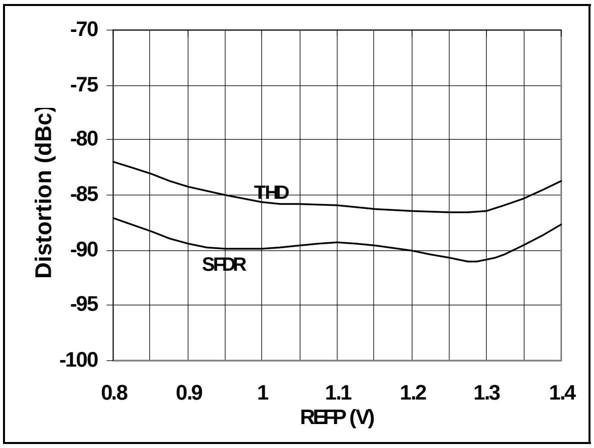


Fig. 11: Distortion vs. VREFP

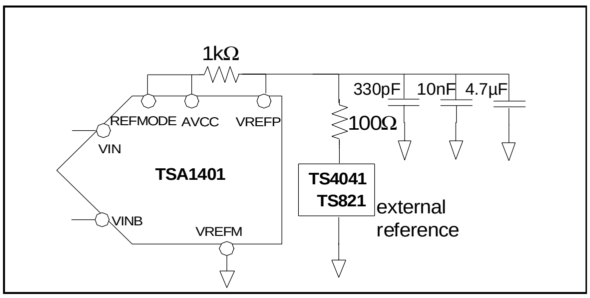
Fin=5MHz;Fs=20Mhz;Icca=26mA;INCM=0.46V



An external reference voltage device may be used for specific applications requiring even better linearity, accuracy or enhanced temperature behavior.

Using the STMicroelectronics TS821, TS4041-1.2 or TS431 Voltage Reference devices leads to optimum performances when configured as shown in *Figure 12*. The full scale is increased to 2.5Vpp differential and SNR and SINAD are enhanced as shown in *Figure 13* .

Fig. 12: External reference setting



In multi-channel applications, the high impedance input of the references permits to drive several ADCs with only one Voltage Reference device.

Fig. 13: Linearity vs. Fs at Fin=5MHz, using TS4041 Icca optimised; VREFP=1.225V; VREFM=GND; INCM=0.65V,

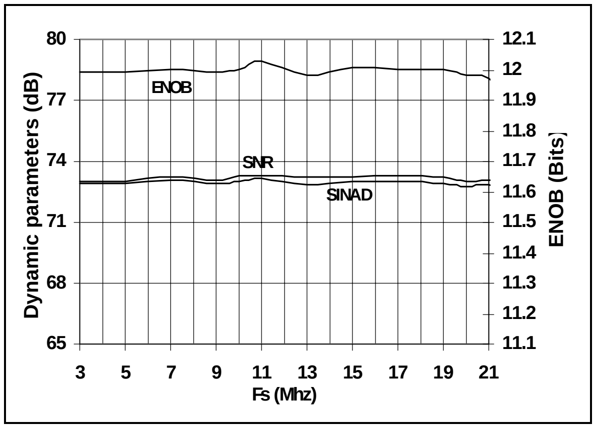
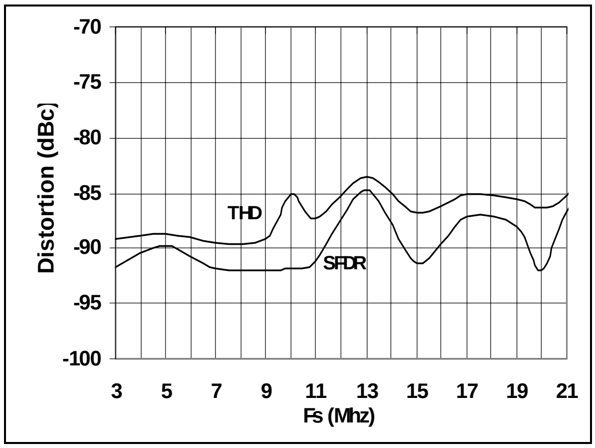


Fig. 14: Distortion vs. Fs at Fin=5MHz, using TS4041 Icca optimised; VREFP=1.225V; VREFM=GND; INCM=0.65V



The magnitude of the analog input common mode, CM should stay close to VREFP/2. Higher level will introduce more distortion.

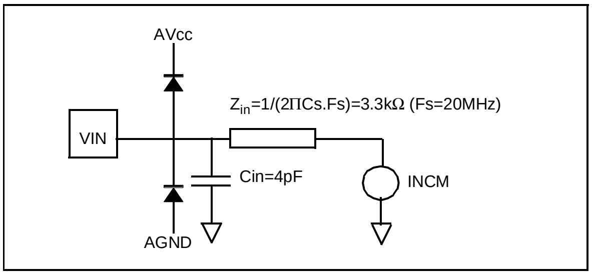
5.1.2 - Driving the analog input

The TSA1401 has been designed to be differentially driven for better noise immunity. Some measurements have been done with single-ended signals. It degrades a little bit the performances, with an SFDR of -75dBc and an ENOB of 11.2 bits at 20Msps, Fin at 10MHz.

The switch-capacitor input structure of TSA1401, presents a high input impedance (3.3kΩ at Fs=20MHz) but not constant in time (see equivalent input circuit *Figure 15*). Indeed at the end of each conversion, the charge update of the sampling capacitor will draw/inject a small current transient on the input signal.

One method to mask this transient current is a low-pass RC filter as shown on *Figures 16* and *Figure 17*. A larger capacitor value compared to the sampling capacitor (appoximately 2pF) mounted in parallel of the two analog inputs signals will absorb the transient glitches.

Fig. 15: ADC input equivalent circuit

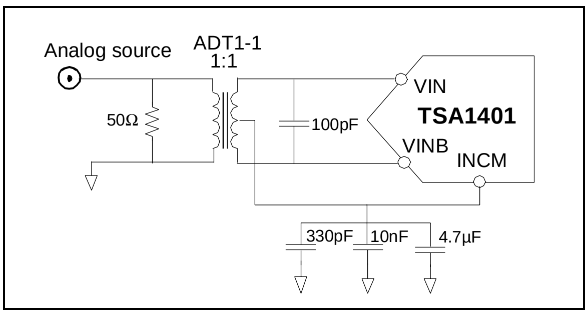


Single-ended signal with transformer:

Using an RF transformer is a good means to achieve high performance.

Figures 16 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs.

Fig. 16: Differential input configuration with transformer

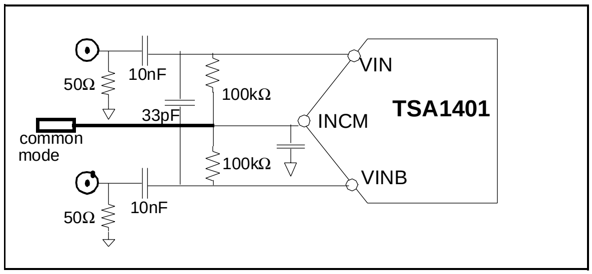


The internal common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.46V. The INCM is decoupled to maintain a low noise level on this node.

AC coupled differential input:

Figure 17 represents the biasing of a differential input signal in AC-coupled differential input configuration. Both inputs VIN and VINB are centered around the common mode voltage CM, that can be forced through INCM or supplied externally (in this case the internal common mode of the TSA1401 may be left internal at 0.45V, different from the input common mode value).

Fig. 17: AC-coupled differential input



5.2 - Clock management

The converter performances are very dependant on clock input accuracy, in terms of aperture delay and jitter. The voltage error induced by the jitter of the clock is:

$V_{error}=SR.T_j$,

where T_j is the jitter of the clock (system clock and ADC) and,

SR is the slew rate of the input signal:

SR max=$2\Pi.F_{in}.FS$ (FS full scale, F_{in} input signal frequency)

V_{error} should be less than an LSB to guarantee no missing codes. At the end we have:

$V_{error}=2\Pi.F_{in}.FS.T_j$ and $Verror< FS/2^n$

$T_j <FS/(2\Pi.Fs.F_{in}.2^n)$.

For TSA1401 at 10MHz input frequency, we have

T_j <1ps. Consequently to target the maximum performances of the TSA1401, the clock applied should have a jitter below 1ps.

The clock power supplies must be separated from the ADC output ones to avoid digital noise modulation at the output.

It is strongly advised not to switch off the clock when the circuit is active (power supply on).

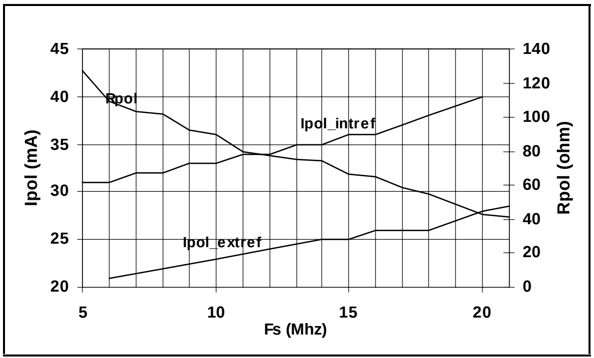
5.3 - Power consumption optimization

The internal architecture of the TSA1401 enables the optimization of the power consumption according to the sampling frequency of the application. For this purpose, a resistor (value Rpol) is placed between IPOL and the analog Ground pins. At 20MHz sampling frequency, the Rpol for optimized consumption is equal to 41kΩ.

Optimized power consumption of the circuit versus the sampling frequency are shown in two configurations (*Figure 18*):

- REFMODE=0 internal references
- REFMODE=1 external references

Fig. 18: Analog Current consumption vs. Fs
According value of Rpol polarization resistances: internal references



5.4 - Digital outputs

Data Format Select (DFSB)

When set to low level (VIL), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing.

When set to high level (VIH), DFSB provides a standard binary output coding.

Output Enable (OEB)

When set to low level (VIL), all digital outputs remain active and are in low impedance state. When set to high level (VIH), all digital outputs buffers are in high impedance state. It results in lower consumption while the converter goes on sampling.

When OEB is set to low level again, the data is then valid on the output with a very short Ton delay(1ns).

The timing diagram page 4 summarizes this operating cycle.

Out of Range (OR)

This function is implemented on the output stage in order to set up an "Out of Range" flag whenever the digital data is over the full scale range.

Typically, there is a detection of all the data being at '0' or all the data being at '1'. This ends up with an output signal OR which is in low level state (VOL) when the data stay within the range, or in high level state (VOH) when the data are out of the range.

Data Ready (DR)

The Data Ready output is an image of the clock being synchronized on the output data (D0 to D13). This is a very helpful signal that simplifies the synchronization of the measurement equipment or the controlling DSP.

As digital output, DR goes in high impedance state when OEB is asserted to High level as described in the timing diagram page 4.

5.5 - Layout precautions

To use the TSA1401 circuit in the best manner at high frequencies, some precautions have to be taken for power supplies:

- The separation of the analog signal from the digital part and from the buffers power supply is essential to prevent noise from coupling onto the input signal.

- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.

- Proper termination of all inputs and outputs is needed; with output termination resistors, the amplifier load will be only resistive and the stability of the amplifier will be improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.

- To keep the capacitive loading as low as possible at digital outputs, short lead lengths when routing are essential to minimize currents when the output changes. To minimize this output capacitance, buffers or latches close to the output pins can relax this constraint. It is also helpful to use 47 to 56 ohms series resistors at the ADC output pins, located as close to the ADC output pins as possible.

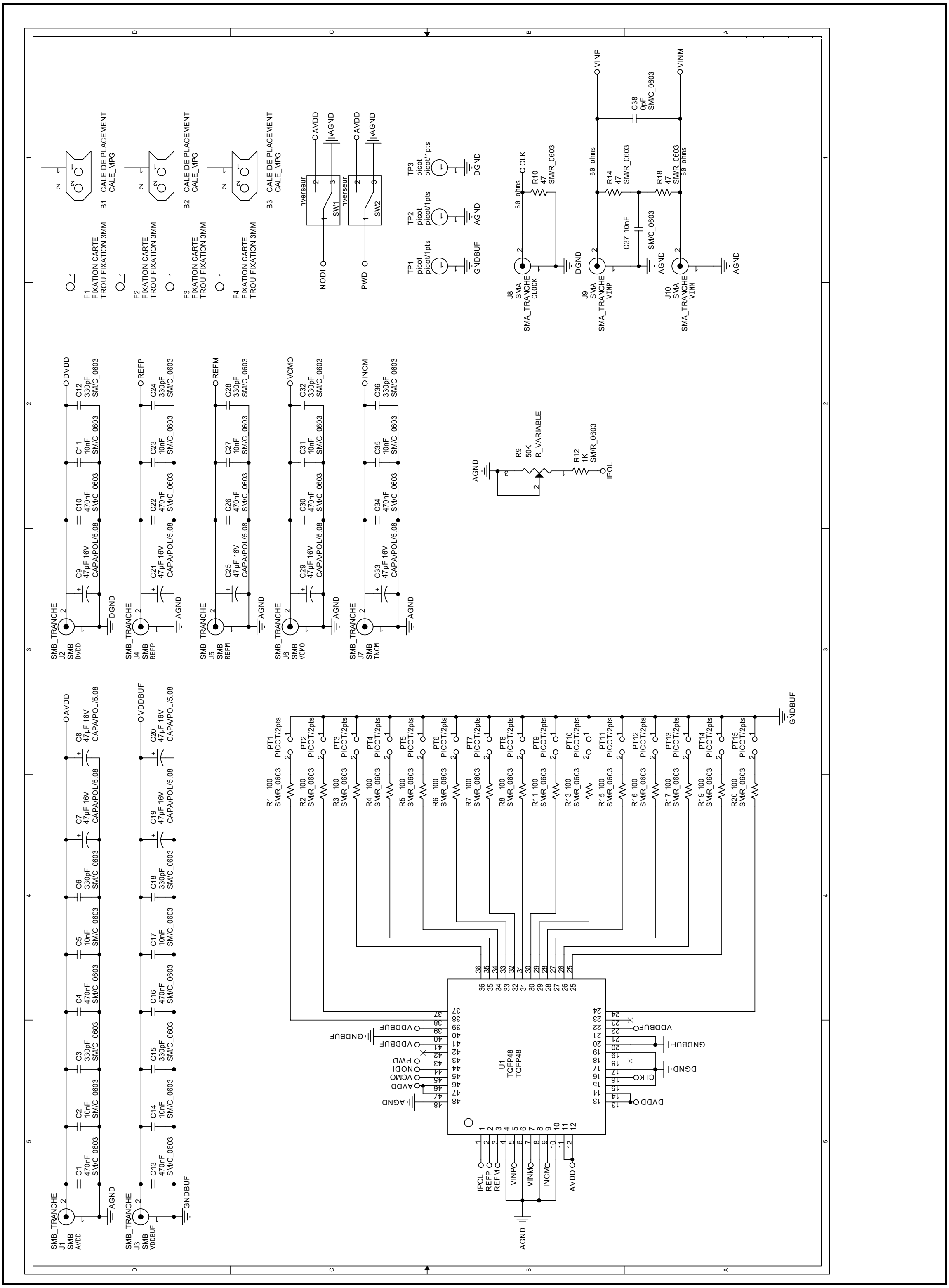
- Choose component sizes as small as possible (SMD).

EVAL1401 evaluation board

The characterization of the board has been made with a fully ADC devoted test bench.
The schematic of the evaluation board is shown on figure 19. The analog signal must be filtered to be very pure.
The dataready signal is the acquisition clock of the logic analyzer.

All characterization measurement has been made with an input amplitude of +0.2dB for static parameters and -0.5dB for dynamic parameters

Fig. 19: TSA1401 Evaluation board schematic



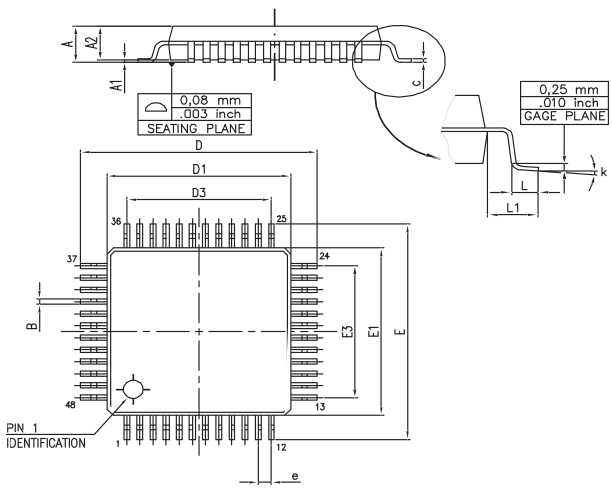
Printed circuit board - List of components

Reference	Part	PCB Footprint
B1,B2,B3	CALE DE PLACEMENT	CALE_MPG
C1,C4,C10,C13,C16,C22, C26,C30,C34	470nF	SM/C_0603
C2,C5,C11,C14,C17,C23, C27,C31,C35,C37	10nF	SM/C_0603
C3,C6,C12,C15,C18,C24, C28,C32,C36	330pF	SM/C_0603
C7,C8,C9,C19,C20,C21,C25, C29,C33	100µF 16V	CAPA/POL/5.08
C38	0pF	SM/C_0603
J1,J2,J3,J4,J5,J6,J7	SMB	SMB_TRANCHE
J8,J9,J10	SMA	SMA_TRANCHE
PT1,PT2,PT3,PT4,PT5,PT6, PT7,PT8,PT9,PT10,PT11, PT12,PT13,PT14,PT15	picot	PICOT/2pts
R1,R2,R3,R4,R5,R6,R7,R8, R11,R13,R15,R16,R17,R19, R20	100	SM/R_0603
R9	200K	R_VARIABLE
R10,R14,R18	49.9	SM/R_0603
R12	1K	SM/R_0603
SW1,SW2	micro switch 1	inverseur
TP1,TP2,TP3	picot	picot/1pts

6 PACKAGE MECHANICAL DATA

TQFP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.0035		0.0079
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.020	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°



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