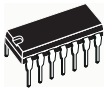
TS274

High performance CMOS quad ooperational amplifiers

- Output voltage can swing to ground
- Excellent phase margin on capacitive loads
- Gain bandwidth product: 3.5MHz
- Stable and low offset voltage
- Three input offset voltage selections

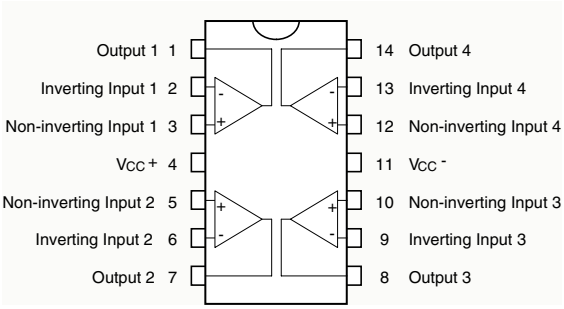


N
DIP-14
(Plastic Package)

D
SO-14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

Pin connections (top view)



Description

The TS274 devices are low cost, quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the ST silicon gate CMOS process allowing an excellent consumption-speed ration. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio:

- I_{CC} = 10µA/amp.: TS27L4 (very low power)
- I_{CC} = 150µA/amp.: TS27M4 (low power)
- I_{CC} = 1mA/amp.: TS274 (standard)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

1 Order codes

Part Number	Temperature Range	Package	Packing	Marking
TS274CD/DT	0°C, +70°C	SO-14	Tube or Tape & Reel	274C
TS274ACD/DT				274AC
TS274CN		DIP 14	Tube	TS274CN
TS274ACN				TS274ACN
TS274CPT		TSSOP 14	Tape & Reel	
TS274ACPT				
TS274ID/DT	-40°C, +125°C	SO-14	Tube or Tape & Reel	274I
TS274AID/DT				274AI
TS274IN		DIP 14	Tube	TS274IN
TS274AIN				TS274AIN
TS274IPT		TSSOP-14	Tape & Reel	
TS274AIPT				

2 Absolute maximum ratings & operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	TS274C/AC/BC	TS274I/AI/BI	Unit
V_{CC}^+	Supply Voltage (1)	18		V
Vid	Differential Input Voltage (2)	±18		V
V_i	Input Voltage (3)	-0.3 to 18		V
I_o	Output Current for $V_{CC}^+ \geq 15V$	±30		mA
I_{in}	Input Current	±5		mA
T_{oper}	Operating Free-Air Temperature Range	0 to +70	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150		°C
R_{thja}	Thermal Resistance Junction to Ambient(4) SO-14 TSSOP14 DIP14	 103 100 80		°C/W
R_{thjc}	Thermal Resistance Junction to Case SO-14 TSSOP14 DIP14	 31 32 33		°C/W
ESD	HBM: Human Body Model(5)	500		V
	MM: Machine Model(6)	100		V
	CDM: Charged Device Model	800		V

1. All values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
5. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
6. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ - 1.5	V

3 Typical application information

Figure 1. Block diagram

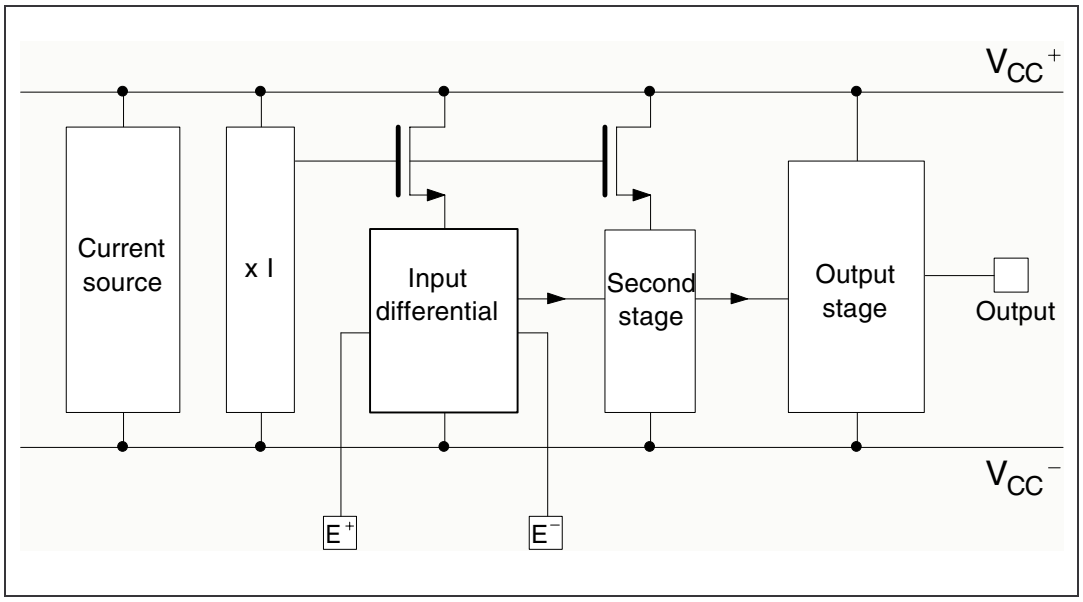
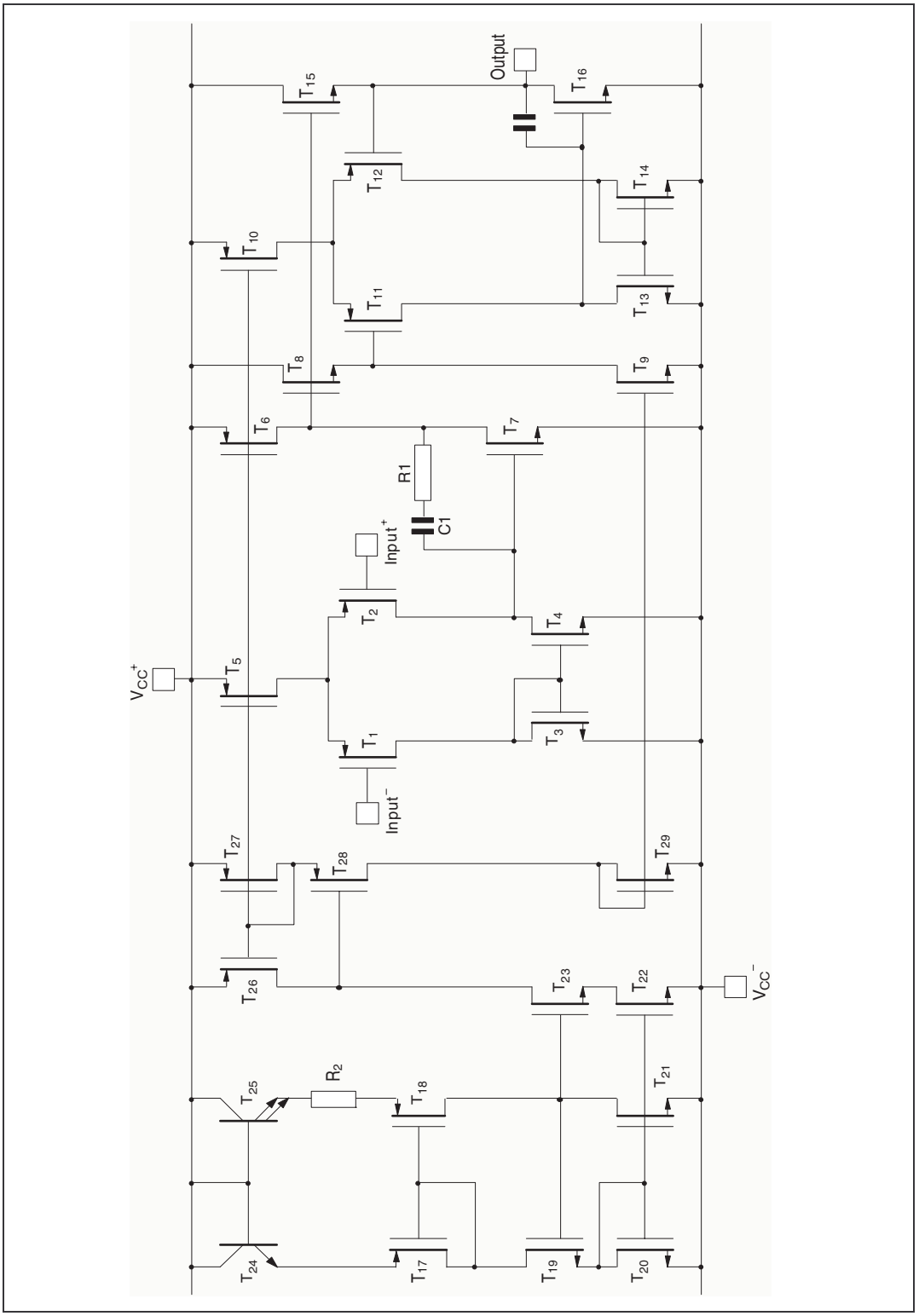


Figure 2. Schematic diagram (for 1/4 TS274)



4 Electrical characteristics

Table 3. V_{CC}^+ = +10V, V_{CC}^-= 0V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Conditions	TS274C/AC/BC			TS274I/AI/BI			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{io}	Input Offset Voltage	V_O = 1.4V, V_{ic} = 0V TS274C/I TS274AC/AI TS274B/C/I		 1.1 0.9 0.25	 10 5 2		 1.1 0.9 0.25	 10 5 2	mV
		$T_{min} \le T_{amb} \le T_{max}$ TS274C/I TS274AC/AI TS274B/C/I			 12 6.5 3			 12 6.5 3.5	
DV_{io}	Input Offset Voltage Drift			2			2		µV/°C
I_{io}	Input Offset Current (1)	V_{ic} = 5V, V_O = 5V $T_{min} \le T_{amb} \le T_{max}$		1	 100		1	 200	pA
I_{ib}	Input Bias Current (1)	V_{ic} = 5V, V_O = 5V $T_{min} \le T_{amb} \le T_{max}$		1	 150		1	 300	pA
V_{OH}	High Level Output Voltage	V_{id} = 100mV, R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	Low Level Output Voltage	V_{id} = -100mV			50			50	mV
A_{vd}	Large Signal Voltage Gain	V_{iC} = 5V, R_L = 10kΩ, V_o = 1V to 6V $T_{min} \le T_{amb} \le T_{max}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product	A_v = 40dB, R_L = 10kΩ, C_L = 100pF, f_{in} = 100kHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio	V_{iC} = 1V to 7.4V, V_o = 1.4V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio	V_{CC}^+ = 5V to 10V, V_o = 1.4V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier)	A_v = 1, no load, V_o = 5V $T_{min} \le T_{amb} \le T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_o	Output Short Circuit Current	V_o = 0V, V_{id} = 100mV		60			60		mA
I_{sink}	Output Sink Current	V_o = V_{CC}, V_{id} = -100mV		45			45		mA
SR	Slew Rate at Unity Gain	R_L = 10kΩ, C_L = 100pF, V_i = 3 to 7V		5.5			5.5		V/µs
ϕm	Phase Margin at Unity Gain	A_v = 40dB, R_L = 10kΩ, C_L = 100pF		40			40		Degrees
K_{OV}	Overshoot Factor			30			30		%
e_n	Equivalent Input Noise Voltage	f = 1kHz, R_s = 100Ω		30			30		nV/√Hz
V_{o1}/V_{o2}	Channel Separation			120			120		dB

1. Maximum values including unavoidable inaccuracies of the industrial test.

Figure 3. Supply current (each amplifier) vs. supply voltage

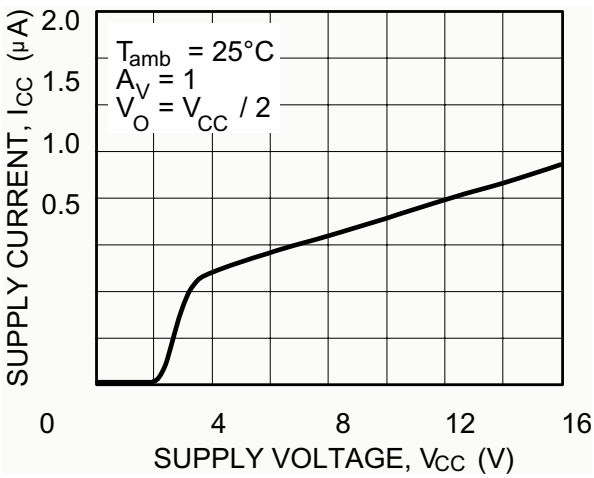


Figure 4. High level output voltage vs. high level output current

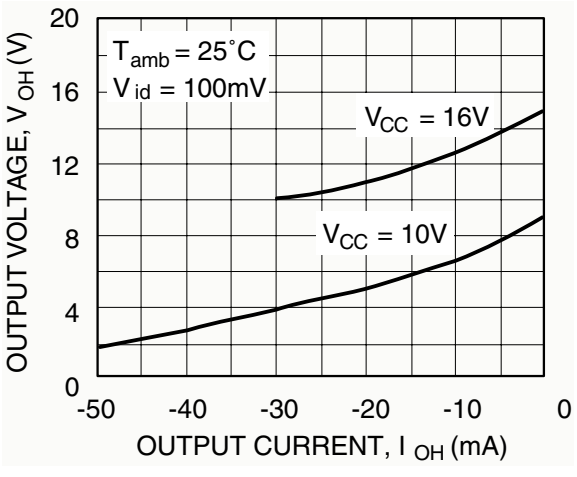


Figure 5. Input bias current vs. free-air temperature

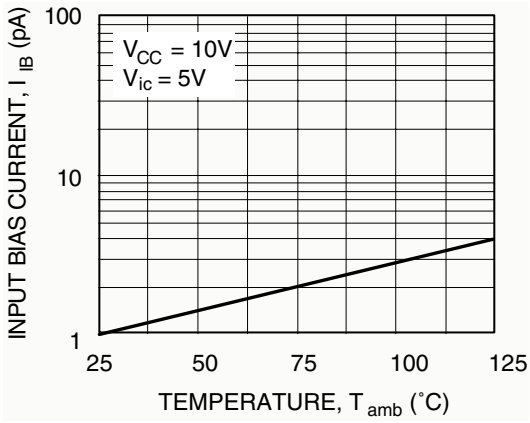


Figure 6. Low level output voltage vs. low level output current

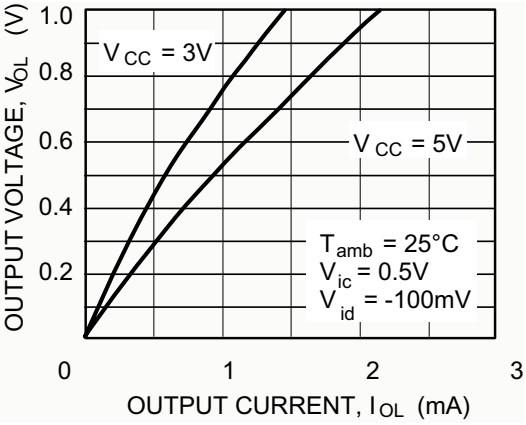


Figure 7. High level output voltage vs. high level output current

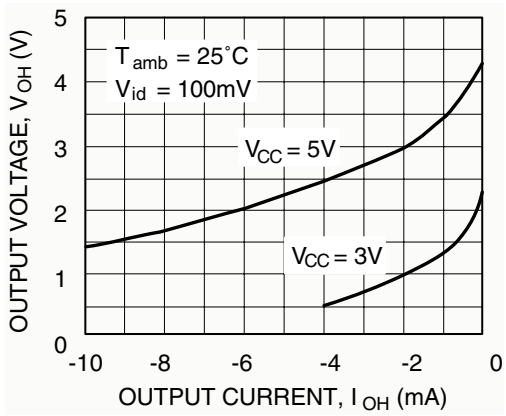


Figure 8. Low level output voltage vs. low level output current

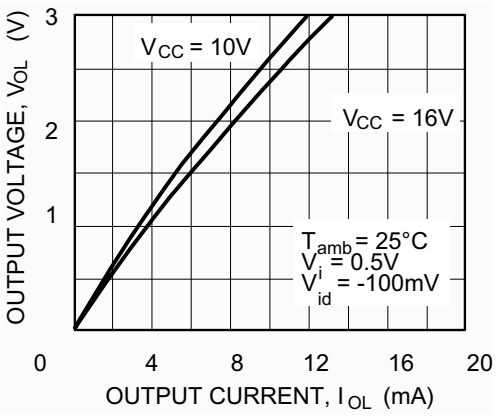


Figure 9. Open loop frequency response and phase shift

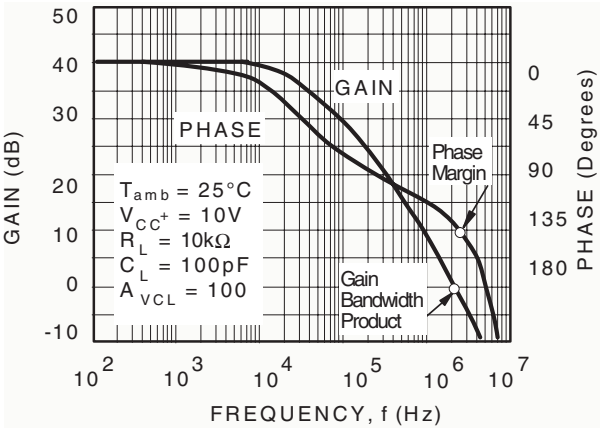


Figure 10. Phase margin vs. capacitive load

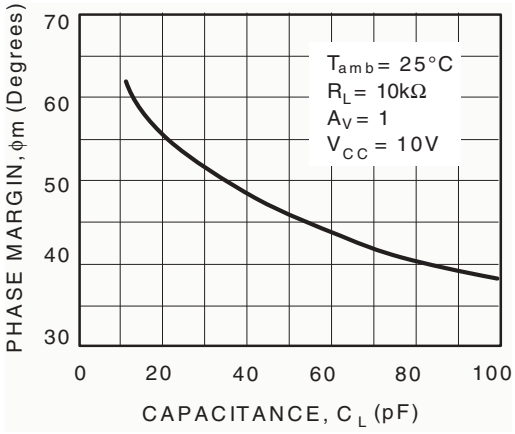


Figure 11. Gain bandwidth product vs. supply voltage

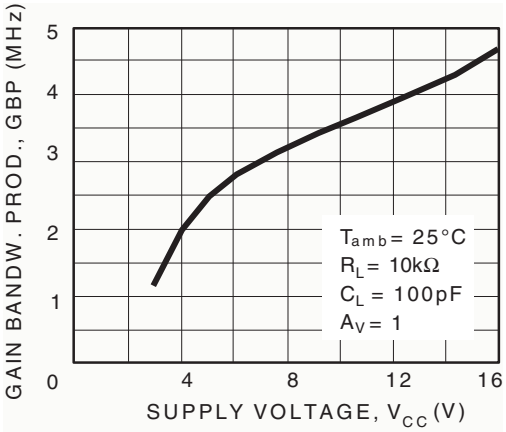


Figure 12. Slew rate vs. supply voltage

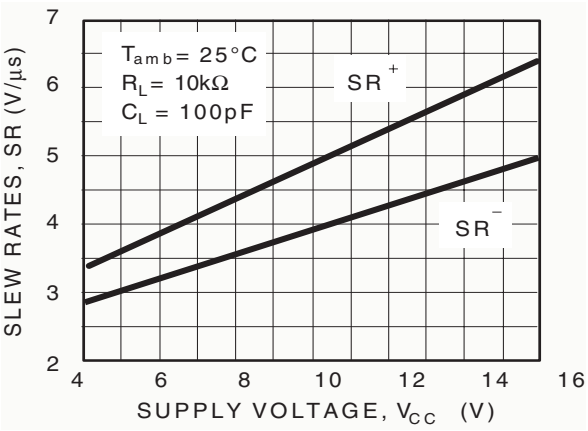


Figure 13. Phase margin vs. supply voltage

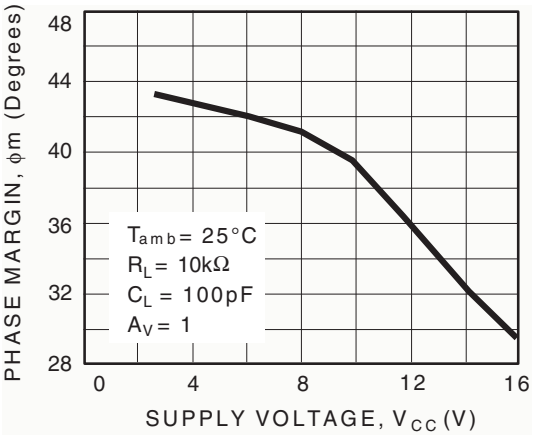
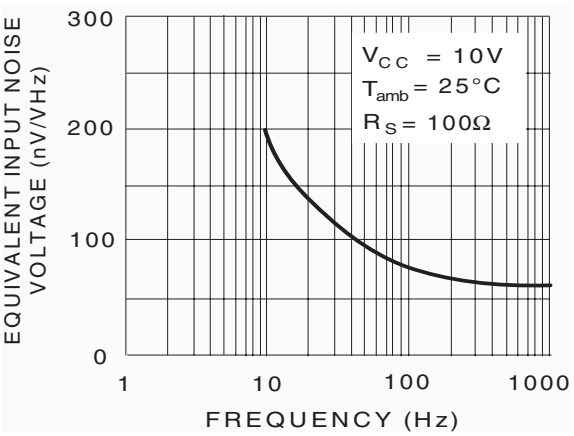


Figure 14. Input voltage noise vs. frequency



5 Macromodel

5.1 Important note concerning this macromodel

Please consider following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.

Data issued from macromodels used outside of its specified conditions (V_{CC}, Temperature, etc.) or even worse: outside of the device operating conditions (V_{CC}, Vicm, etc.) are not reliable in any way.

5.2 Macromodel code

```
********************************
.SUBCKT TS27X 1 2 3 4 5
*** INP- = 1, INP+ =2, OUT = 3 VDD=4 VSS = 5
*** TYPE = TS271/TS272/TS274
.MODEL MDTH D IS=1E-8 KF=2.664E-16 CJO=10F
***INPUT STAGE
CIP 2 5 1E-12
CIN 1 5 1E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8
RIN 15 16 8
RIS 11 15 223.84
CPS 11 15 1E-9
DIP 11 120 MDTH 400E-12
DIN 15 140 MDTH 400E-12
RDEG1 12 120 4400
RDEG2 14 140 4400
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 38E-6
***ICC
DICC1 4 31 MDTH 400E-12
DICC2 31 32 MDTH 400E-12
DICC3 32 33 MDTH 400E-12
DICC4 33 34 MDTH 400E-12
RICC 34 5 20E3
ICC 4 5 600E-6
***COMMON MODE INPUT LIMITATION
DINN 17 13 MDTH 400E-12
VIN 17 5 DC -0.1
DINR 15 18 MDTH 400E-12
VIP 4 18 DC 2.2
***GM1 STAGE
FGM1P 119 5 VOFP 1
FGM1N 119 5 VOFN 1
RAP 119 4 1E6
```

```
RAN 119 5 1E6
***GM2 STAGE
G2P 19 5 119 5 4E-4
G2N 19 5 119 4 4E-4
R2P 19 4 450E3
R2N 19 5 450E3
***COMPENSATION
CC 19 119 7p
***BUFFER
EBUF 20 5 19 5 1
***SHORT-CIRCUIT LIMITATIONS( ISINK, ISOURCE)
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 910
VIPM 28 4 DC 50
HONM 21 27 VOUT 1222
VINM 5 27 DC 50
VOUT 3 23 DC 0
***VOH, VOL DEFINITIONS
DOP 19 25 MDTH 400E-12
VOP 4 25 2.5
DON 24 19 MDTH 400E-12
VON 24 5 0.92
***OUTPUT RESISTOR
ROUT 23 20 10
.ENDS
```

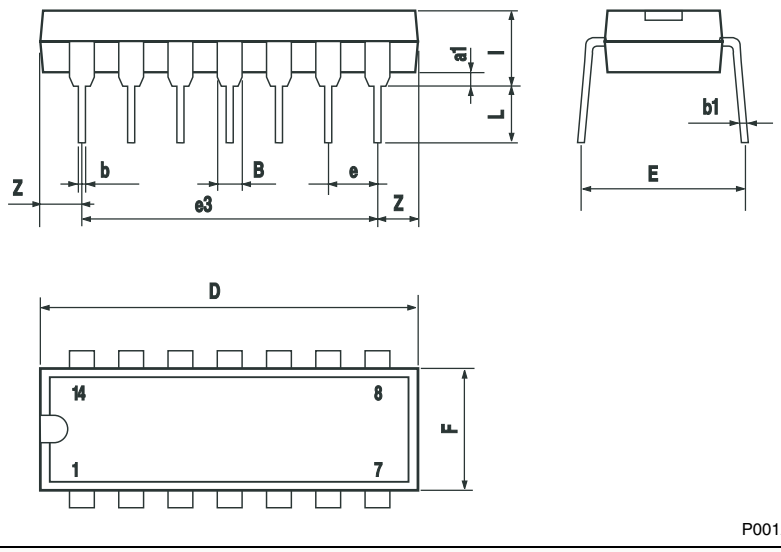
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP14 package

Plastic DIP-14 MECHANICAL DATA

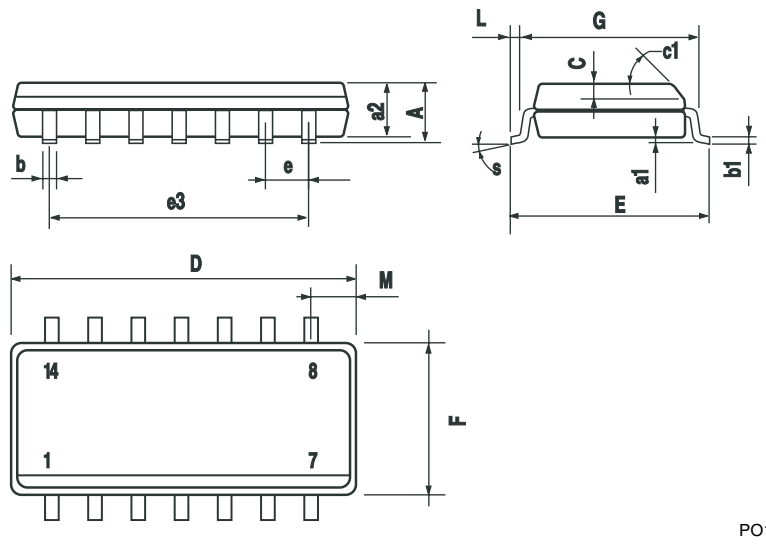
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



6.2 SO-14 package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

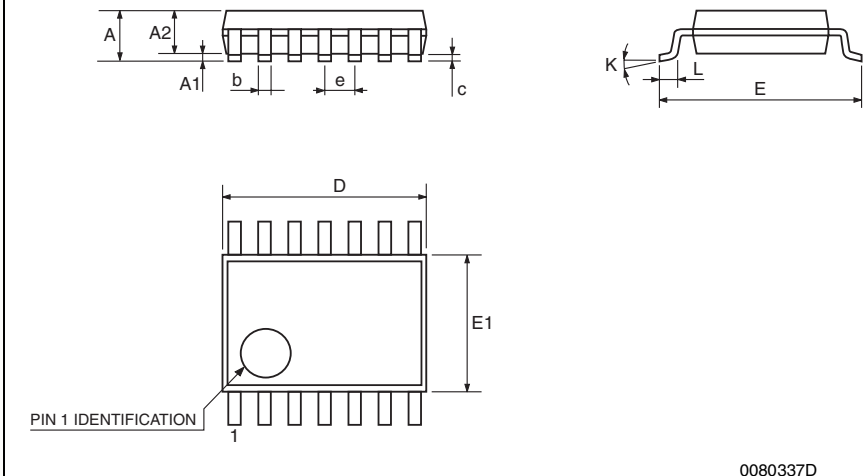


PO13G

6.3 TSSOP14 package

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



7 Revision history

Table 4. Document revision history

Date	Revision	Changes
Nov. 2001	1	Initial release.
April 2006	2	– ESD protection inserted in *Table 1. on page 3*. – Thermal Resistance Junction to Case information added see *Table 1. on page 3*. – Macromodel insertion in paragraph *5 on page 9*.