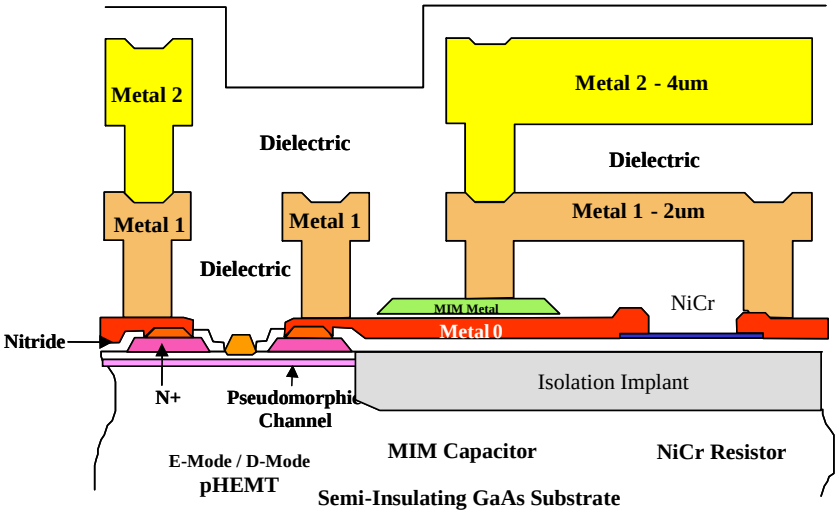
TQPED

0.5 um E/D pHEMT Foundry Service



0.5 um pHEMT Device Cross-Section

General Description

TriQuint's TQPED process is based on our production-released 0.5 µm TQPHT process. TQPED partners an E-Mode pHEMT device with our TQPHT D-Mode transistors to be the first foundry pHEMT process to integrate E-Mode and D-Mode transistors on the same wafer. This process is targeted for low noise amplifiers, linear, low loss and high isolation RF switch applications, converters and integrated RF Front Ends. The TQPED process offers a D-Mode pHEMT with a –0.8 V pinch off, and an E-Mode pHEMT with a +0.35 V threshold voltage. The three metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost –effective die sizes.

Features

- E-Mode, 0.35 V, Vth
- D-Mode, -0.8 V Vp
- InGaAs Active Layer pHEMT Process
- 0.5 um Optical Lithography Gates
- High Density Interconnects:
  - 2 Global
  - 1 Local
- High-Q Passives
- Thin Film Resistors
- High Value Capacitors
- Backside Vias Optional
- Based on Production TQPHT pHEMT and Interconnect
- Nominal TOM3 FET Models Available

Applications

- Highly Efficient, and Linear Power Amplifiers
- Low Loss, High Isolation, Low-Harmonic Contnt Switches
- Integrated digital control logic for Switches and Transceivers
- Converters
- Integrated RF Front Ends– LNA, SW, PA
- Wireless Transceivers, Base stations, Direct Broadcast Satellite Radars, Digital Radios, RF / Mixed Signal ICs
- Power Detectors and Couplers

Production Release: Q1'2005

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TQPED Process Details

Process Details @ Vds = 3.0V			
Element	Parameter	Value	Units
D-Mode pHEMT	Vp (1uA/um)	-0.8	V
	Idss	225	mA/mm
	Imax	550	mA/mm
	Breakdown, Vdg	15 min, 20 typ	V
	Ft @ 50% Idss	25	GHz
	Fmax @ 50% Idss	90	GHz
	Gm (50% Idss)	350	mS/mm
	Ron	1.5	Ohms * mm
E-Mode pHEMT	Vth (1uA/um)	+0.35	V
	Idss	0.1	uA/um
	Imax	310	mA/mm
	Breakdown, Vdg	15 min, 18 typ	V
	Ft @ 50% Idss	30	GHz
	Fmax @ 50% Idss	100	GHz
	Gm (50% Idss)	625	mS/mm
	Ron	2.5	Ohms * mm
Common Process Element Details			
Gate Length		0.5	µm
Interconnect		3	Metal Layers
MIM Caps	Value	630	pF/mm2
Resistors	NiCr	50	Ohms/sq
	Bulk	285	Ohms/sq

Maximum Ratings

Storage Temperature Range	-65 to +150	Deg C
Operating Temperature Range	-55 to +150	Deg C
EFET/DFET Transistor (Vs open; Idg = 1uA/um)	15	V
Capacitor	40	V

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Prototyping and Development

- Prototype Development Quick Turn (PDQ):
  - Shared mask set
  - Run monthly
  - Hot Lot cycle time
- Prototype Wafer Option (PWO):
  - Customer-specific masks; Customer schedule
  - 2 wafers delivered
  - Hot Lot cycle time
  - With thinning and sawing; optional backside vias

Design Tool Status

- Complete Design Manual Now
- Device Library of circuit elements: FETs, diodes, thin film resistors, capacitors, inductors
- Design Kit for Agilent's ADS design environment
- Design Kit planned for AWR Microwave Office
- Layout Library in GSD II format
- Cadence Development Kit with PCells in Preliminary Release
- Layout Rule Sets for Design Rule Check for ICED, Cadence
- Qualified package models for supported package styles
- Noise parameters on specific device sizes available

Training

- GaAs Design Classes:
  - Half-Day Introduction; Upon request
  - Four-Day Technical Training; Fall and Spring at TriQuint Oregon facility
- For Training & PDQ Schedules, please visit: www.triquint.com/foundry/

Process Qualification Status

- Mature process based on TQPHT 150-mm process
- Process release to production scheduled for Q1 2005
- Full 150mm wafer Process Qualification in process. To be completed early Q1 2005
- For more information on Quality and Reliability, contact TriQuint or visit: www.triquint.com/manufacturing/QR/

Applications Support Services

- Tiling of GDSII stream files including PCM
- Design Rule Check services
- Layout Versus Schematic check services
- Packaging Development Engineering
- Test Development Engineering:
  - On-wafer
  - Packaged parts
- Thermal Analysis Engineering
- Yield Enhancement Engineering
- Part Qualification Services
- Failure Analysis

Manufacturing Services

- Mask making
- Production 150-mm wafer fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Diesort Testing
- RF On-wafer testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative/ Distributor or Foundry Services Division for Additional information:
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