Initial Release

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Low threshold, -2.4V max.
- High input impedance
- Low input capacitance, 110pFmax.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Application

- Logic level interfaces-ideal for TTL and CMOS
- Battery operated systems
- Photo voltaic devices
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature****	300°C

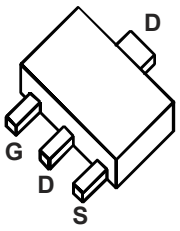
*****Distance of 1.6mm from case for 10 seconds.*

General Description

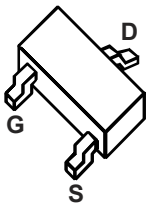
These low threshold enhancement-mode (normally-off) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-243AA (SOT-89)*



TO-236AB (SOT-23)*

** "Green" Certified Package*

Ordering Information

Order Number / Package		BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)
TO-243AA**	**TO-236AB*****				
TP5322N8	TP5322K1	-220V	12Ω	-2.4V	-0.7A
TP5322N8-G*	TP5322K1-G*	-220V	12Ω	-2.4V	-0.7A

***Same as SOT-89. Product supplied on 2000 piece carrier tape reels.*
****Same as SOT-23. Products supplied on 3000 piece carrier tape reels.*

Product Marking for SOT-89

TP3C✶

Where ✶=2-week alpha date code

Product Marking for SOT-23

P3C✶

Where ✶=2-week alpha date code

A042005

Thermal Characteristics

Package	I_D (continuous)	I_D (pulsed)	Power Dissipation @ T_A = 25°C	θ_{JC} °C/W	θ_{JA} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-0.26A	-0.90A	1.6W	15	78**	-0.26A	-0.9A
TO-236AB	-0.12A	-0.70A	0.36W	200	350	-0.12A	-0.7A

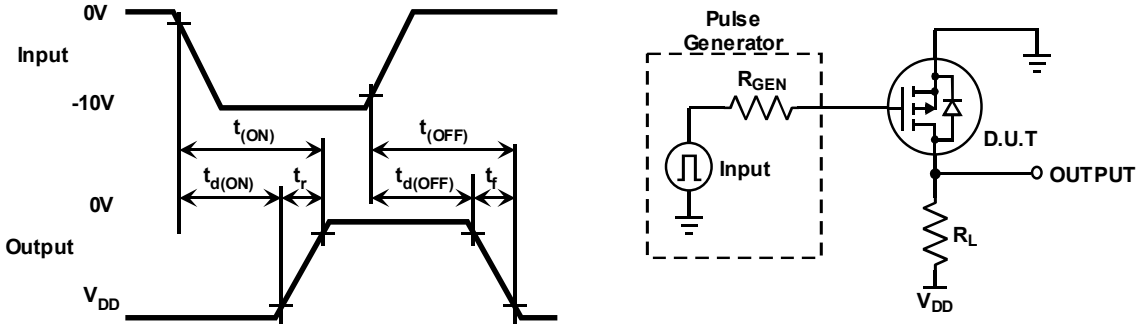
I_D(continous) is limited by max rated Tj.
***Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant PD increase possible on ceramic substate.*

Electrical Characteristics *(@25°C unless otherwise specified)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-220			V	V_{GS} = 0V, I_D = -2mA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-10	µA	V_{GS} = 0V, V_{DS} = Max Rating
				-1.0	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	On-State Drain Current	-0.7	-0.95		A	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		10	15	Ω	V_{GS} = -4.5V, I_D = -100mA
			8.0	12		V_{GS} = -10V, I_D = -200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/°C	V_{GS} = -10V, I_D = -200mA
G_{FS}	Forward Transconductance	100	250		mmho	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input Capacitance			110	pF	V_{GS} = 0V, V_{DS} = -25V f = 1MHz
C_{OSS}	Common Source Output Capacitance			45		
C_{RSS}	Reverse Transfer Capacitance			20		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = -25V, I_D = -0.7A R_{GEN} = 25 Ω
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-Off Delay Time			20		
t_f	Fall Time			15		
V_{SD}	Diode Forward Voltage Drop			-1.8	V	V_{GS} = 0V, I_{SD} = -0.5A
t_{rr}	Reverse Recovery Time		300		ns	V_{GS} = 0V, I_{SD} = -0.5A

Notes:
1) All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse at 2% duty cycle.)
2) All AC parameters sample tested.

Switching Waveforms and Test Circuit



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