N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package
				Die*
60V	3.0Ω	2A	2.0V	TN1506NW
100V	3.0Ω	2A	2.0V	TN1510NW

* Die in wafer form.

Features

- ❑ Low threshold — 2.0V max.
- ❑ High input impedance
- ❑ Low input capacitance — 50pF typical
- ❑ Fast switching speeds
- ❑ Low on resistance
- ❑ Free from secondary breakdown
- ❑ Low input and output leakage
- ❑ Complementary N- and P-channel devices

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ❑ Logic level interfaces – ideal for TTL and CMOS
- ❑ Solid state relays
- ❑ Battery operated systems
- ❑ Photo voltaic drives
- ❑ Analog switches
- ❑ General purpose line drivers
- ❑ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C

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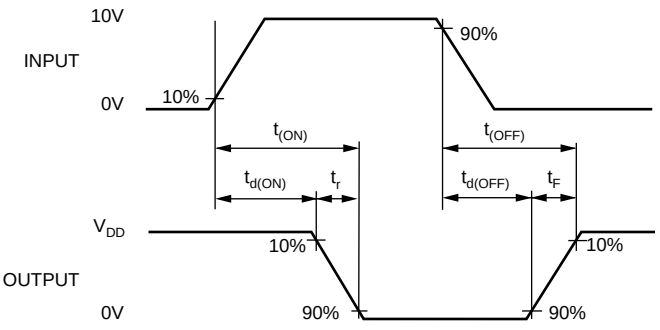
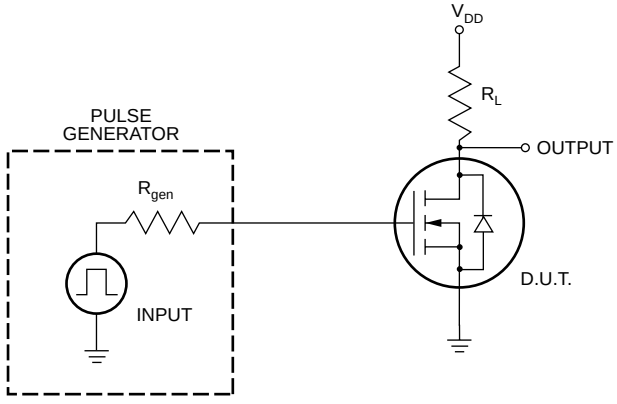
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN1510	100			V	I_D = 1mA, V_{GS} = 0V
		TN1506	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		2.0	V	V_{GS} = V_{DS}, I_D = 0.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.2	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					500		V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.75	1.4		A	V_{GS} = 5V, V_{DS} = 25V
			2.0	3.4			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	4.5	Ω	V_{GS} = 4.5V, I_D = 250mA
				1.6	3.0		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.1	%/°C	I_D = 0.5A, V_{GS} = 10V
G_{FS}	Forward Transconductance		225	400		m℧	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input Capacitance			50	60	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	35		
C_{RSS}	Reverse Transfer Capacitance			4.0	8.0		
$t_{d(ON)}$	Turn-ON Delay Time			2.0	5.0	ns	V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25Ω
t_r	Rise Time			3.0	5.0		
$t_{d(OFF)}$	Turn-OFF Delay Time			6.0	7.0		
t_f	Fall Time			3.0	6.0		
V_{SD}	Diode Forward Voltage Drop			1.0	1.5	V	I_{SD} = 0.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time			400		ns	I_{SD} = 0.5A, V_{GS} = 0V

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





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