CMOS 4-BIT MICROCONTROLLER

TMP47C850N
TMP47C850F

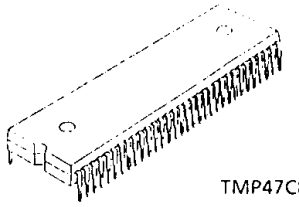
The 47C850 is a high performance 4-bit single chip microcomputer based on the TLCS-470 series. And the 47C850 has a built-in DTMF receiver and BEEP output circuit, which is suitable for application in telephones.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C850N	8192 × 8-bit	512 × 4-bit	SDIP64	TMP47C050E
TMP47C850F			QFP64	TMP47C050G

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time :
  2.23μs (at 3.58MHz), 244μs (at 32.8KHz)
- ◆92 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (52 pins)
  - Input 2ports 5pins
  - Output 4ports 16pins
  - I/O 8ports 31pins
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Interval Timer
- ◆Watchdog Timer
- ◆Serial interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - External/Internal clock, leading/trailing edge shift, and 4/8-bit mode
- ◆DTMF (Dual Tone Multi Frequency) receiver circuit
  - DTMF signal detect, 4-bit hexadecimal code conversion
  - Equivalent function to TC35300BP (Software for adjusting acquisition)
- ◆BEEP output function
  - Ten different frequencies can be selected for output frequencies.
- ◆4-bit A/D converter input 4 channels
- ◆High current outputs
  LED direct drive capability (typ. 20mA × 16-bit)
- ◆Dual-clock operation
  High-speed/Low-power consumption operating mode
- ◆Hold function
  Battery/capacitor back-up
- ◆Real Time Emulator : BM47C850

SDIP64

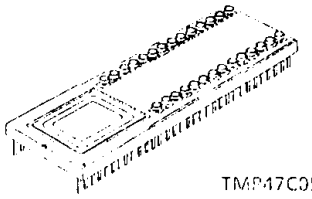


TMP47C850N

QFP64

TMP47C850F

SDIC64



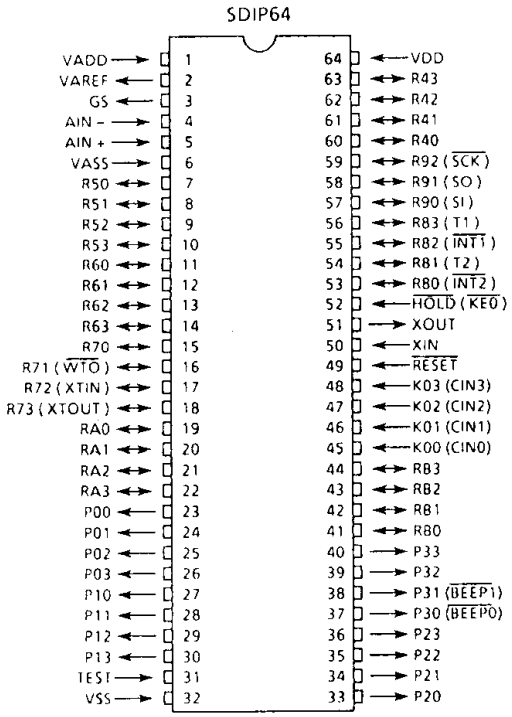
TMP47C050E

QFC64

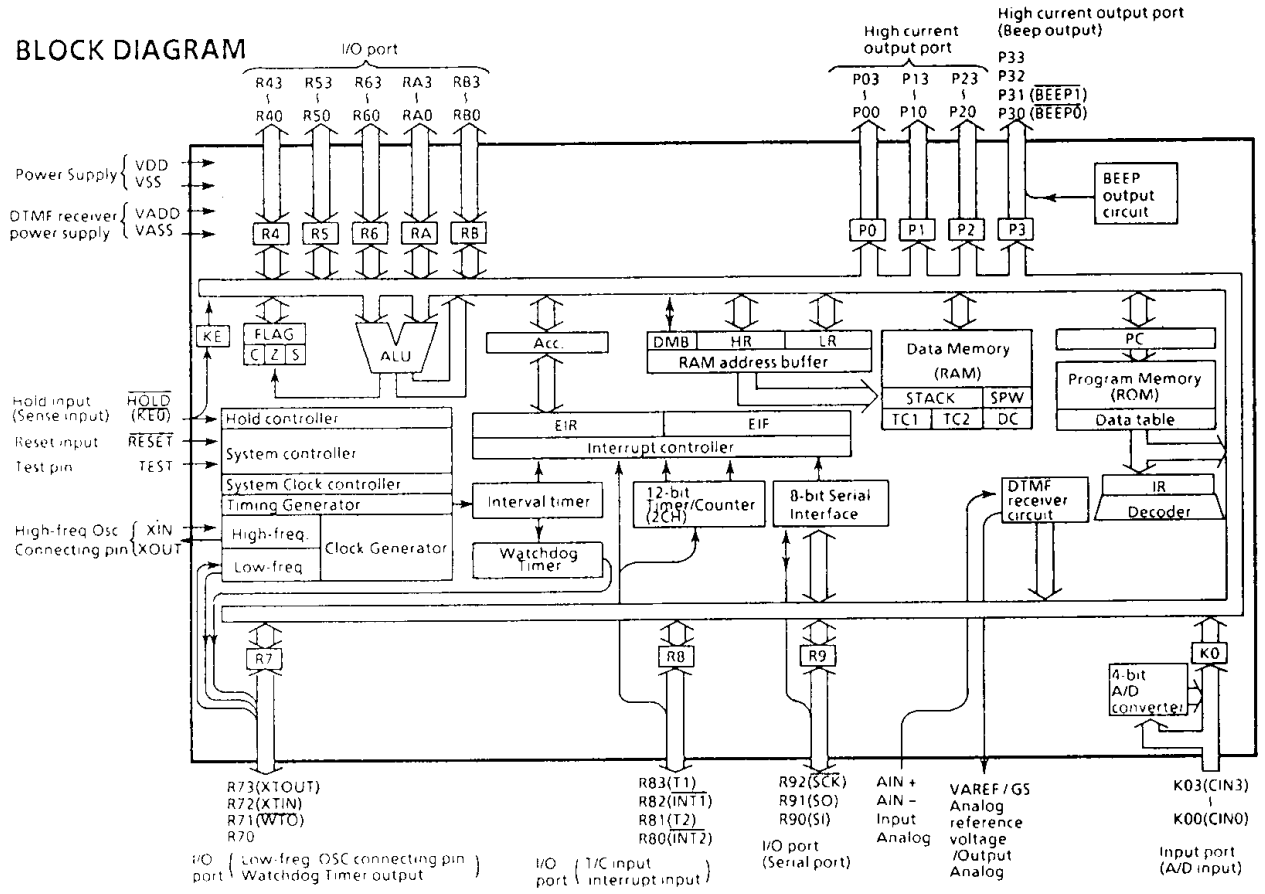
TMP47C050G

PIN ASSIGNMENT (TOP VIEW)

SDIP64



BLOCK DIAGRAM



PIN FUNCTIONS

PIN NAME	Input/Output	FUNCTIONS	
K03 (CIN3) ~ K00 (CIN0)	Input	4-bit input port.	A/D converter (Comparator) input
P03 ~ P00	Output	4-bit output port with latch	
P13 ~ P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 ~ P20			
P33 ~ P32	Output	4-bit output port with latch	
P31 ($\overline{BEEP1}$) ~P30 ($\overline{BEEP0}$)	Output (Output)		BEEP output
R43 ~ R40	I/O	4-bit I/O port with latch. When used as the input port, the latch must be set to "1".	
R53 ~ R50			
R63 ~ R60			
RA3 ~ RA0			
RB3 ~ RB0			
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as the input port or watchdog timer output, the latch must be set to "1".	Resonator connecting pins (Low-frequency). For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as the input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer/counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as the input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN, XOUT	Input, Output	Resonator connecting pin (High-frequency). For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
AIN +, AIN −	Input	DTMF signal input	
VAREF, GS	Output	VDD/2 reference voltage output. First stage differential amplifier output.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VADD		Analog reference voltage for DTMF receiver	
VASS		Analog reference GND for DTMF receiver	

OPERATIONAL DESCRIPTION

Concerning the 47C850 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C860, the technical data sheets for the 47C860 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) Internal CPU Function

They are similar to that of the 47C860.

(2) Peripheral Hardware Function

① I/O port	⑤ A/D Converter (comparator) input circuit
② Interval Timer	⑥ BEEP output function
③ Timer/Counters	⑦ DTMF Receiver circuit
④ Watchdog Timer	⑧ Serial Interface

As the description has been provide with priority on ports (①, ⑤, ⑥ and ⑦) changed from 47C860.

2. PERIPHERAL HARDWARE FUNCTION

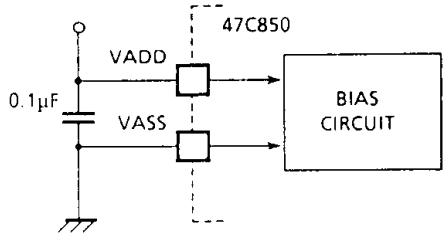
2.1 I/O Ports

The 47C850 has 14 ports (52 pins) each as follows.

① K0	;	4-bit input (shared with comparator inputs)
② P0, P1, P2	;	4-bit output
③ P3	;	4-bit output (shared with BEEP output)
④ R4, R5	;	4-bit input/output
⑤ R6	;	4-bit input/output
⑥ R7	;	4-bit input/output (shared with the low-frequency resonator connection pins and the watchdog timer output)
⑦ R8	;	4-bit input/output (shared with external interrupt request input and timer/counter input)
⑧ R9	;	3-bit input/output (shared with serial ports)
⑨ RA, RB	;	4-bit input/output
⑩ KE	;	1-bit sense input (shared with hold request/release signal input)

The description has been provide with priority on ports (①, ③ and ④) changed from 47C860.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

※ DTMF Receiver Analog Power Supply
Noise in the DTMF analog power supply adversely affects the reception level of the DTMF receiver. To obtain a stable performance of the DTMF receiver, insert a bypass capacitor between VADD and VASS, as close to the device as possible.



Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port (A/D converter input)	P0 output port (Note 3)	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	P3 output latch	P3 output port ($\overline{BEEP}$ output)	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	RB input port	RB output port	○	○	○	–	○	○	–
0C	DTMF receiver status input	——	○	–	–	–	–	○	–
0D	DTMF receiver data input	DTMF receiver circuit control	○	○	○	–	–	○	–
0E	Status input (Note 4)	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	BEEP output frequency set	–	○	–	–	–	–	–
13	Undefined	BEEP output control	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	K0 port input selector	–	○	–	–	–	–	–
18	Undefined	A/D converter input control	–	○	–	–	–	–	–
19	Undefined	Interval timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	Undefined	Serial interface control 1	–	○	–	–	–	–	–
1F	Undefined	Serial interface control 2	–	○	–	–	–	–	–

Note 1 "——" means the reserved state. Unavailable for the user programs.

Note 2 The 5-bit to 8-bit data conversion instruction [OUTB @ HL], automatic access to ports P1 and P2.

Note 3 As concerns the port address "00". In and TEST instructions operate port K0, and out instruction operates port P0.

Note 4 The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.

Table 2-1. Port Address Assignments and Available I/O Instructions

(1) Port K0 (K03~K00)

The 4-bit input port. Port K0 is shared with the A/D converter (comparator) input. The K0 port input selector (OP17) determines whether this port is to be used for digital or comparator input. The most significant bit of the K0 port input selector is set to "1" for digital input and to "0" for comparator input.

The K0 port input selector is initialized to "0" during reset.

Port K0 (Port address IP00)

3	2	1	0
K03 (CIN3)	K02 (CIN2)	K01 (CIN1)	K00 (CIN0)

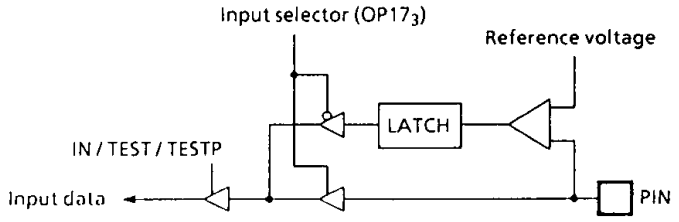


Figure 2-1. Port K0

(2) Port P3 (P33~P30)

The 4-bit output with a latch. The latch is initialized to "1" during reset. The P30 pin and the P31 pin are also used for BEEP output.

Port R3 (Port address OP03/IP03)

3	2	1	0
P33	P32	P31 ($\overline{BEEP1}$)	P30 ($\overline{BEEP0}$)

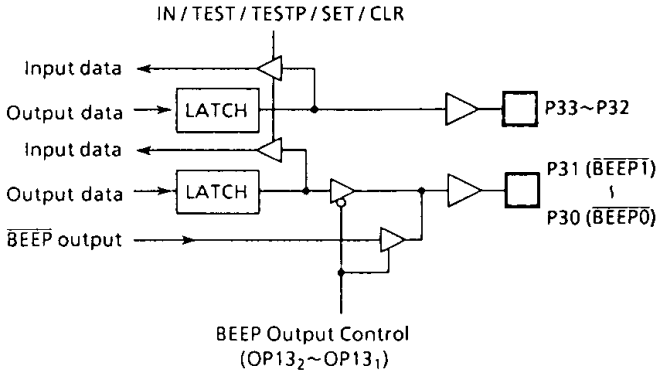


Figure 2-2. Port P3

(3) Ports R4 (R43~R40), R5 (R53~R50)

These ports are 4-bit I/O ports with latch. The latch is initialized to "1" during reset. When used as input port, the latch should be set to "1".

Port R4 (Port address OP04 /IP04)

3	2	1	0
R43	R42	R41	R40

Port R5 (Port address OP05 /IP05)

3	2	1	0
R53	R52	R51	R50

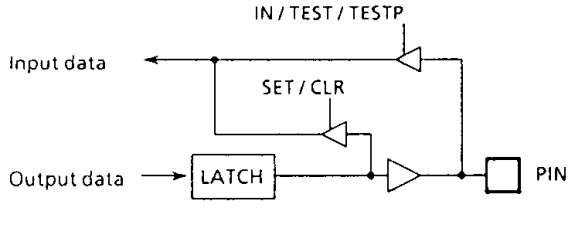


Figure 2-3. Ports R4 and R5

2.2 Comparator Input

It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0-CIN3) can be detected as 16-stage by setting reference voltage.

The comparator input can also be used as K0 port (digital input). To use as K0 port, set the port address OP17 to "1***"

2.2.1 Circuit of Comparator Input

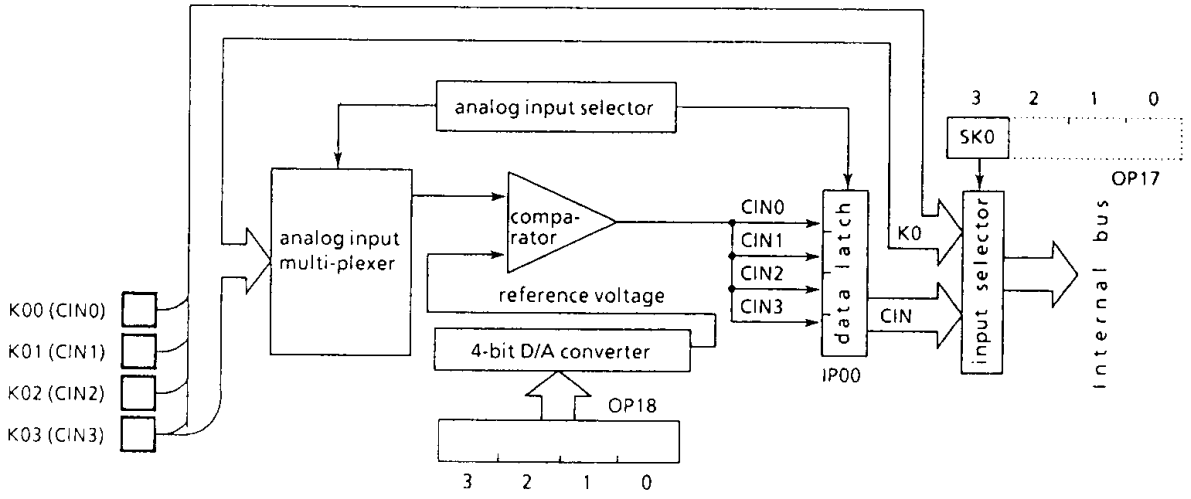


Figure 2-4. Comparator Input Circuit

2.2.2 Control of Comparator Input

Port K0 Input Selector
(Port address : OP17 Initial value : 0***)

3	2	1	0
SK0			

SK0	Input select
0	CIN comparator input
1	K0 digital input

Figure 2-5. Command Register

Reference voltage (Vref.) is set by command register (port address OP18), and it is determined by the following form.

$$V_{REF} = V_{DD} \times (n + 1) / 16 \text{ [V]} \quad (n = 0 \sim 15)$$

After initialization sequence, 4-channel comparator inputs continue comparison operation successively.

Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 8-instruction cycles after setting a reference voltage to read data form the comparator.

When analog input voltage is higher than reference voltage, comparator data latch is set to "1".

At the initialization sequence, OP18 is set to "0".

OP18				Vref. [V]
3	2	1	0	
0	0	0	0	0.31
0	0	0	1	0.62
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.56
0	1	0	1	1.87
0	1	1	0	2.19
0	1	1	1	2.50
1	0	0	0	2.81
1	0	0	1	3.12
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.37
1	1	1	0	4.69
1	1	1	1	5.00

Table 2-2. Reference Voltage

Note. When the comparator input is selected, the comparator consumes typically 700μa current at VDD = 5V. To reduce the power consumption, K0 port should be set to digital mode. In the HOLD mode, the comparator current is automatically cut off by hardware.

2.3 BEEP Output Circuit

BEEP output circuit generates square wave in the audible frequency range. This circuit can make use the key input confirmation tone and the bell tone for telephone applications.

$\overline{BEEP0}$ and $\overline{BEEP1}$ output pins are shared by the P30 and P31 output. To output BEEP, select BEEP using OC1 or OC2 of the BEEP control register (OP13) and enable output with POC.

2.3.1 Configuration of BEEP Output Circuit

Figure 2-6 shows configuration of the BEEP output circuit. The clock pulse of BEEP output circuit is supplied by a timing generator. BEEP output is controlled by frequency selection and output enable/disable setting.

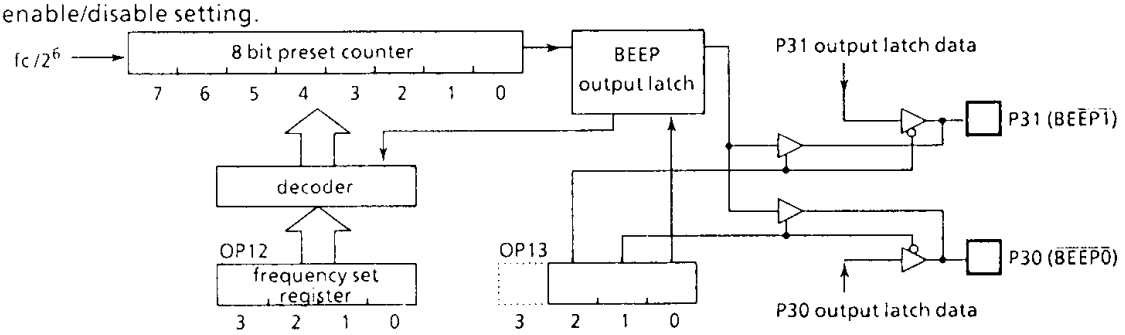


Figure 2-6. BEEP Output Circuit

2.3.2 Control of BEEP Output

The output frequency is set by Command register (port address OP12). The output frequency is illustrated in Table 2-3. BEEP output changes to "H" level when any other data ("B" ~ "F") are set (OP12).

OP12 3	2	1	0	Output freq. [Hz]
0	0	0	1	200
0	0	1	0	400
0	0	1	1	595
0	1	0	0	799
0	1	0	1	999
0	1	1	0	1216
0	1	1	1	1398
1	0	0	0	1645
1	0	0	1	1748
1	0	1	0	1998

Table 2-3. Output Frequency

BEEP Output Control
(Port address : OP13 Initial value: *000)

3	2	1	0
	OC2	OC1	POC

OC2 Selects output
0 : P31 port output
1 : $\overline{BEEP1}$ output

OC1 Selects output
0 : P30 port output
1 : $\overline{BEEP0}$ output

POC Controls BEEP output
0 : Disable output
1 : Enable output

Figure 2-7. BEEP Output Control Command Register

2.4 DTMF Receiver

The 47C850 has a built-in DTMF receiver (equivalent to the TC35300BP) which extracts DTMF signals from among the dialing signals received on the circuits of tone dialing type telephones and converts them to 4-bit codes.

A differential amplifier is built into the signal input portion section for connecting a balance circuit and adjusting the reception level. The acquisition time is set with the software.

(DTMF: Dual Tone Multi-Frequency)

2.4.1 DTMF Receiver Configuration

The DTMF receiver consists of a band pass filter which passes only the signal band used for DTMF, a signal decision circuit that determines which signals in the frequency detected high and low groups are valid DTMF signals and converts them to 4-bit codes, and a bias circuit.

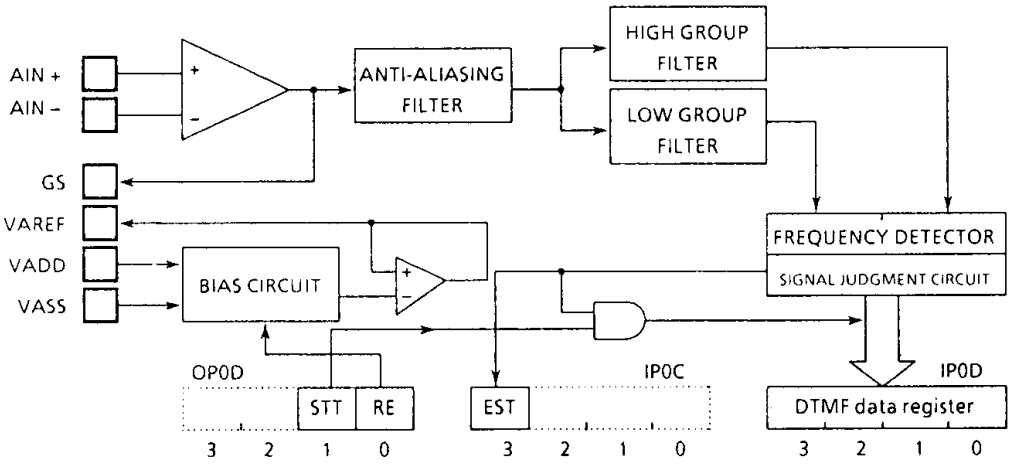


Figure 2-8. DTMF Receiver

(1) Band Pass Filter

The band pass filter consists of a high-precision switched capacitor configured with an anti-aliasing filter, and band pass filters which pass only the low and high groups.

The anti-aliasing filter attenuates the components around 400KHz to prevent detection of the wrong tone. The high and low band pass filters eliminate unnecessary signal components.

(2) Bias Circuit

The bias circuit controls the bias in analog circuits such as filters and adjusts the reception level.

Setting RE (bit 0 of the command register OP0D) to "1" applies bias to all analog circuits and places the DTMF receiver in operating status. Several tens of milliseconds are required for the analog circuits to stabilize so, after setting RE, wait at least 100ms before starting the decision operation.

The reception level can be adjusted as with the TC353008P. Figure 2-9 shows a typical connection for the balance circuit. The gain of the operational amplifier in the next stage is determined as follows:

$$(\text{Gain}) = 20 \times \log \frac{R5}{R1}$$

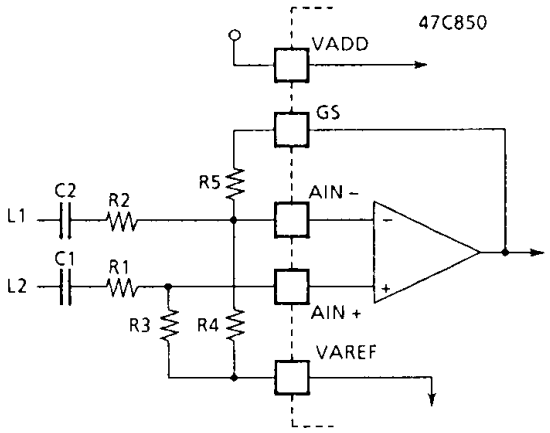


Figure 2-9. The Typical Connection for the Balance Circuit

(3) Signal Decision Circuit and Decision Operation

The signal decision circuit determines whether or not the various high and low group signals are valid, sets EST to "1" when a signal is valid and converts to codes corresponding to the DTMF digit.

After it has been confirmed that EST is set to "1", setting STT to "1" sends the conversion data (codes) to the DTMF data register. Since the completion of conversion cannot be monitored by the hardware, the acquisition time is set with the software.

The last valid tone pair received by the DTMF data register is latched. Clearing RE to "0" puts the DTMF receiver in standby status, but the values in the DTMF data register are hold.

2.4.2 DTMF Receiver Control

The DTMF receiver is controlled by the command register (OP0D), status register (IP0C) and DTMF data register (IP0D).

(1) DTMF Receiver Control (OP0D)

The DTMF receiver operation is enabled and the conversion data in the DTMF data register are revised. STT is not cleared by the hardware.

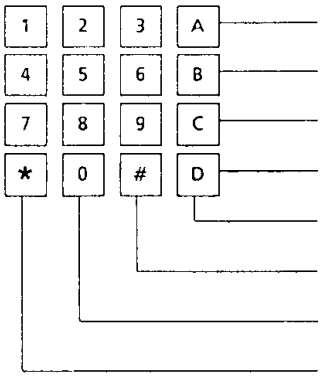
(2) DTMF Receiver Status (IP0C)

The DTMF receiver flag (EST) is a 1-bit flag which indicates whether or not a detected tone pair is valid. This flag is set to "1" when both the frequency detected high and low group signals are valid and is cleared to "0" when the signal detected is not a DTMF signal or no signal is detected.

(3) DTMF Data Register (IP0D)

This register stores the conversion data corresponding to the valid DTMF signals and always holds the code received last.

Table 2-4 shows the DTMF dialing matrix and Table 2-5 shows telephone circuit dial keys and tone frequencies which correspond to the converted codes.



Tone register	Tone freq. (Hz)
ROW0	697
ROW1	770
ROW2	852
ROW3	941
COL3	1633
COL2	1477
COL1	1336
COL0	1209

Table 2-4. DTMF DIALING MATRIX

DTMF Receiver Control

(Port address : OP0D Initial : **00)

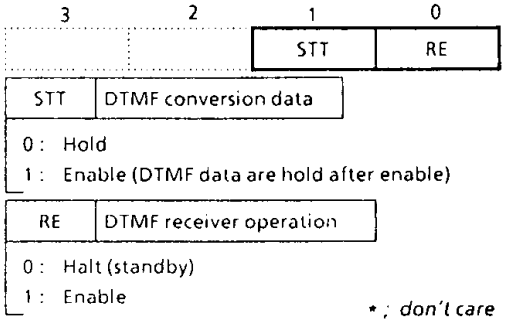


Figure 2-10. Command Register

DTMF Receiver Status

(Port address : IP0C)

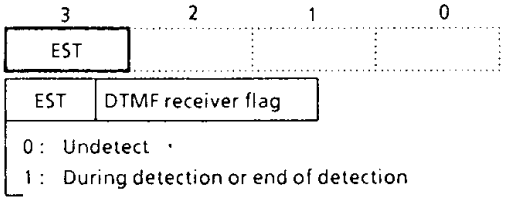


Figure 2-11. Status Register

ROW tone [Hz]	COLUM tone [Hz]	Dial key symbol	EST (IP0C)	DTMF receiver data (IP0D)			
				D3	D2	D1	D0
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1336	0	1	1	0	1	0
941	1209	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
–	–	ANY	0	*	*	*	*

Note. * ; *don't care*

Table 2-5. Telephone Circuit Dial Keys and Tone Frequencies which Correspond to the DTMF Data

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Ports P0, P3, R7, RA, RB	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P1, P2, R4, R5, R6, R8, R9	− 0.3 to 10	
Output Current (per 1 pin)	I_{OUT1}	Port R	3.2	mA
	I_{OUT2}	Port P	30	
Output Current (Total)	ΣI_{OUT2}	Port P	240	
Power Dissipation [T_{opr} = 60°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	5.5	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		3.5759	3.5831	MHz
	fs	XTIN, XTOUT		30	34	KHz

Note. : Input voltage V_{IH3}, V_{IL3} : in the SLOW or HOLD mode

A / D CONVERSION CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN3 to CIN0		V_{SS}	−	V_{DD}	V
A/D Conversion Error				−	−	$\pm\frac{1}{2}$	LSB

D.C. CHARACTERISTICS (V_{SS} = 0V, Topr = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.7	–	V
Input Current	I_{IN1}	K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V/0V	–	–	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Low Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	sink open drain	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	2	μA
Output High Voltage	V_{OH}	Ports (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	–	–	V
Output Low Voltage	V_{OL}	Except port P and XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	
Output Low Current	I_{OL2}	Port P	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Output VREF Voltage	V_{REF}	VAREF pin		2.4	–	2.7	V
Output VREF Resistance	R_{REF}		VREF = 2.55V	–	–	1	KΩ
Supply Current (in the Normal mode)	I_{DD}	DTMF receiver stopped	V_{DD} = 5.5V, fc = 3.58MHz	–	3	6	mA
	I_{DDR}	DTMF receiver moving			7	14	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768KHz	–	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V*

Note 2. *Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up) is contained.*

Note 3. *Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V*
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V
Low frequency clock is only oscillated (connecting XTIN, XTOUT).

OPERATIONAL AMPLIFIER CHARACTERISTICS (AIN +, AIN – to GS) (V_{SS} = 0V, V_{DD} = 5.0V, T_{opr} = 25°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	V_{IO}		–	± 25	–	mV
Input Offset Current	I_{IO}	$V_{SS} \leq V_{IN} \leq V_{DD}$	–	± 100	–	nA
Power Supply Rejection Ratio	PSRR	1KHz	–	60	–	dB
Common Mode Rejection Ratio	CMRR		–	60	–	
Open Loop Gain	A_O		–	65	–	
0 dB Band Width	f_T		–	500	–	KHz
Rated Output Voltage	V_O	GS pin (Load Resistance: 100 Kohm or over)	–	4.5	–	V_{PP}
Load Resistance	R_L	GS pin	–	30	–	KΩ
Capacitive Load	C_L		–	50	–	pF

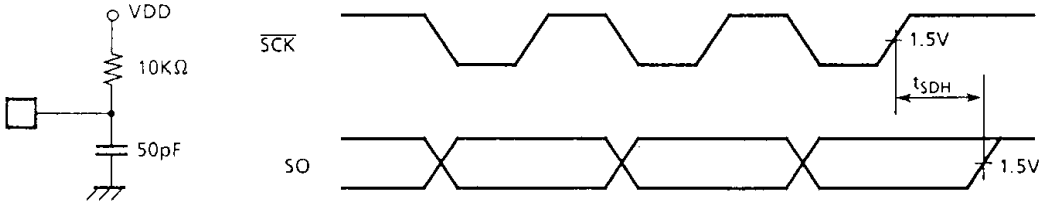
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = − 30 to 60°C)

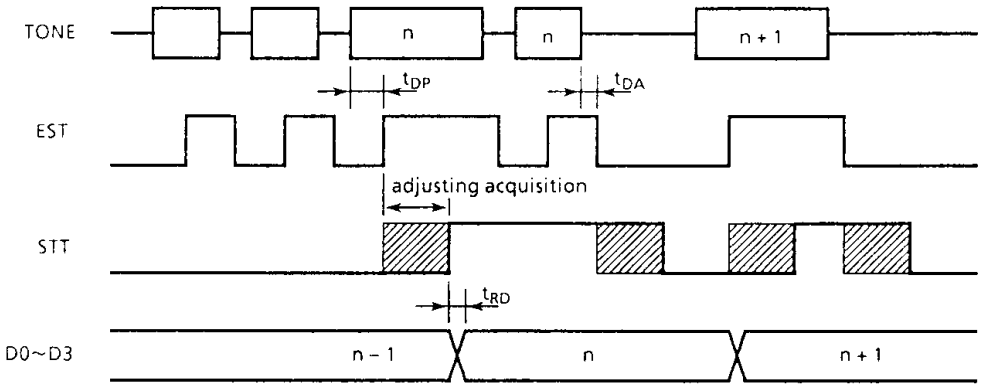
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	−	2.23	−	μs
		In the SLOW mode	235	−	267	
High Level Clock Pulse Width	t_{WCH}	External clock mode	80	−	−	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ − 300	−	−	ns
Minimum Input Signal Level for Reception		Each tone composite signal	−	− 35	− 30	dBm
EST Output Delay Time	t_{DP}	"L" → "H"	5	11	14	ms
	t_{DA}	"H" → "L"	0.5	4.0	8.5	
DTMF Output Delay Time	t_{RD}		−	6	9	μs

(1) Serial Port (Completion of Transmission)

Note. Shift data Hold Time: External circuit for $\overline{SCK}$ pin and SO pin



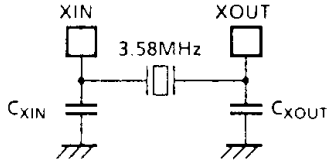
(2) DTMF Receiver (Signal Detect Timing)



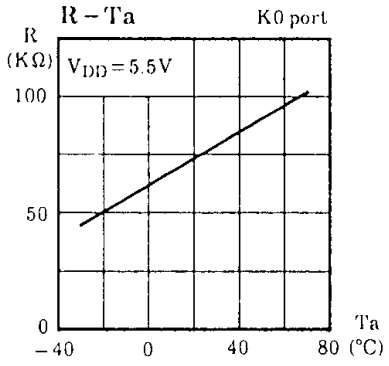
RECOMMENDED OSCILLATING CONDITIONS

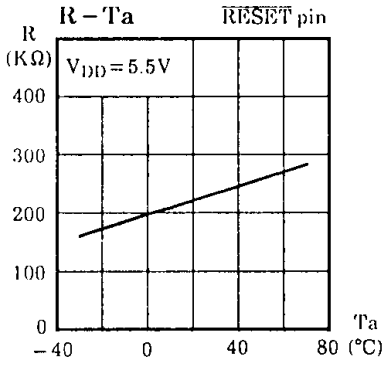
(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = − 30 to 60°C)

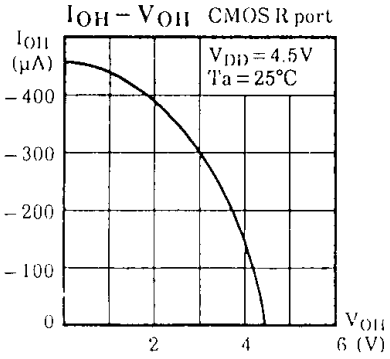
(1) 3.58MHz
Crystal Resonator

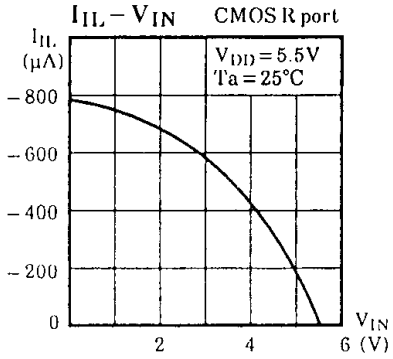


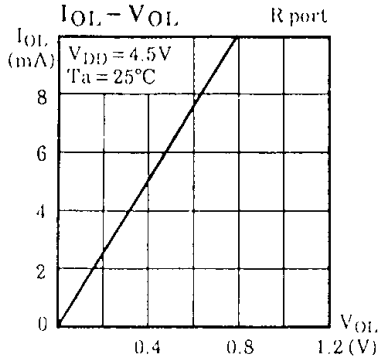
TYPICAL CHARACTERISTICS

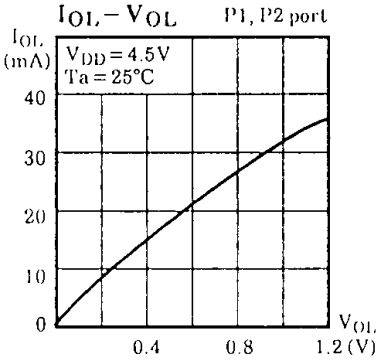


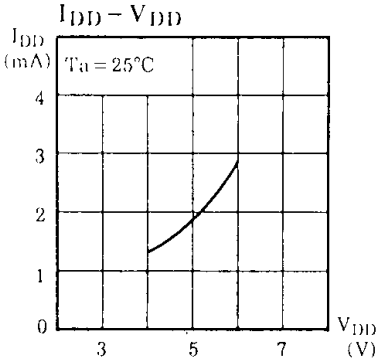


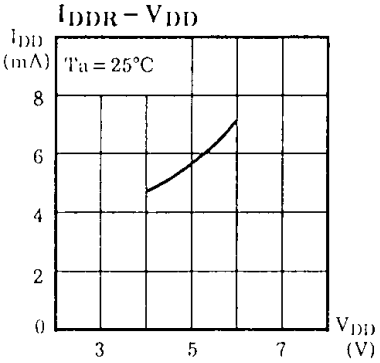












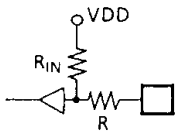
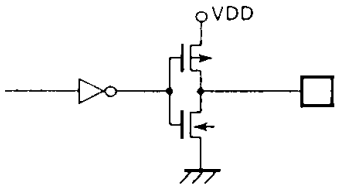
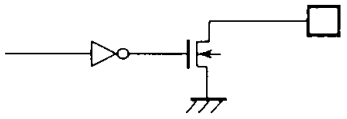
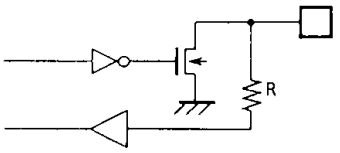
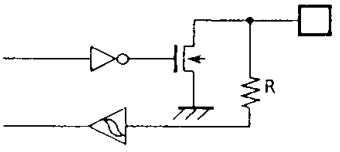
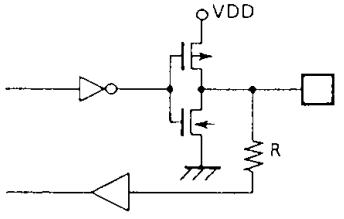
INPUT/OUTPUT CIRCUITRY

(1) Control Pins

The input/output circuitries of the 47C850 control pins are similar to those of the 47C860.

(2) I/O Ports

The input/output circuitries of the 47C850 I/O ports appoint code: WB.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	WB 	Pull-up resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P0 P3	Output		Push-pull output Initial "High" High current I_{OL} = 20mA (typ.)
P1 P2	Output		Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.)
R4 R5 R6 R7	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
RA RB	I/O		Push-pull output Initial "High" R = 1KΩ (typ.)

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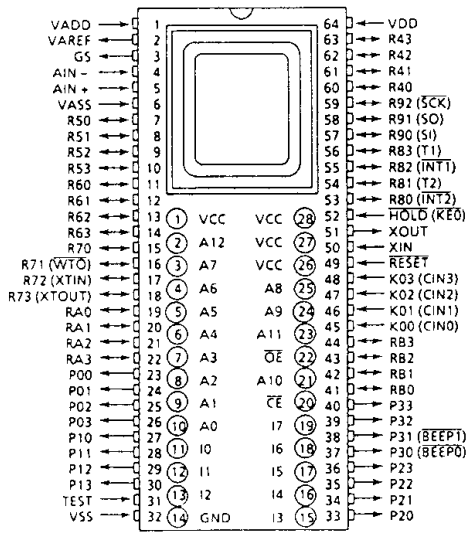
CMOS 4-BIT MICROCONTROLLER

TMP47C050E
TMP47C050G

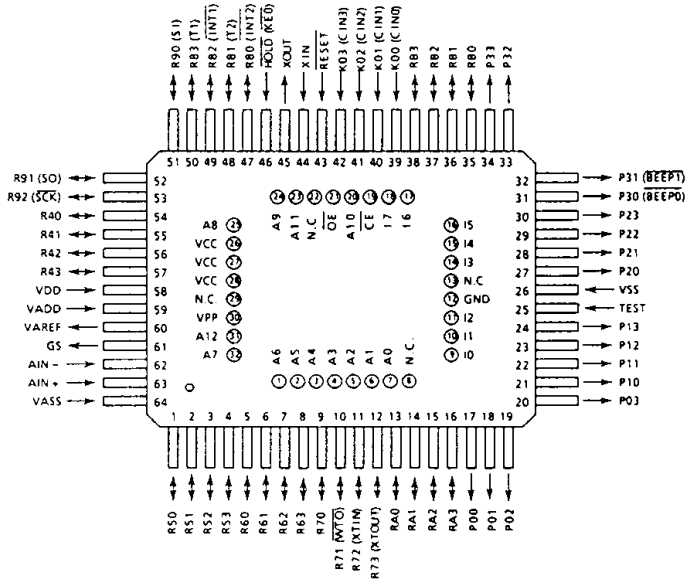
The 47C050, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C850 application systems (programs).
The 47C050 is pin compatible with the 47C850 which is mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)

QFC64



SDIC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A12 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

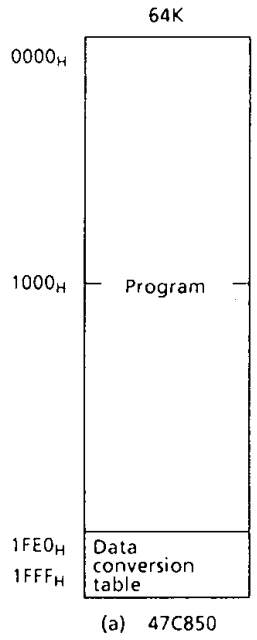
A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5~5.5V	–	–	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	–	–	ns
Data Hold Time	t_{IH}	Topr = – 30~60°C	50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area are as shown in Figure 1.



(a) 47C850

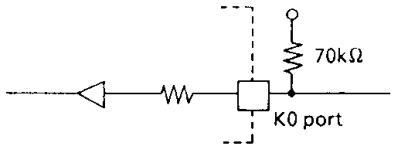
Figure 1. Program area

(2) Data memory

47C050 contains two 256 x 4 bit data memory banks (DMB0, DMB1).

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C050 are different to the code WB of the 47C850.
When this chip is used as evaluator with the code WB of the 47C850, it is necessary to provide the external resistors.



(a) Code : WB

Figure 2. I/O code and external circuitry