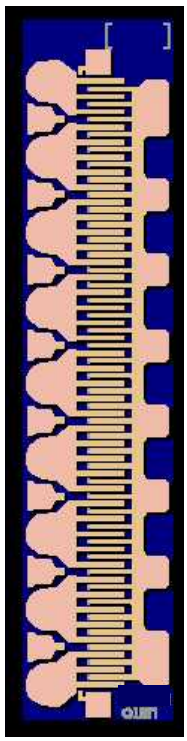
TriQuint SEMICONDUCTOR

Product Data Sheet
March 31, 2003

9.6 mm Discrete HFET TGF4260-SCC



Key Features and Performance

- 9600 µm x 0.5 µm HFET
- Nominal Pout of 37dBm at 6 GHz
- Nominal Gain of 9.5dB at 6 GHz
- Nominal PAE of 52% at 6 GHz
- Frequency Range: DC - 10.5 GHz
- Suitable for high reliability applications
- 0.6 x 2.4 x 0.1 mm (0.024 x 0.093 x 0.004 in)

Primary Applications

- Cellular Base Stations
- High-reliability space
- Military

Description

The TriQuint TGF4260-SCC is a single gate 9.6 mm discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high efficiency power applications up to 10.5 GHz in Class A and Class AB operation.

Typical performance at 6 GHz is 37dBm power output, 9.5 dB Gain, and 52% PAE.

Bond pad and backside metallization are gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire bonding processes.

The TGF4260-SCC is readily assembled using automatic equipment.

TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER 1/	VALUE	NOTES
V_{DS}	Drain to Source Voltage	12 V	
V_{GS}	Gate to Source Voltage Range	0 to -5.0 Volts	
P_D	Power Dissipation	6.8 W	2/
T_{CH}	Operating Channel Temperature	150°C	3/, 4/
T_{STG}	Storage Temperature	-65 to 200°C	
T_M	Mounting Temperature (30 seconds)	320°C	

1/ These ratings represent the maximum values for this device. Stresses beyond those listed under "Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "DC Probe Characteristics" is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

2/ When operated at this bias condition with a base plate temperature of 70 ^{0}C, the MTTF life is reduced from 1.7 E+12 to 3 E+9 hours.

3/ Junction temperature will directly affect the device Mean Time to Failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels

4/ These ratings apply to each individual FET

TABLE II
DC PROBE CHARACTERISTICS
(T_A = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note
I_{DSS}	Saturated Drain Current	--	2352	--	mA	1/
G_M	Transconductance	--	1584	--	mS	1/
V_P	Pinch-off Voltage	1	1.85	3	V	2/
V_{BGS}	Breakdown Voltage Gate-Source	17	22	30	V	2/
V_{BGD}	Breakdown Voltage Gate-Drain	17	22	30	V	2/

1/ Total for eight FETS
2/ V_P, V_{BGS}, and V_{BGD} are negative.

TABLE III
ELECTRICAL CHARACTERISTICS
(T_A = 25 °C, Nominal)
Bias Conditions: Vd = 8.5 V, Id = 520 mA

Symbol	Parameter	Typical	Unit
Pout	Output Power	37	dBm
Gp	Power Gain	9.5	dB
PAE	Power Added Efficiency	52	%

TABLE IV
THERMAL INFORMATION*

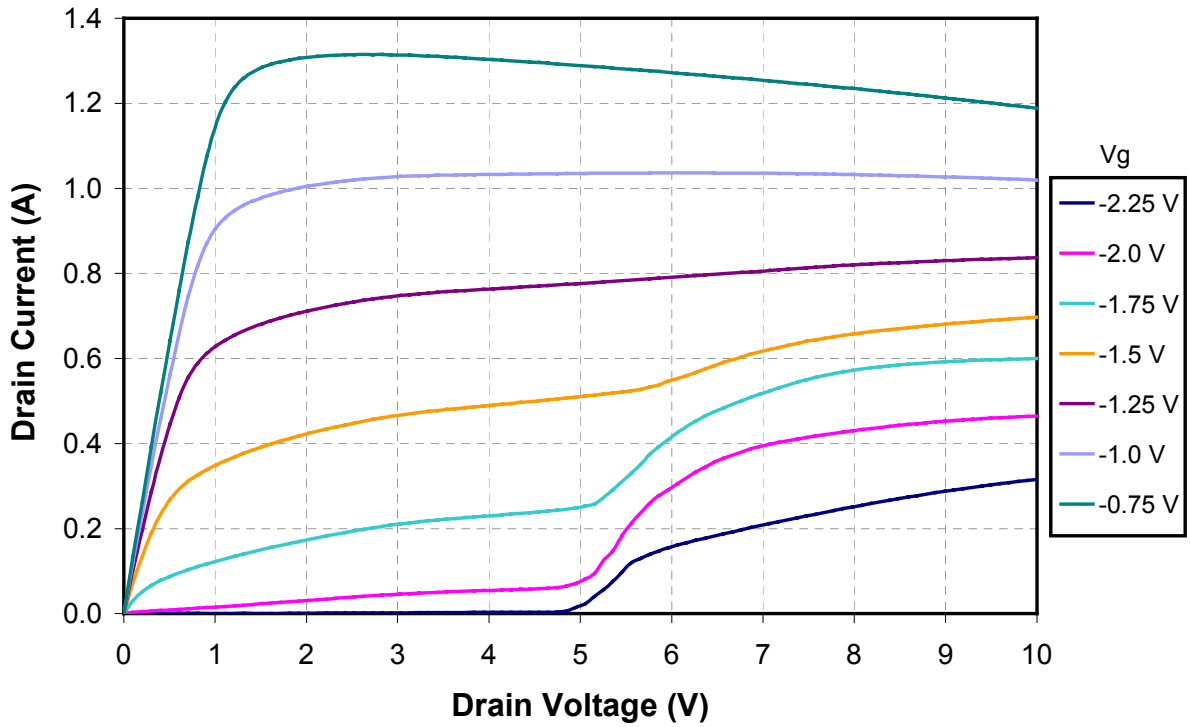
Parameter	Test Conditions	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 8.5 V I_D = 520 mA Pdiss = 6.8 W	101.64	7.16	1.7 E+12

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

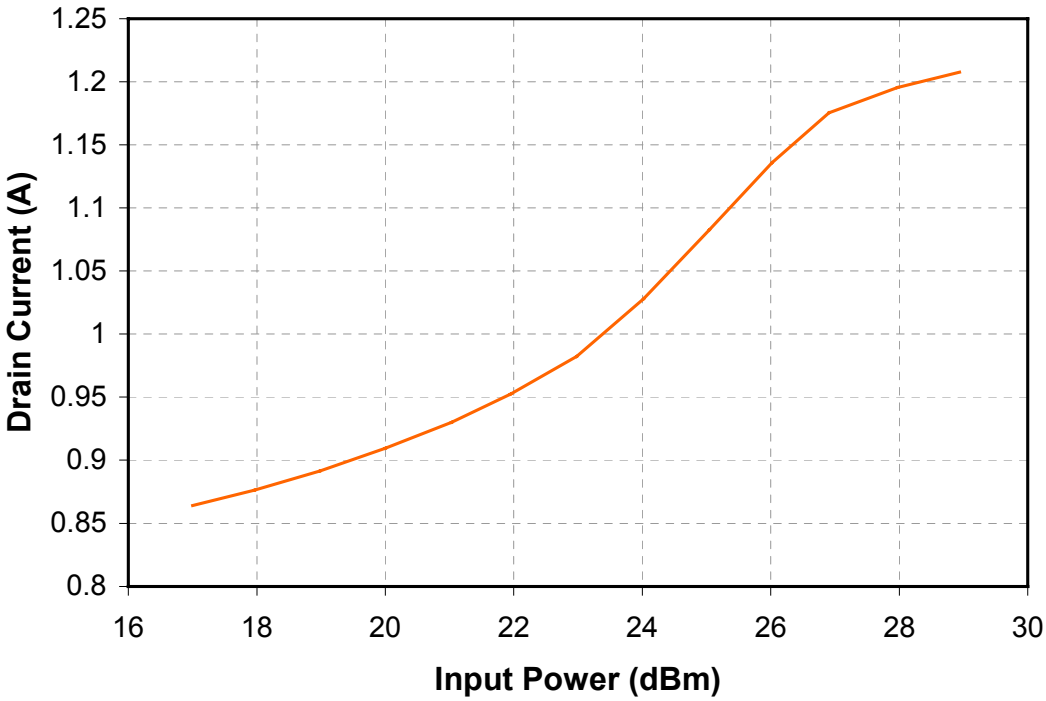
* The thermal information is a result of a detailed thermal model.

TYPICAL PERFORMANCE

(T_A = 25 °C, Nominal)



Bias Conditions: F = 6 GHz, Vd = 8.5 V, Iq = 795 mA



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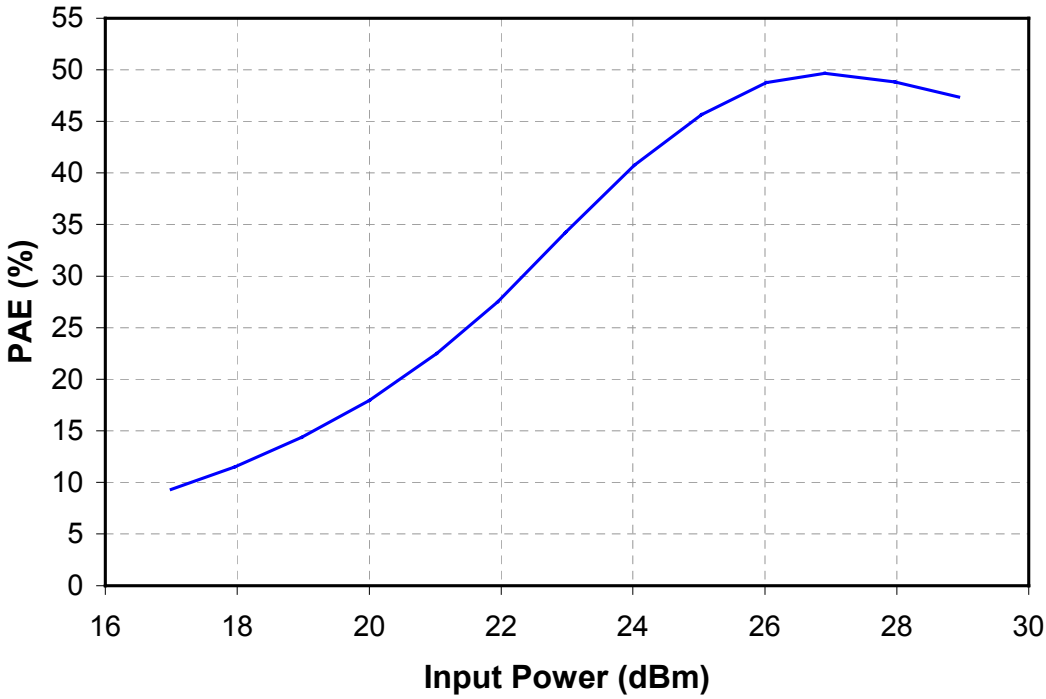

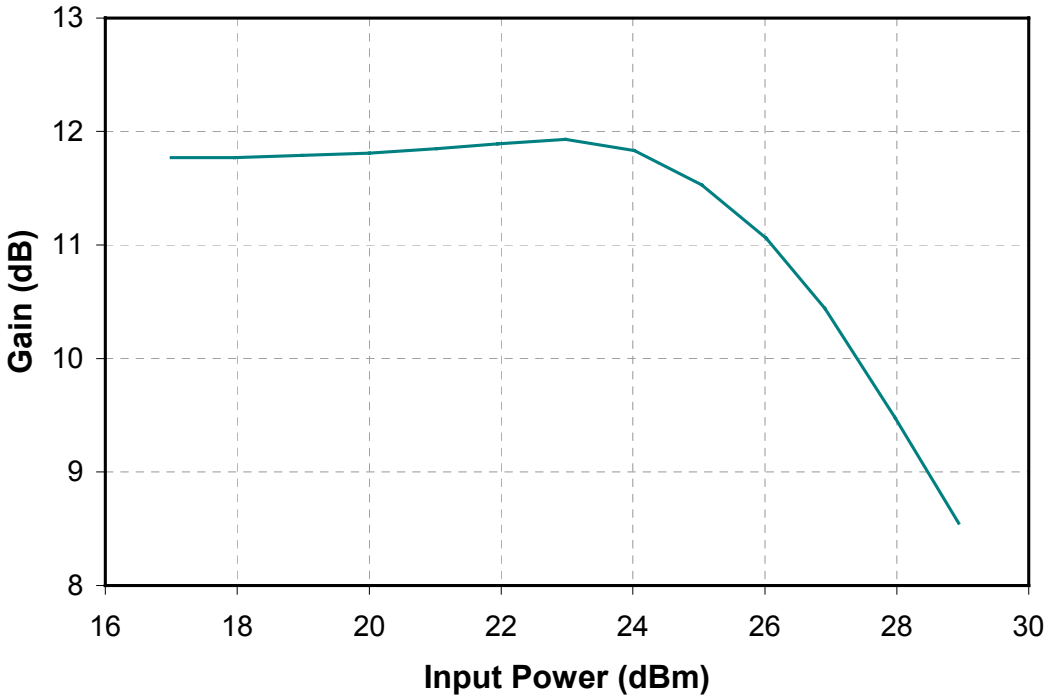

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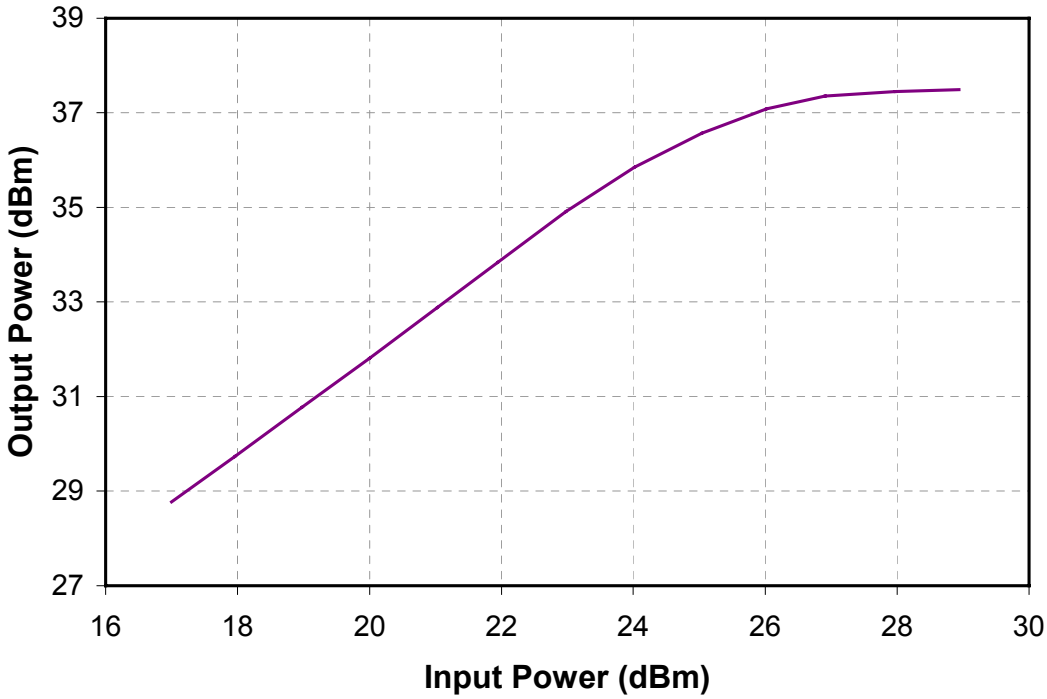

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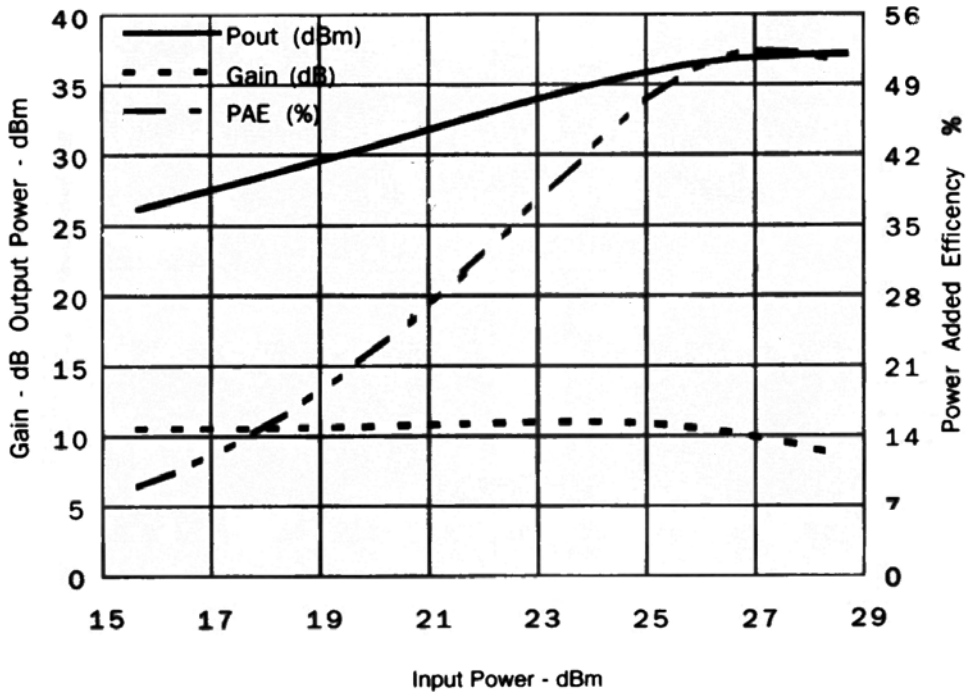
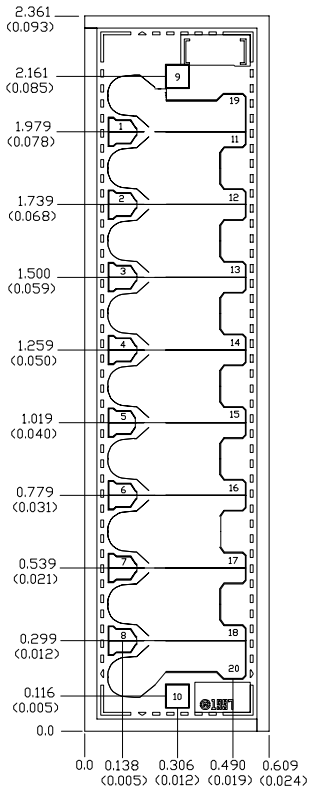


Unmatched Modeled S-Parameter Data for the TGF4260-SCC

FREQ (GHz)	S11 MAG dB	ANG (°) deg	S21 MAG dB	ANG (°) deg	S12 MAG dB	ANG (°) deg	S22 MAG dB	ANG (°) deg
0.5	-0.377	-142.378	16.279	105.604	-35.345	18.236	-2.334	-175.122
1.0	-0.368	-160.678	10.599	93.104	-35.031	9.671	-2.176	-176.556
1.5	-0.364	-167.064	7.118	86.611	-35.026	6.854	-2.126	-176.745
2.0	-0.360	-170.296	4.606	81.733	-35.090	5.622	-2.086	-176.594
2.5	-0.356	-172.250	2.630	77.536	-35.194	5.098	-2.044	-176.322
3.0	-0.351	-173.564	0.994	73.710	-35.320	5.000	-1.998	-176.008
3.5	-0.346	-174.511	-0.409	70.122	-35.473	5.217	-1.947	-175.688
4.0	-0.340	-175.232	-1.643	66.712	-35.645	5.705	-1.892	-175.382
4.5	-0.333	-175.802	-2.750	63.445	-35.831	6.448	-1.834	-175.099
5.0	-0.327	-176.269	-3.756	60.305	-36.027	7.442	-1.774	-174.846
5.5	-0.320	-176.662	-4.682	57.281	-36.233	8.690	-1.712	-174.627
6.0	-0.313	-177.000	-5.543	54.367	-36.444	10.198	-1.648	-174.441
6.5	-0.305	-177.297	-6.349	51.559	-36.648	11.968	-1.585	-174.290
7.0	-0.298	-177.562	-7.108	48.855	-36.845	14.002	-1.522	-174.172
7.5	-0.290	-177.803	-7.828	46.254	-37.028	16.295	-1.459	-174.084
8.0	-0.283	-178.025	-8.513	43.753	-37.190	18.833	-1.398	-174.026
8.5	-0.276	-178.231	-9.167	41.353	-37.323	21.596	-1.338	-173.995
9.0	-0.269	-178.424	-9.794	39.050	-37.419	24.556	-1.280	-173.988
9.5	-0.262	-178.607	-10.398	36.846	-37.484	27.673	-1.224	-174.004
10	-0.255	-178.782	-10.979	34.737	-37.503	30.902	-1.170	-174.039
10.5	-0.249	-178.949	-11.540	32.724	-37.477	34.192	-1.119	-174.091
11.0	-0.242	-179.110	-12.084	30.804	-37.406	37.493	-1.069	-174.160
11.5	-0.236	-179.266	-12.611	28.976	-37.291	40.755	-1.022	-174.241
12.0	-0.230	-179.417	-13.124	27.239	-37.140	43.932	-0.977	-174.335
12.5	-0.225	-179.564	-13.622	25.593	-36.948	46.987	-0.934	-174.438
13.0	-0.219	-179.708	-14.107	24.034	-36.719	49.893	-0.893	-174.551
13.5	-0.214	-179.848	-14.581	22.563	-36.472	52.628	-0.854	-174.670
14.0	-0.209	-179.986	-15.043	21.177	-36.199	55.182	-0.817	-174.796

Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond Pad #1 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #11 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #2 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #12 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #3 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #13 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #4 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #14 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #5 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #15 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #6 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #16 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #7 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #17 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #8 (gate)	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #18 (drain)	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #9 (gate)*	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #19 (drain)*	0.084 x 0.084 (0.003 x 0.003)
Bond Pad #10 (gate)*	0.075 x 0.075 (0.003 x 0.003)	Bond Pad #20 (drain)*	0.084 x 0.084 (0.003 x 0.003)

Minimum connections to Bond pads 1 to 8 and 11 to 18.
Sources are connected to backside metalization.
*Alternate gate and drain pads used for paralleling TGF4260's or for multiple gate wires.

NOTE: Gate bias supplies should be designed to sink or source gate current. The magnitude and direction of the gate current is a function of bias point, load impedence, and drive level.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handing, assembly and test.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

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Note: Die are shipped in gel pack unless otherwise specified.