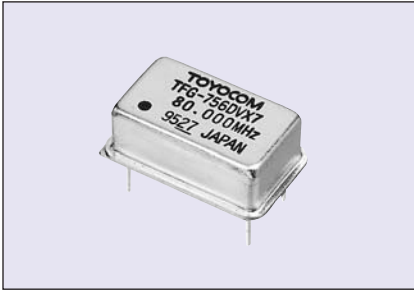


Crystal Clock Oscillator



TFG-756DVX7

FULL DIP Double-Sealed VCXO

Features

- CMOS logic output
- DIP-14 pin package compatible
- Hermetically double-sealed metal package
- Voltage controlled oscillator

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating
Supply voltage	V_{CC}	-0.5 to +7.0 V
Input voltage	V_{IN}	-0.5 to $V_{CC}+0.5$ V
Output voltage	V_O	-0.5 to $V_{CC}+0.5$ V
Output current	I_O	± 20 mA
Storage temperature	T_{stg}	-40 to +85 °C

Parameter		TFG-756DVX7	Conditions
Frequency	f_o	40 to 100 MHz	
Frequency Stability	$\Delta f/f_o$	± 50 ppm max.	(*1)
Pullability		± 150 ppm min.	at $V_{cont}=0$ to +5.0V, $Ref=+2.5$ V
Control Voltage Range	V_{cont}	+2.5 V ± 2.5 V	DC, Pin #1
Operating Temperature	T_{opr}	0 °C to +70 °C	
Supply Voltage	V_{CC}	+5.0 V $\pm 5\%$	DC, Pin #14
Supply Current	I_{CC}	See Table A (max.)	$V_{CC}=+5.25$ V
Output Voltage	V_{OH} V_{OL}	$V_{OH}=V_{CC}-0.5$ V min. / $V_{OL}=+0.5$ V max.	$I_{OH}=-4$ mA Pin #8 $I_{OL}=+4$ mA
Symmetry	SYM	40 to 60 %	at 50% V_{CC}
Rise/Fall time	t_r/t_f	See Table A (max.)	at 20% to 80% V_{CC}
Load Capacitance	C_L	30 pF max.	
Start-up time	t_{st}	4 ms max.	

*1 Inclusive of calibration tolerance at +25°C, operating temperature, operating voltage range.

*2 Rise time (0 to +4.75V) of $V_{CC} > 150\mu s$

Package Outlines [Dimensions in mm]

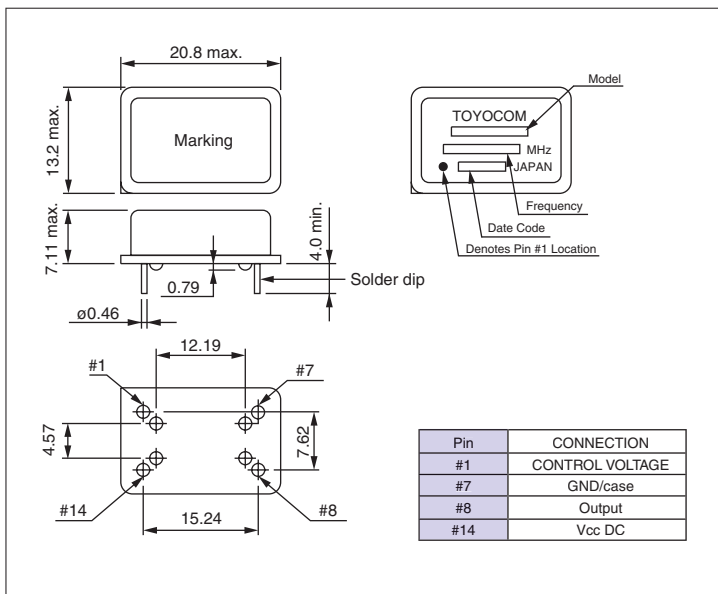


Table A

Freq. (MHz)	$40 \leq f_o$ $f_o \leq 60$	$60 < f_o$ $f_o \leq 100$
I_{CC} (mA)	50	60
t_r, t_f (ns)	4	3

Test Circuit

See Test Circuit page TEST-7