

TC74AC299P, TC74AC299F, TC74AC299FW

8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74AC299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

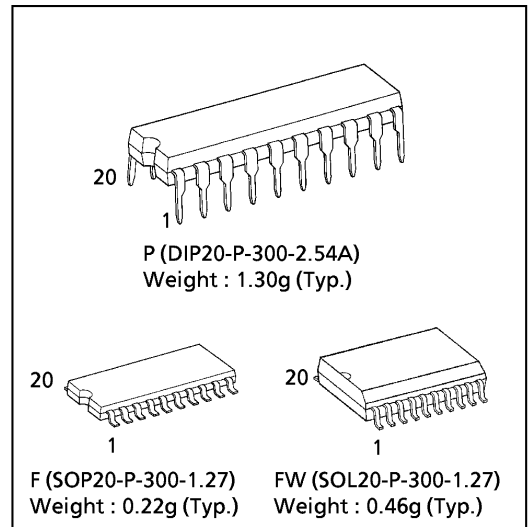
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

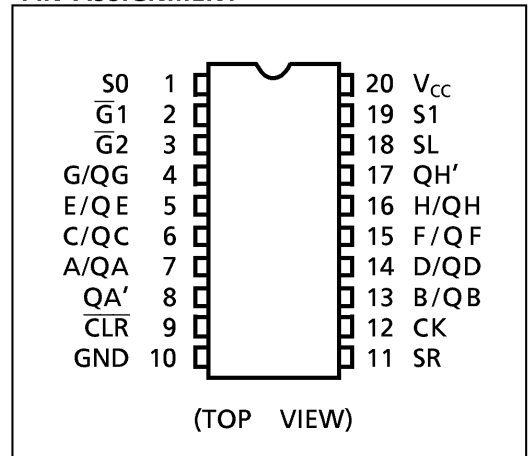
When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

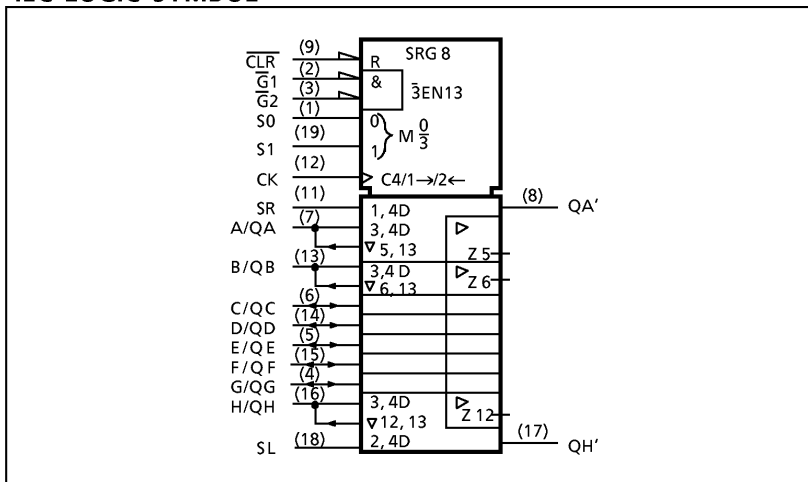
- High Speed..... $f_{MAX} = 150\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.... $V_{CC} \text{ (opr)} = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F299



PIN ASSIGNMENT



IEC LOGIC SYMBOL



APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

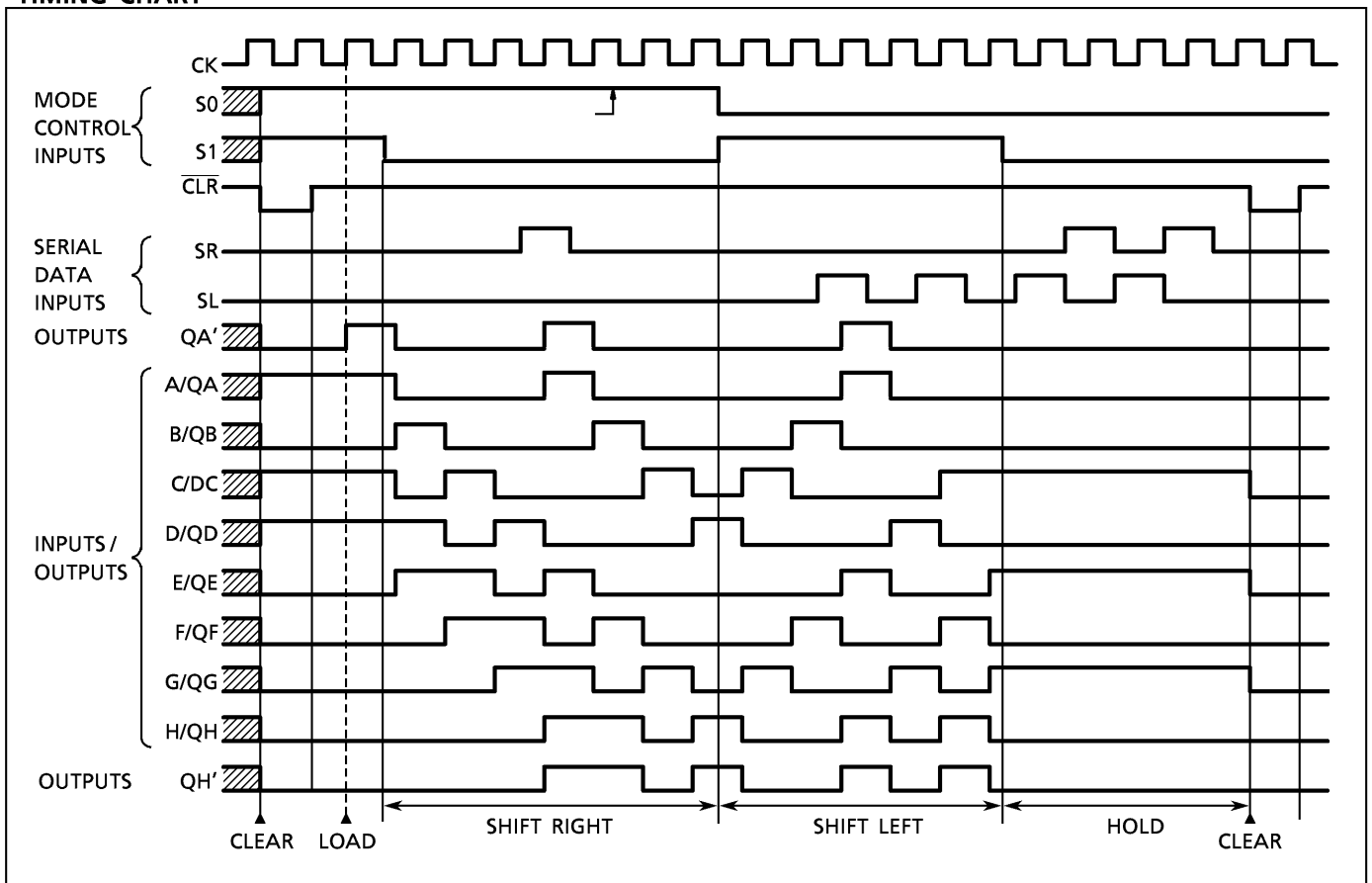
TRUTH TABLE

MODE	INPUTS								INPUTS/OUTPUTS		OUTPUTS	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*		SL	SR				
CLEAR	L	H	H	X	X	X	X	X	Z	Z	L	L
	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓	X	H	H	QGn	H	QGn
	H	L	H	L	L	↑	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓	H	X	QBn	H	QBn	H
	H	H	L	L	L	↑	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↑	X	X	a	h	a	h

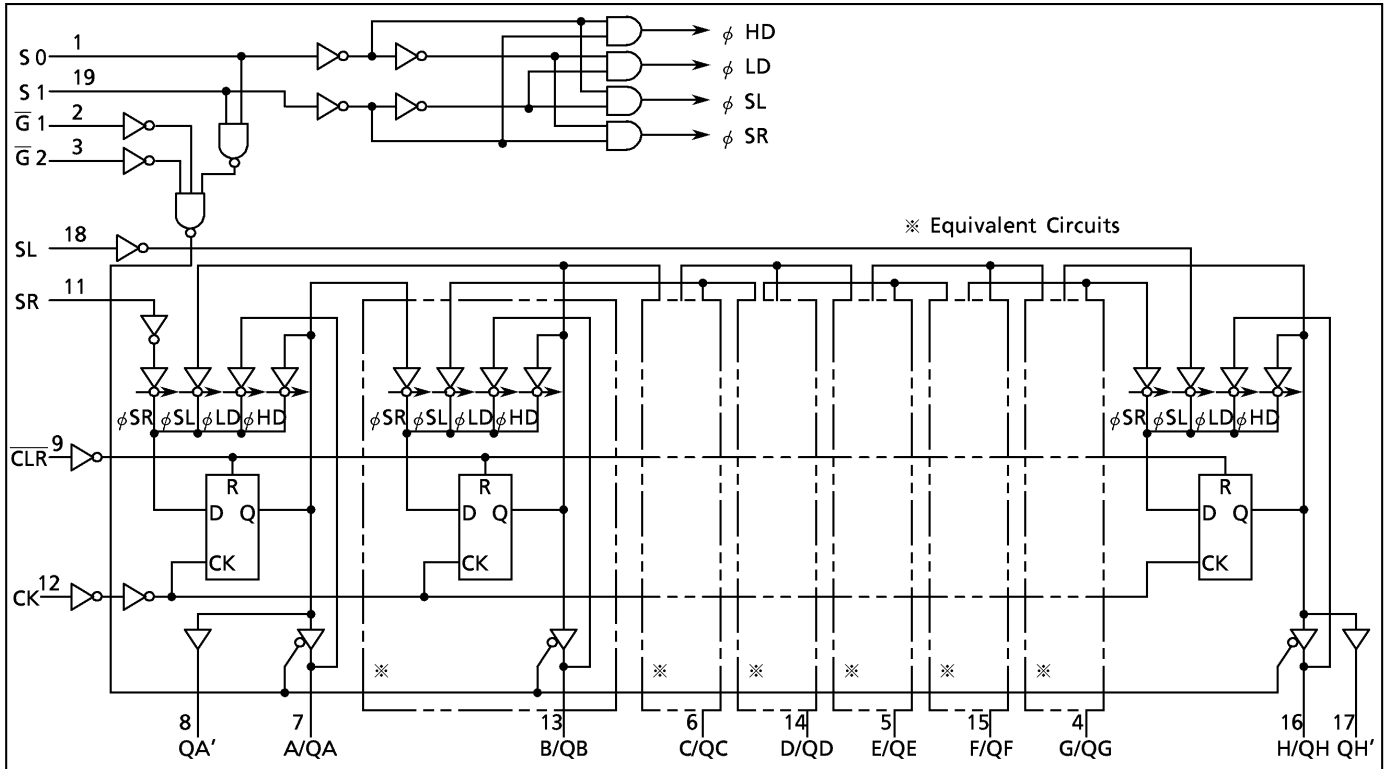
* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

- Z : High Impedance
- Qn0 : The level of Qn before the indicated steady - state input conditions were established.
- Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.
- a, h : The level of the steady - state inputs A, H, respectively.
- X : Don't Care.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 250	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise and Fall Time	dt/dV	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	I _{OL} = 12mA I _{OL} = 24mA I _{OL} = 75mA*	2.0	—	—	±0.5	—	±5.0	μA
				3.0	—	—	±0.1	—	±1.0	
				5.5	—	—	8.0	—	80.0	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	μA	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING RECOMMENDED OPERATING CONDITIONS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C	Ta = -40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _W (L) t _W (H)		3.3 ± 0.3	8.0	8.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum Pulse Width (CLR)	t _W (L)		3.3 ± 0.3	7.0	7.0	
			5.0 ± 0.5	5.0	5.0	
Minimum Set - up Time (SL, SR, A~H)	t _s		3.3 ± 0.3	6.0	6.0	
			5.0 ± 0.5	4.0	4.0	
Minimum Set - up Time (S0, S1)	t _s		3.3 ± 0.3	11.9	13.6	
			5.0 ± 0.5	7.0	7.0	
Minimum Hold Time (SL, SR, A~H)	t _h		3.3 ± 0.3	1.0	1.0	
			5.0 ± 0.5	1.0	1.0	
Minimum Hold Time (S0, S1)	t _h		3.3 ± 0.3	0.0	0.0	
			5.0 ± 0.5	0.0	0.0	
Minimum Removal Time (CLR)	t _{rem}		3.3 ± 0.3	5.0	5.0	
			5.0 ± 0.5	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-QA', QH')	t _{pLH} t _{pHL}		3.3 ± 0.3	—	10.6	18.4	1.0	21.0	ns
			5.0 ± 0.5	—	6.8	10.5	1.0	12.0	
Propagation Delay Time ($\overline{\text{CLR}}$ -QA', QH')	t _{pLH} t _{pHL}		3.3 ± 0.3	—	8.1	14.0	1.0	16.0	
			5.0 ± 0.5	—	6.1	9.2	1.0	10.5	
Propagation Delay Time (CK-QA ~ QH)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	10.9	19.3	1.0	22.0	
			5.0 ± 0.5	—	7.3	10.5	1.0	12.0	
Propagation Delay Time ($\overline{\text{CLR}}$ -QA ~ QH)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	9.8	16.7	1.0	19.0	
			5.0 ± 0.5	—	6.7	10.9	1.0	12.4	
Output Enable Time	t _{pZL} t _{pZH}		3.3 ± 0.3	—	9.9	17.5	1.0	20.0	
			5.0 ± 0.5	—	6.6	9.6	1.0	11.0	
Output Disable Time	t _{pLZ} t _{pHZ}		3.3 ± 0.3	—	8.1	14.0	1.0	16.0	
			5.0 ± 0.5	—	6.4	9.6	1.0	11.0	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	45	90	—	45	—	MHz
			5.0 ± 0.5	80	140	—	80	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Bus Input Capacitance	C _{I/O}			—	13	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)			—	137	—	—	—	

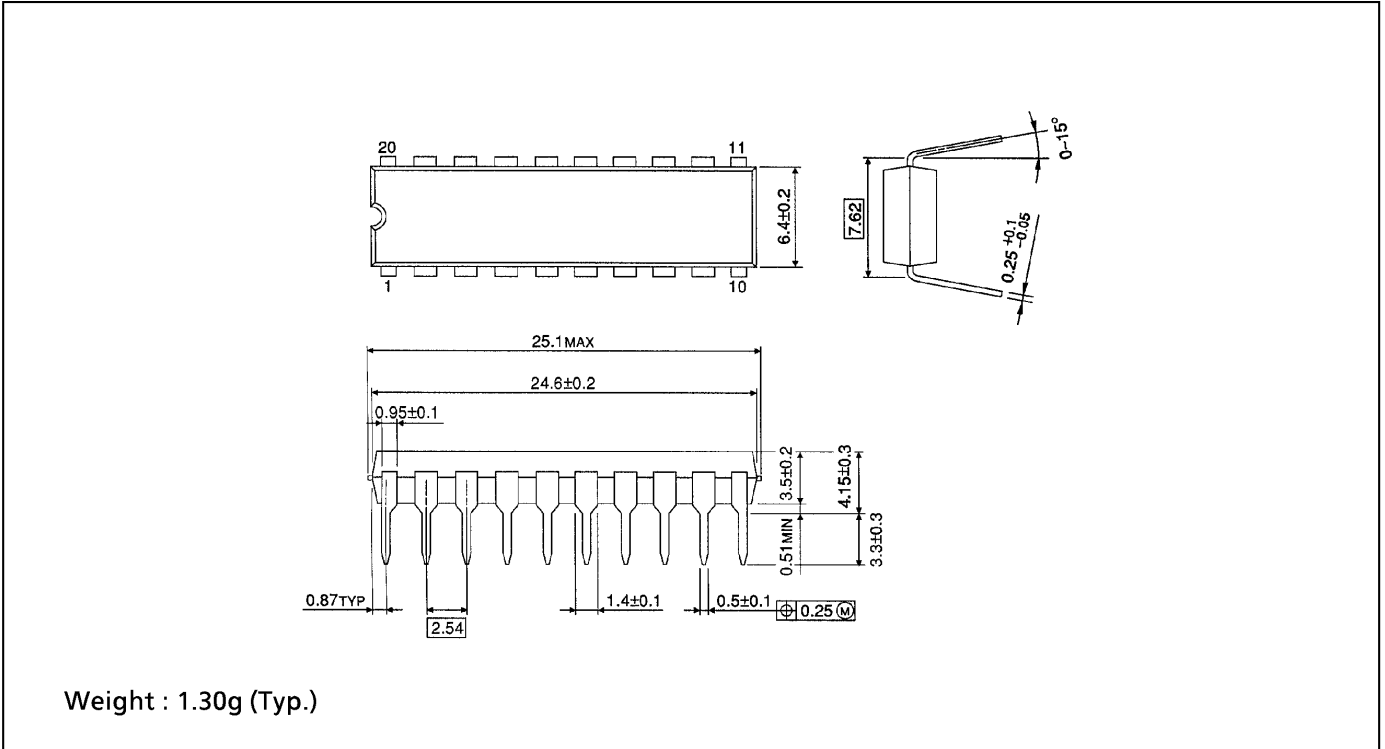
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

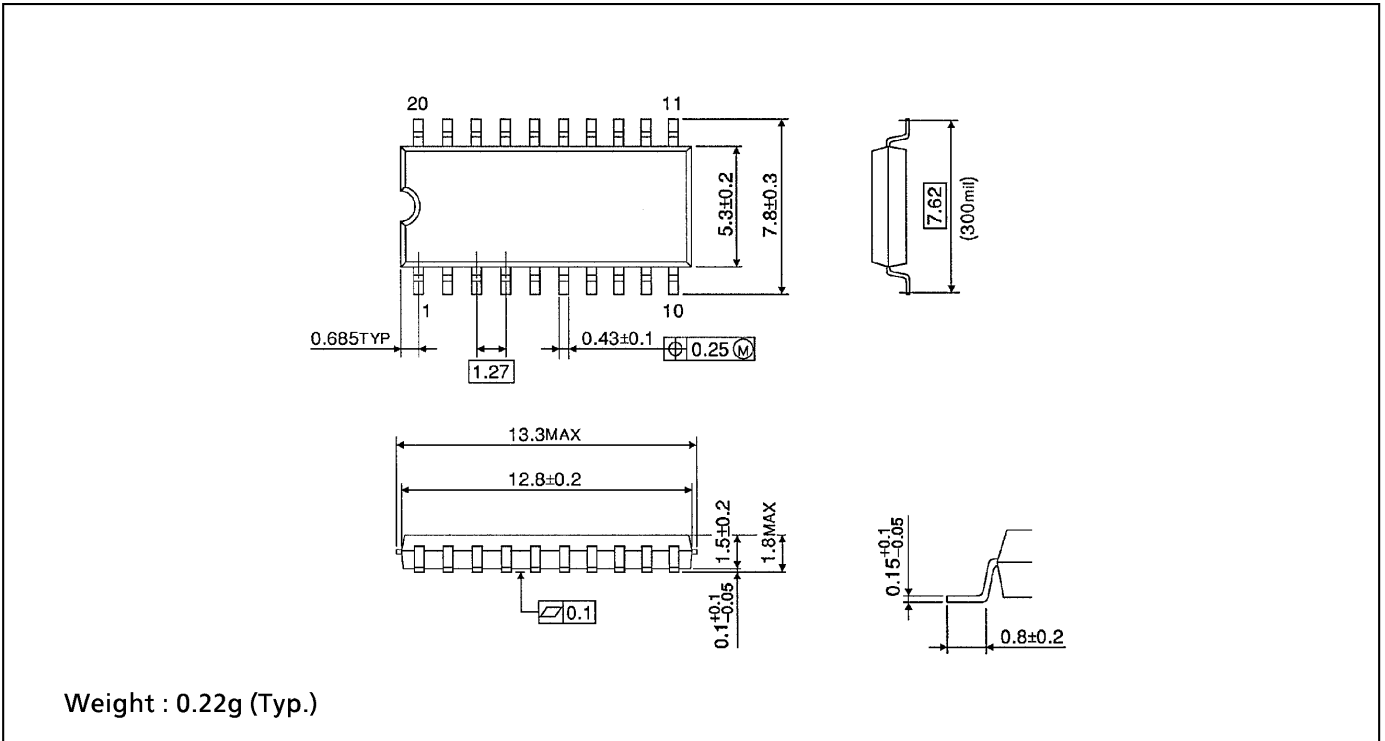
DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

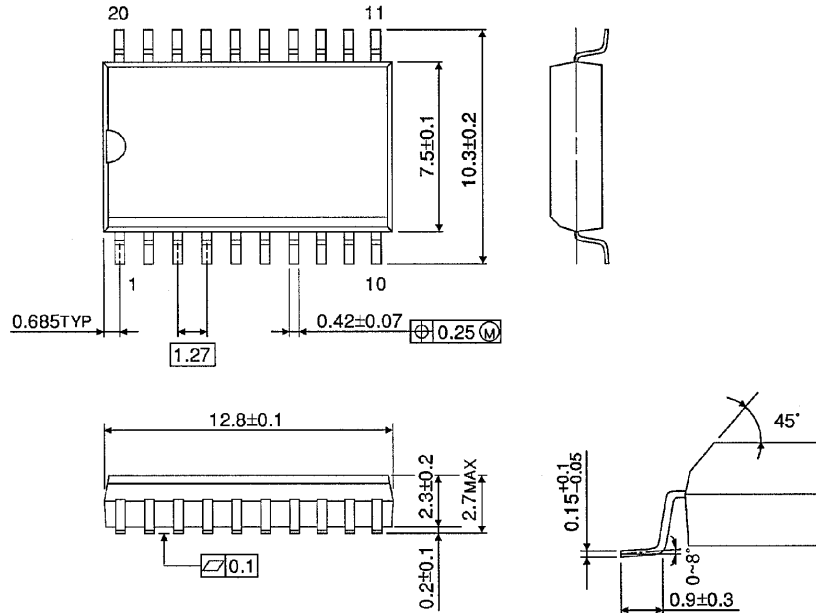
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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