| Preliminary | TOSHIBA CMOS Integrated Circuit   Silicon Monolithic |

TB6575FNG

PWM Sensorless Controller for 3-Phase Full-Wave BLDC Motors

The TB6575FNG provides sensorless commutation and PWM current control for 3-phase full-wave BLDC motors. It controls rotation speed by changing a PWM duty cycle by analog voltage.

Features

- 3-phase full-wave sensorless drive
- PWM chopper drive
- PWM duty cycle control by analog input
- 20-mA current sink capability on PWM output pins
- Overcurrent protection
- Forward/reverse rotation
- Lead angle control (7.5° and 15°)
- Overlap commutation
- Rotation speed sensing signal
- DC excitation mode to improve startup characteristic
- DC excitation time and forced commutation time for startup operation can be changed.
- Forced commutation frequency can be selected. ($f_{XT}/(6 \times 2^{16})$, $f_{XT}/(6 \times 2^{17})$, $f_{XT}/(6 \times 2^{18})$)
- Output polarity switching (P-channel + N-channel, N-channel + N-channel)

SSOP24-P-300-0.65A
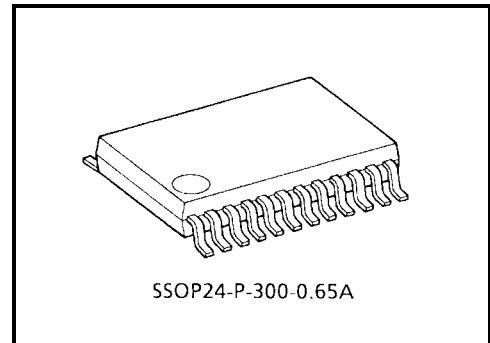
Weight: 0.14 g (typ.)

Block Diagram
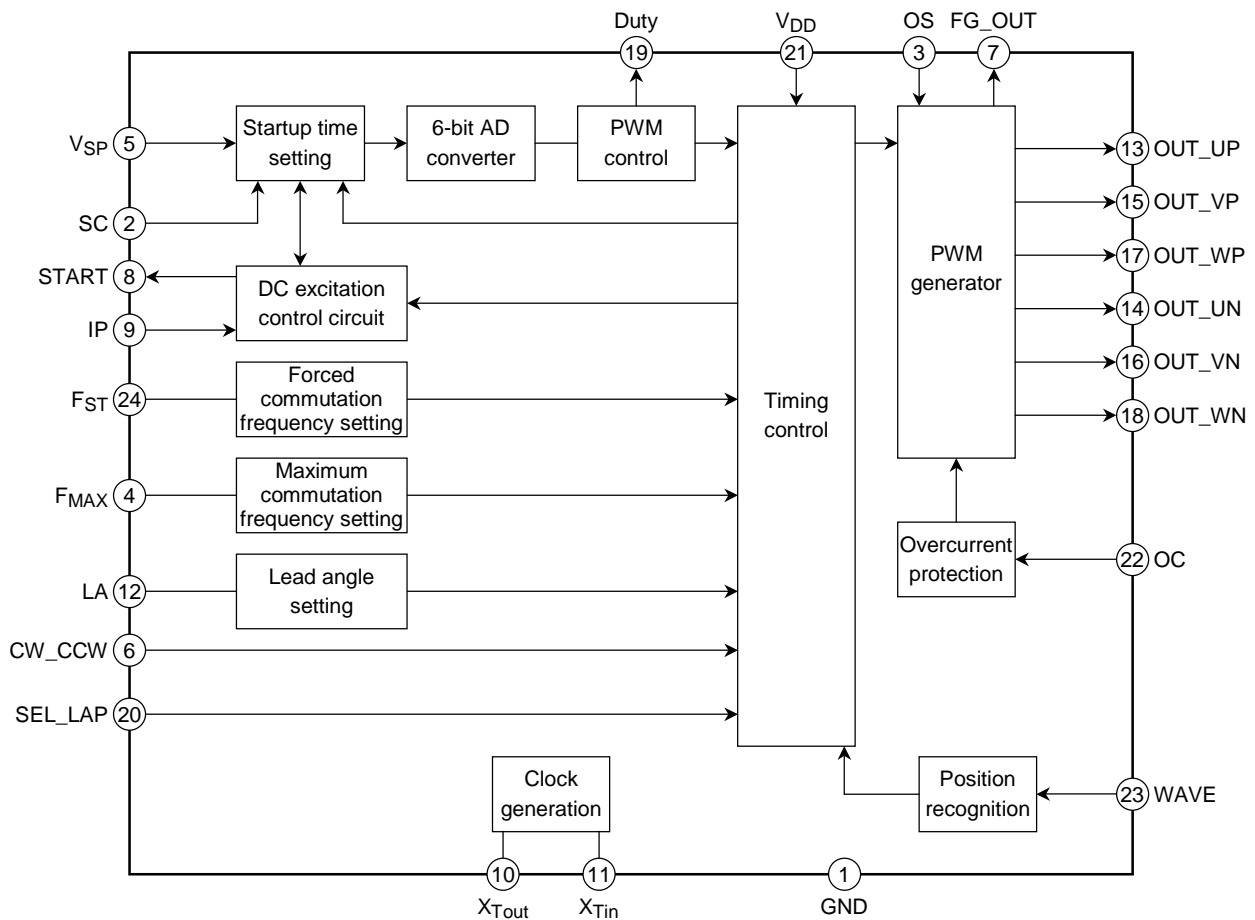
Pin Assignment

GND	1	24	F_{ST}
SC	2	23	WAVE
OS	3	22	OC
F_{MAX}	4	21	V_{DD}
V_{SP}	5	20	SEL_LAP
CW_CCW	6	19	Duty
FG_OUT	7	18	OUT_WN
START	8	17	OUT_WP
IP	9	16	OUT_VN
X_{Tout}	10	15	OUT_VP
X_{Tin}	11	14	OUT_UN
LA	12	13	OUT_UP

Pin Description

Pin No.	Symbol	I/O	Description
1	GND	—	Ground pin
2	SC	I	Connection pin for a capacitor to set a startup commutation time and duty cycle ramp-up time
3	OS	I	Select the polarity of transistors. 　High or open : High-side transistor = P-channel (active low) 　　　　　　　　　Low-side transistor = N-channel (active low) 　Low　　　　　: High-side transistor = N-channel (active low) 　　　　　　　　　Low-side transistor = N-channel (active low) The pin has a pull-up resistor.
4	F_{MAX}	I	Set an upper limit of the maximum commutation frequency. 　High or open : Maximum commutation frequency $f_{MX} = f_{XT}/(6 \times 2^9)$ 　Low　　　　　: Maximum commutation frequency $f_{MX} = f_{XT}/(6 \times 2^{10})$ The pin has a pull-up resistor.
5	V_{SP}	I	Duty cycle control input 　$0 \le V_{SP} \le V_{AD}$ (L): Output off 　V_{AD} (L) $\le V_{SP} \le V_{AD}$ (H): Set the PWM duty cycle according to the analog input. 　V_{AD} (H) $\le V_{SP} \le V_{DD}$: Duty cycle = 100% (31/32) The pin has a pull-down resistor.
6	CW_CCW	I	Rotation direction input 　High　　　　　: Reverse rotation (U → W → V) 　Low or open : Forward rotation (U → V → W) The pin has a pull-down resistor.
7	FG_OUT	O	Rotation speed sensing output 　The pin is low at startup or upon a detection of a fault. This pin drives three pulses per rotation (3 ppr) based on the back-EMF (electromotive force) sensing. (In the case of 4 pole motor, 6 pulse output per rotation.)
8	START	O	DC excitation time setting pins 　When $V_{SP} \ge 1$ V (typ.), the START pin goes low to start DC excitation.
9	IP	I	After the IP pin reaches $V_{DD}/2$, the TB6575FNG moves from DC excitation to forced commutation mode.
10	X_T	—	Connection pins for a crystal oscillator
11	X_{Tin}	—	These pins have a feedback resistor.
12	LA	I	Lead angle control input 　LA = Low or open : Lead angle of 7.5° 　LA = high　　　 : Lead angle of 15° The pin has a pull-down resistor.
13	OUT_UP	O	PWM output signal for the high-side (positive-side) transistor driving motor phase U 　The PWM polarity can be specified by pin 3.
14	OUT_UN	O	PWM output signal for the low-side (negative-side) transistor driving motor phase U 　This signal is active high.
15	OUT_VP	O	PWM output signal for the high-side (positive-side) transistor driving motor phase V 　The PWM polarity can be specified by pin 3.
16	OUT_VN	O	PWM output signal for the low-side (negative-side) transistor driving motor phase V 　This signal is active high.
17	OUT_WP	O	PWM output signal for the high-side (positive-side) transistor driving motor phase W 　The PWM polarity can be specified by pin 3.
18	OUT_WN	O	PWM output signal for the low-side (negative-side) transistor driving motor phase W 　This signal is active high.
19	Duty	O	PWM output monitor pin 　This pin drives PWM output whose duty cycle corresponds to the V_{SP} input. It also reflects the information at the OC pin.
20	SEL_LAP	I	Overlap commutation select pin 　Low: Overlap commutation　　　　High: 120° commutation The pin has a pull-up resistor.
21	V_{DD}	—	5-V power supply pin
22	OC	I	Overcurrent detection input 　The all PWM output signals are stopped when OC $\ge$ 0.5 (V). The pin has a pull-up resistor.

Pin No.	Symbol	I/O	Description
23	WAVE	I	Position sensing input 3-phase voltage is applied to this pin. The pin has a pull-up resistor.
24	F_{ST}	I	Forced commutation frequency select pin High or open: Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{16})$ Middle : Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{17})$ Low : Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{18})$ The pin has a pull-up resistor.

Functional Description

1. Sensorless drive

On receiving an analog voltage command input, the rotor is aligned to a known position in DC excitation mode, and then the rotation is started in forced commutation mode by applying a PWM signal to the motor. As the rotor moves, back-EMF is acquired.

When a signal indicating the polarity of each of the phase voltages including back-EMF is applied to the position signal input pin, automatic switching occurs from the forced commutation PWM signal to the natural commutation PWM signal (which is generated based on the back-EMF sensing) to drive a BLDC motor in sensorless mode.

2. Startup operation

When the motor is stationary, there is no back-EMF and the motor position is unknown. For this reason, the rotor is aligned to a known position in DC excitation mode and then the rotation is started in forced commutation mode. An external capacitor sets the times that the TB6575FNG stays in DC excitation and forced commutation modes. Those times vary depending on the motor type and motor loading. Thus, they must be adjusted experimentally.

(a): DC excitation period : T_{FIX} (typ.) $= 0.69 \times C1 \times R1$ (s)
(b): Forced commutation period
T_{UP} (typ.) $= C1 \times V_{SP}/3.8\ \mu A$ (s)
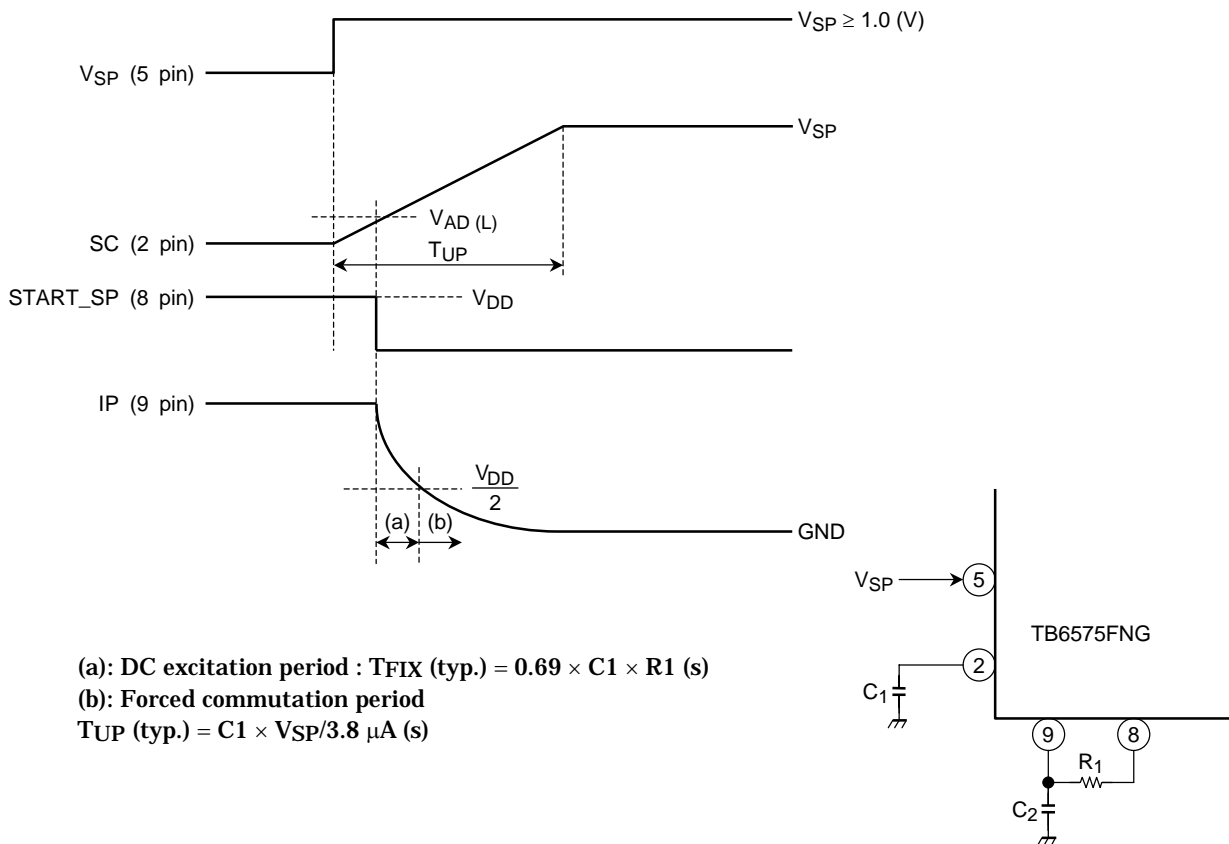
The rotor is aligned to a known position in DC excitation mode for period (a), during which the IP pin voltage decreases to half V_{DD} level. The time constant for the period is determined by C and R_1. After that, switching occurs to forced commutation mode represented by (b). The duty cycles for DC excitation

and forced commutation modes are determined according to the SC pin voltage. When a measurable back-EMF is detected, the motor switches to sensorless mode. The duty cycle for sensorless mode is determined by the V_{SP} value.

3. Forced commutation frequency

The forced commutation frequency for startup operation is set as follows.

The optimal frequency varies depending on the motor type and motor loading. Thus, It must be adjusted experimentally.

F_{ST} = High or Open : Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{16})$
F_{ST} = Middle   : Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{17})$
F_{ST} = Low   : Forced commutation frequency $f_{ST} = f_{XT}/(6 \times 2^{18})$
* f_{XT}: Crystal oscillator frequency

4. PWM frequency

The PWM frequency is determined by an external oscillator.

PWM frequency (f_{PWM}) = $f_{XT}/256$
* f_{XT}: Crystal oscillator frequency

The PWM frequency must be sufficiently high, compared with the electrical frequency of the motor and within the switching performance of the transistors.

OS = High or Open

PWM signal driving high-side transistors

PWM signal driving low-side transistors

Motor pin voltage
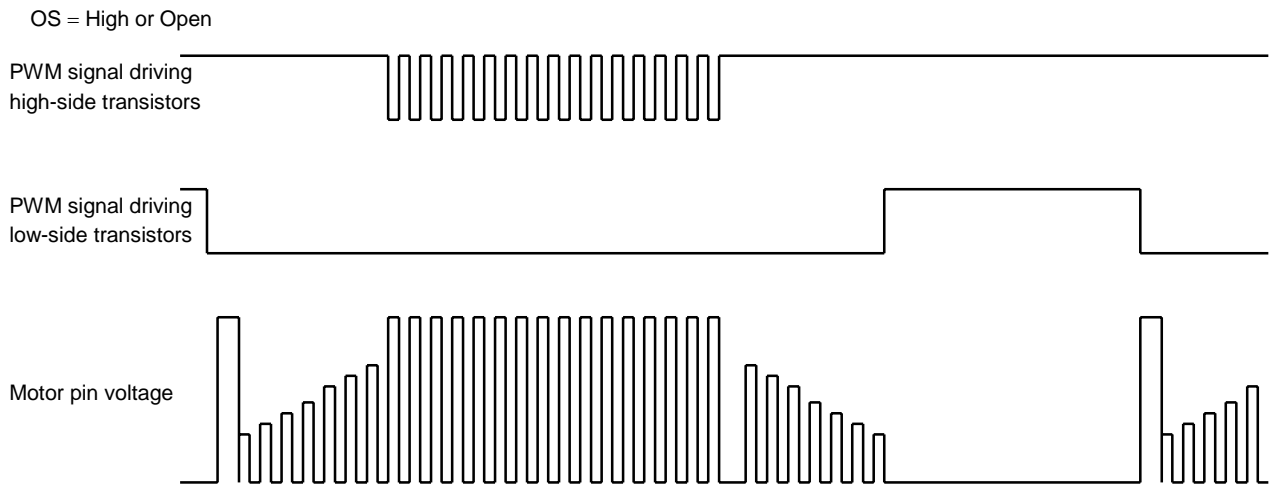
5. Speed control V_{SP} pin

An analog voltage applied to the V_{SP} pin is converted by the 6-bit AD converter to control the duty cycle of the PWM.

$0 \leq V_{DUTY} \leq V_{AD}$ (L)
  → Duty cycle = 0%
V_{AD} (L) $\leq V_{DUTY} \leq V_{AD}$ (H)
  → Figure at the right (1/64 to 63/64)
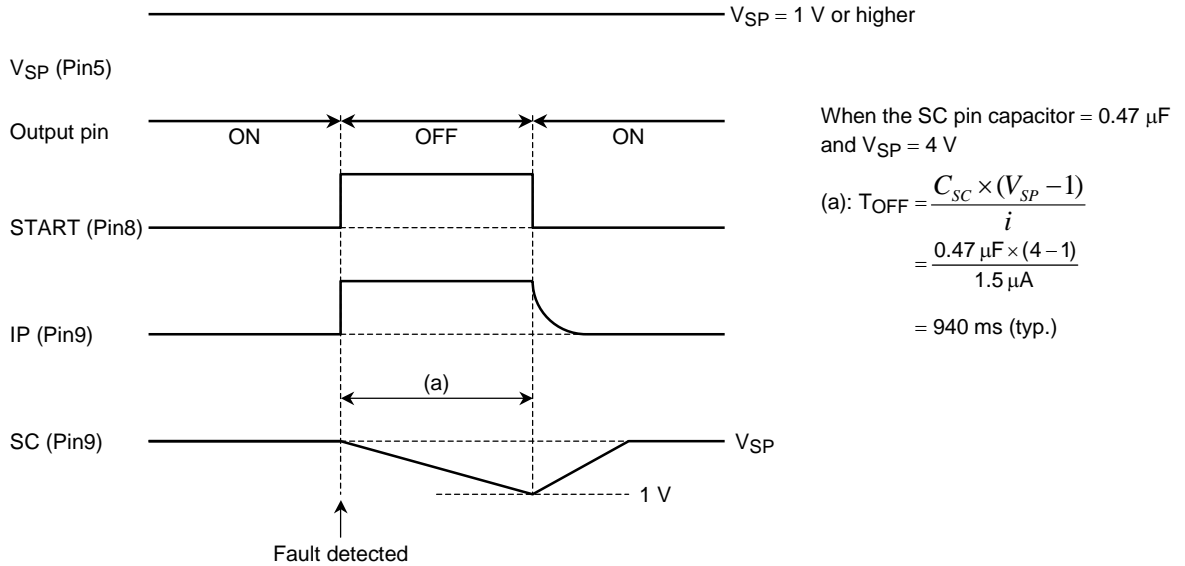V_{AD} (H) $\leq V_{DUTY} \leq V_{DD}$
  → Duty cycle = 100% (63/64)

Duty cycle

100%

0%

VAD (L)
1 V (typ.)

VAD (H)
4 V (typ.)

VSP
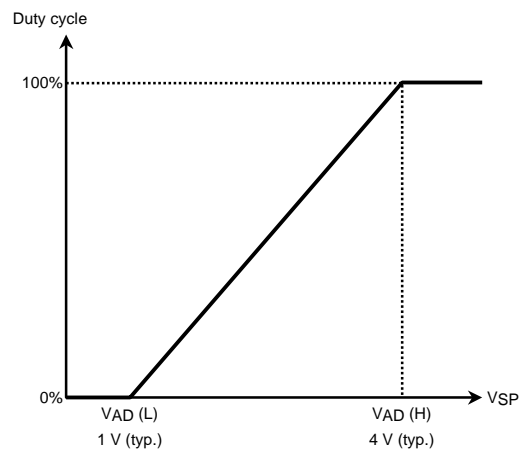
6. Fault protection

When a signal indicating the following faults is applied to the WAVE pin, the output transistors are disabled. After about one second, the motor is restarted. This operation is repeated as long as a fault is detected.

- The maximum commutation frequency is exceeded.
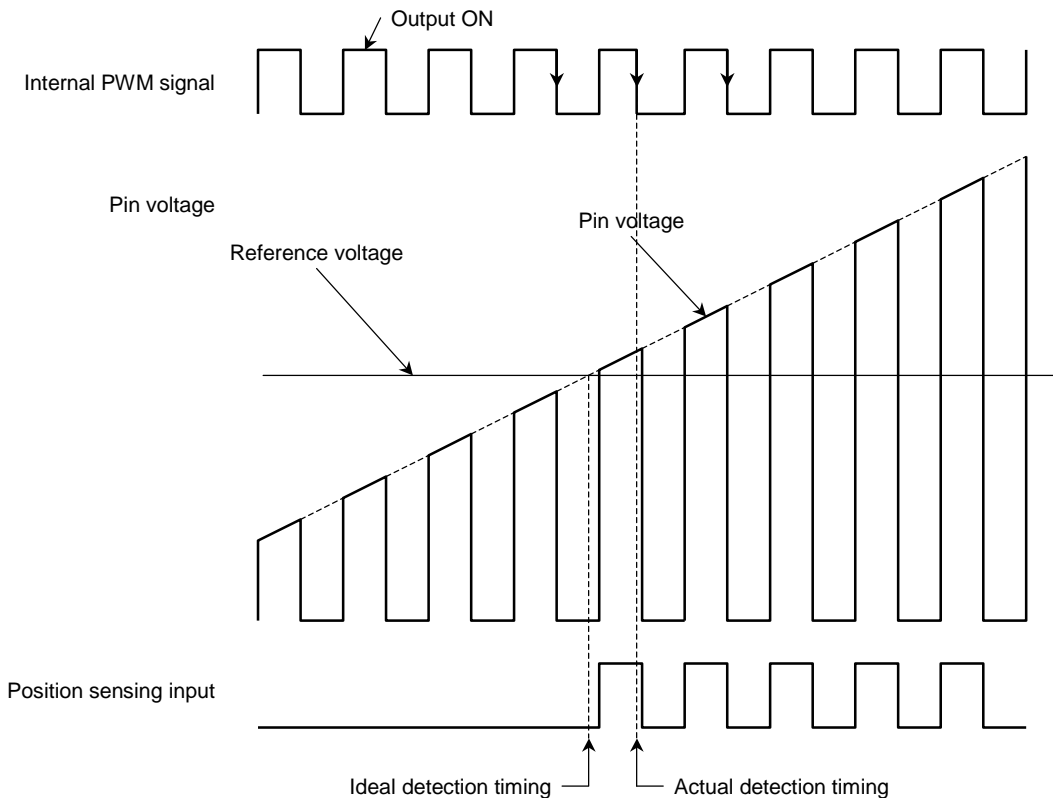- The rotation speed falls below the forced commutation frequency.

V_{SP} = 1 V or higher

V_{SP} (Pin5)

Output pin — ON — OFF — ON

START (Pin8)

IP (Pin9)

(a)

SC (Pin9) — V_{SP} — 1 V

Fault detected

When the SC pin capacitor = 0.47 μF and V_{SP} = 4 V

$$(a): T_{OFF} = \frac{C_{SC} \times (V_{SP} - 1)}{i}$$

$$= \frac{0.47\,\mu F \times (4 - 1)}{1.5\,\mu A}$$

$$= 940\ ms\ (typ.)$$

7. Motor position detection error

A position detection is synchronized with the PWM signal generated in the IC. Thus, a position detection error relative to the PWM signal frequency may occur. Keep this in mind especially when the TB6575FNG is used for a high-speed motor.

A detection is performed on the falling edge of the PWM signal. An error is recognized when the pin voltage exceeds the reference voltage.

Detection error time < $1/f_p$ f_p: PWM frequency = $f_{XT}/256$ f_{XT}: Crystal oscillator frequency

Output ON

Internal PWM signal

Pin voltage

Pin voltage

Reference voltage

Position sensing input

Ideal detection timing — Actual detection timing

8. Lead angle control

The motor runs with a lead angle of 0° in forced commutation mode at startup. After switching to natural commutation, the lead angle automatically changes to the value set by the LA pin.

Back-EMF
PWM signal

(1) Lead angle of 0°

OUT_UP
OUT_UN

OUT_VP
OUT_VN

OUT_WP
OUT_WN

(2) Lead angle of 7.5°

OUT_UP
OUT_UN

OUT_VP
OUT_VN

OUT_WP
OUT_WN

(3) Lead angle of 15°

OUT_UP
OUT_UN

OUT_VP
OUT_VN

OUT_WP
OUT_WN

*OS = High
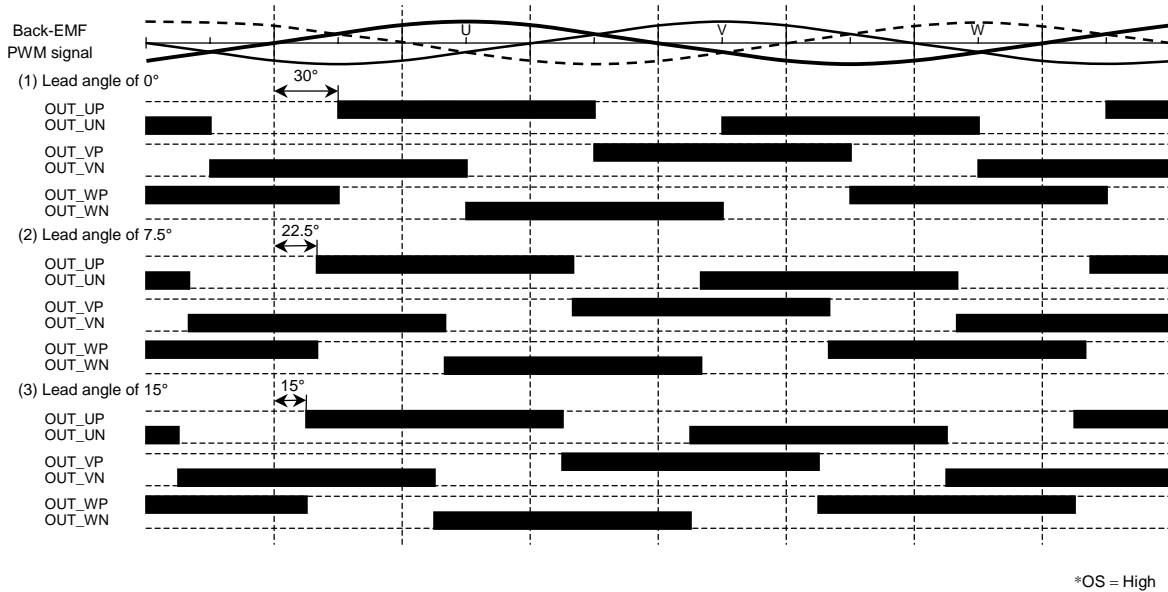
9. Overlap commutation

When SEL_LAP = high, the TB6575FNG is configured to allow for 120° commutation. When SEL_LAP = low, it is configured to allow for overlap commutation. In overlap commutation, there is an overlap period during which both the outgoing transistor and incoming transistor are conducting (as shown in the shaded areas). This period varies according to the lead angle.

Back-EMF
PWM signal

(1) Lead angle of 7.5°

OUT_UP
OUT_UN

OUT_VP
OUT_VN

OUT_WP
OUT_WN

(2) Lead angle of 15°

OUT_UP
OUT_UN

OUT_VP
OUT_VN

OUT_WP
OUT_WN

*OS = High

2004/03/15
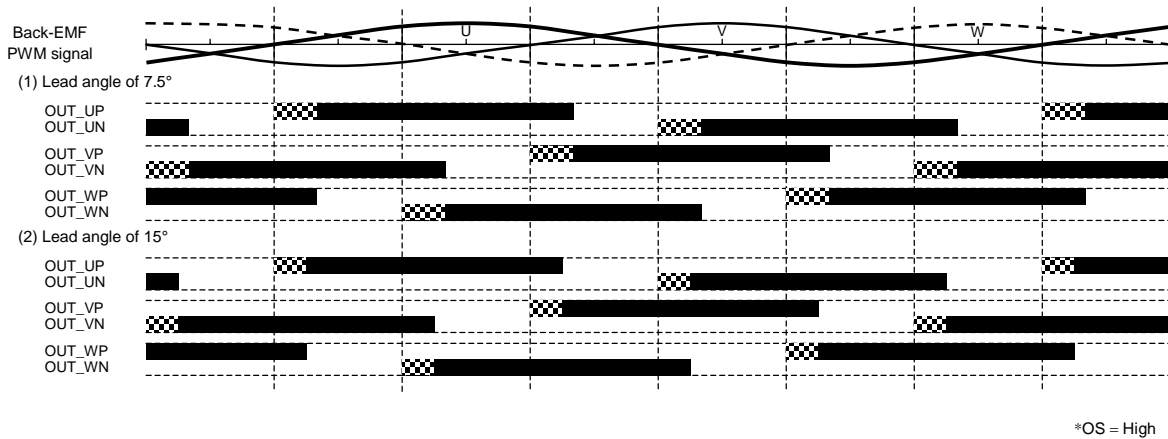
Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	5.5	V
Input voltage	V_{in}	$-0.3 \sim V_{DD} + 0.3$	V
Turn-on signal output current	I_{OUT}	20	mA
Power dissipation	P_D	780 (Note)	mW
Operating temperature	T_{opr}	$-30 \sim 105$	°C
Storage temperature	T_{stg}	$-55 \sim 150$	°C

Note: Without a PCB, stand-alone operation

Recommended Operating Conditions (Ta = −30 to 105°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
Input voltage	V_{in}	—	−0.3	—	$V_{DD} + 0.3$	V
Oscillation frequency	f_{XT}	—	2.0	4.0	8.0	MHz

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Static power supply current	I_{DD}	—	V_{SP} = 0 V, X_{Tin} = H	—	0.7		mA
Dynamic power supply current	$I_{DD\ (opr)}$	—	V_{SP} = 2.5 V, X_{Tin} = 4 MHz, Output open	—	2	6	mA
Input current	I_{IN-1} (H)	—	V_{IN} = 5 V, OC, WAVE, SEL_LAP F_{MAX}, F_{ST}, OS	—	0	1	μA
	I_{IN-1} (L)	—	V_{IN} = 0 V, OC, WAVE, SEL_LAP, F_{MAX}, F_{ST}, OS	−75	−50	—	
	I_{IN-2} (H)	—	V_{IN} = 5 V, CW_CCW, LA, V_{SP}	—	50	75	
	I_{IN-2} (L)	—	V_{IN} = 0 V, CW_CCW, LA, V_{SP}	−1	0	—	
Input voltage	V_{IN-1} (H)	—	OC, SEL_LAP, CW_CCW WAVE, LA, F_{MAX}, OS	3.5	—	5	V
	V_{IN-1} (L)	—	OC, SEL_LAP, CW_CCW WAVE, LA, F_{MAX}, OS	GND	—	1.5	
	V_{IN-2} (H)	—	F_{ST}	4	—	5	
	V_{IN-2} (M)	—	F_{ST}	2	—	3	
	V_{IN-2} (L)	—	F_{ST}	GND	—	1	
Input hysteresis voltage	V_H	—	WAVE,	—	0.45	—	V
Output voltage	V_{O-1} (H)	—	I_{OH} = −2 mA OUT_UP, OUT_VP, OUT_WP	4.5	—	V_{DD}	V
	V_{O-1} (L)	—	I_{OL} = 20 mA OUT_UP, OUT_VP, OUT_WP	GND	—	0.5	
	V_{O-2} (H)	—	I_{OH} = −20 mA OUT_UN, OUT_VN, OUT_WN	4.5	—	V_{DD}	
	V_{O-2} (L)	—	I_{OL} = 2 mA OUT_UN, OUT_VN, OUT_WN	GND	—	0.5	
	V_{O-3} (H)	—	I_{OH} = −0.5 mA FG_OUT	4.5	—	V_{DD}	
	V_{O-3} (L)	—	I_{OL} = 0.5 mA FG_ OUT	GND	—	0.5	
Output leak current	I_L (H)	—	V_{DD} = 5.5 V, V_{OUT} = 0 V OUT_UP, OUT_VP, OUT_WP, OUT_UN, OUT_VN, OUT_WN, FG_OUT	—	0	10	μA
	I_L (L)	—	V_{DD} = 5.5 V, V_{OUT} = 5.5 V OUT_UP, OUT_VP, OUT_WP OUT_UN, OUT_VN, OUT_WN, FG_OUT	—	0	10	
PWM input voltage	V_{AD} (L)	—	V_{SP}	0.8	1.0	1.2	V
	V_{AD} (H)			3.8	4.0	4.2	
C_{SC} charge current	I_{SC}	—	SC	2.6	3.8	5.0	μA
Fault retry time	T_{OFF}	—	V_{SP} = 4 V, SC pin = 0.47 μF	—	940	—	ms
Overcurrent detection voltage	V_{OC}	—	OC	0.46	0.5	0.54	V

Input Equivalent Circuit

1. V_{SP} pin
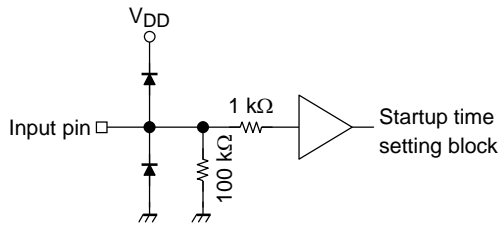
2. SEL_LAP, F_{MAX}, F_{ST}, WAVE and OS pins
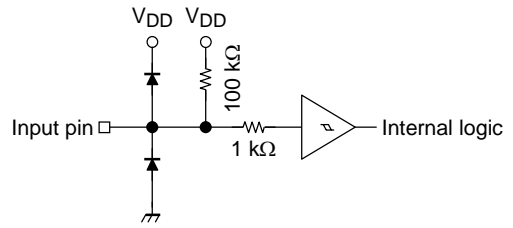
Hysteresis width
WAVE : 450 mV (typ.)
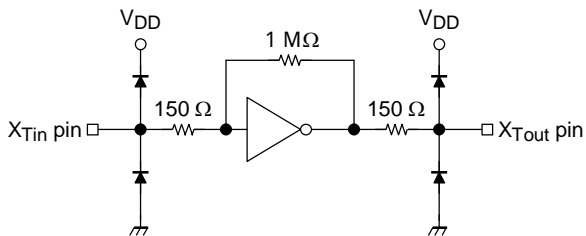
3. LA and CW_CCW pins
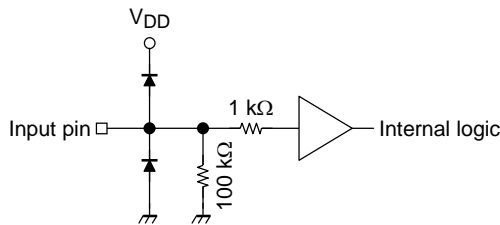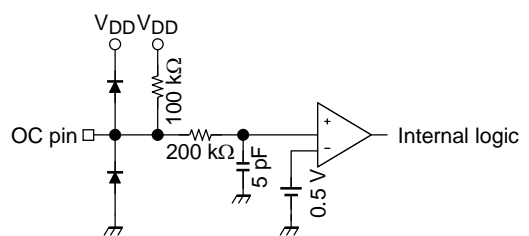

4. OUT_UP, OUT_UN, OUT_VP, OUT_VN,
   OUT_WP, OUT_WN and FG_OUT pins
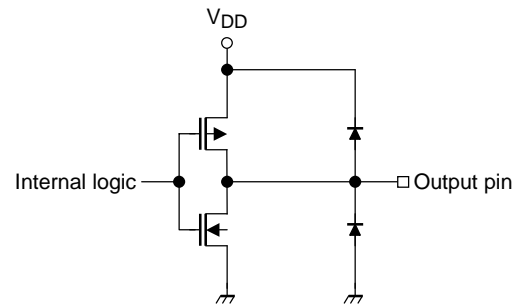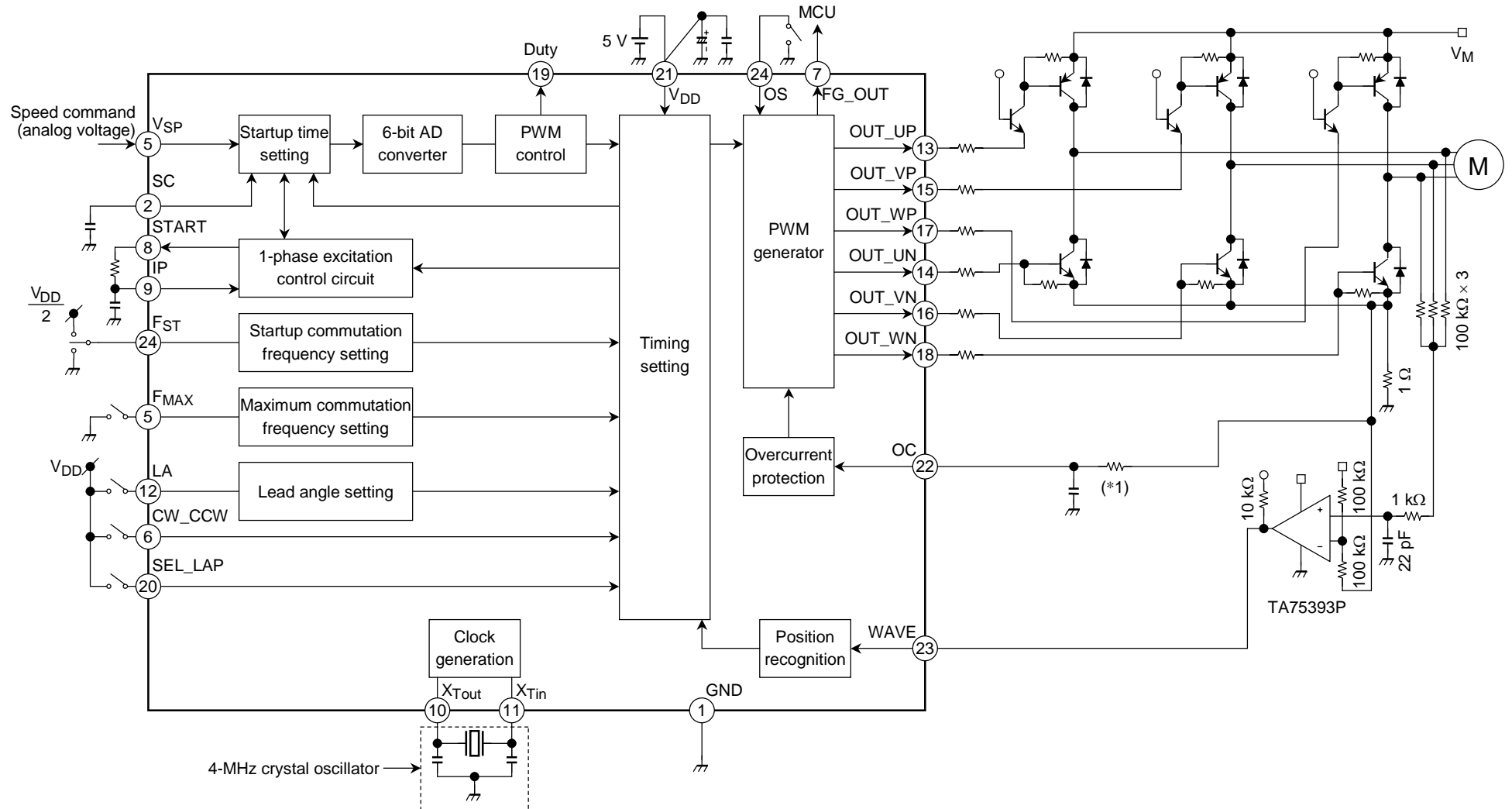

5. X_{Tin} and X_{Tout} pins

6. OC pin

Application Circuit Example

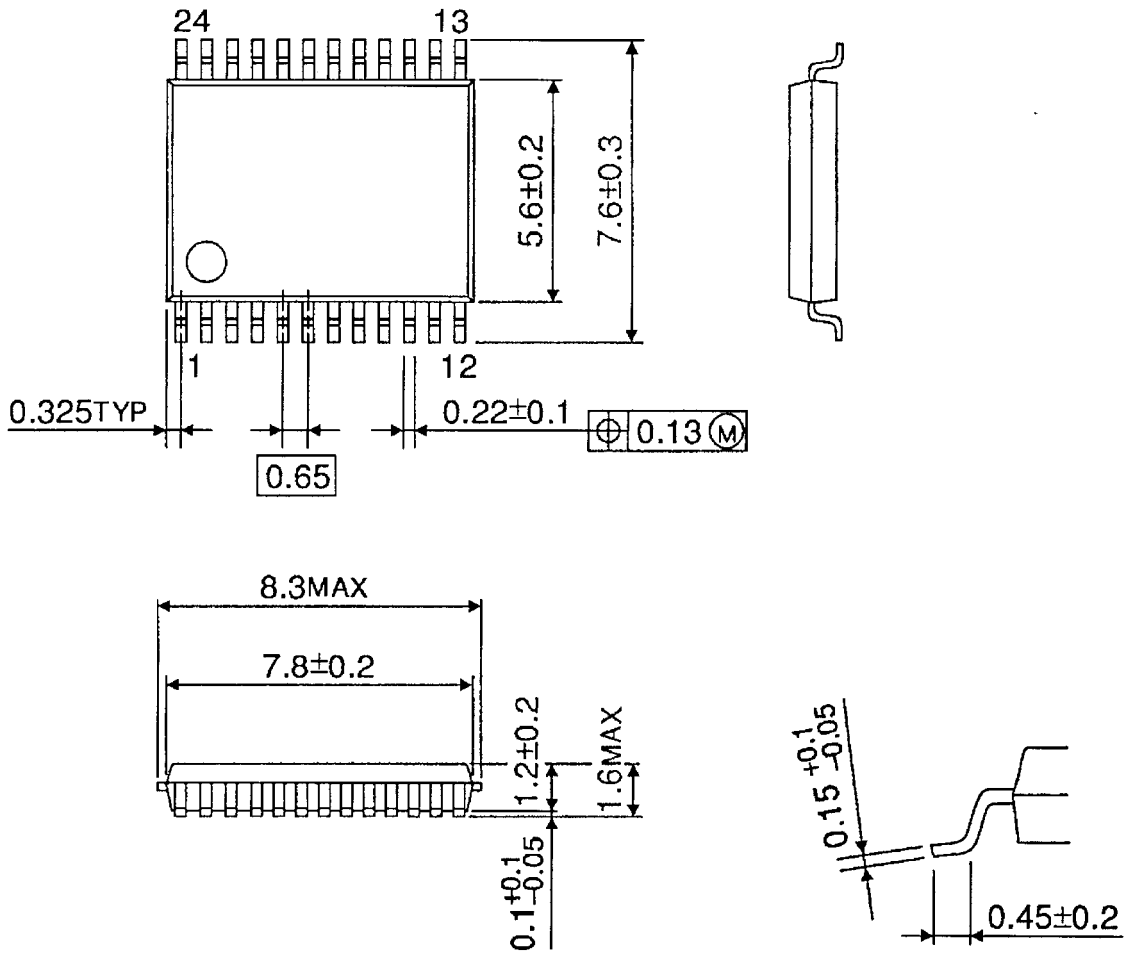Note 1: Because there may be short circuits between outputs, to supply, or to ground, be careful when designing output lines, V_{DD} lines, and ground lines.

Note 2: The above application circuit including component values is reference only. Because the values may vary depending on the motor type, the optimal values must be determined experimentally.

*1: Connect a resistor, if necessary, to prevent malfunction due to noise.

Package Dimensions

SSOP24-P-300-0.65A

Unit : mm

24   13

5.6±0.2   7.6±0.3

1   12

0.325TYP   0.22±0.1   ⊕ | 0.13 Ⓜ

0.65

8.3MAX

7.8±0.2

1.2±0.2   1.6MAX

0.1 +0.1 −0.05

0.15 +0.1 −0.05

0.45±0.2

Weight: 0.14 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA