

# T6C03

## COLUMN AND ROW DRIVER FOR A DOT MATRIX LCD

The T6C03 is a 160-channel-output column and row driver for an STN dot matrix LCD.

The T6C03 features a 42-V LCD drive voltage and an 8-MHz maximum operating frequency. The T6C03 is able to drive LCD panels with a duty ratio of up to 1 / 480.

### Features

- Display duty application : to 1 / 480
- LCD drive signal : 160
- Data transfer : Column: 4 / 8-bit bidirectional  
Row: Single / Dual bidirectional
- Operating frequency : 8 MHz (V<sub>DD</sub> = 5 V ± 10%)
- LCD drive voltage : 14 to 42 V
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 1.3 kΩ (max) (20 V, 1 / 13 bias)
- Display-off function : When / DSPOF is L, all LCD drive outputs (O1 to O160) remain at the V<sub>5</sub> level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.
- EI / LP input : EI / LP input enables LSI operation.  
Connect EIO1 / 2 from the 1st LSI to L.

Unit: mm

T6C03	LEAD PITCH	
	IN	OUT
(UA)	0.8	0.14

Please contact with Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

000707EBE1

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● Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

● Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.

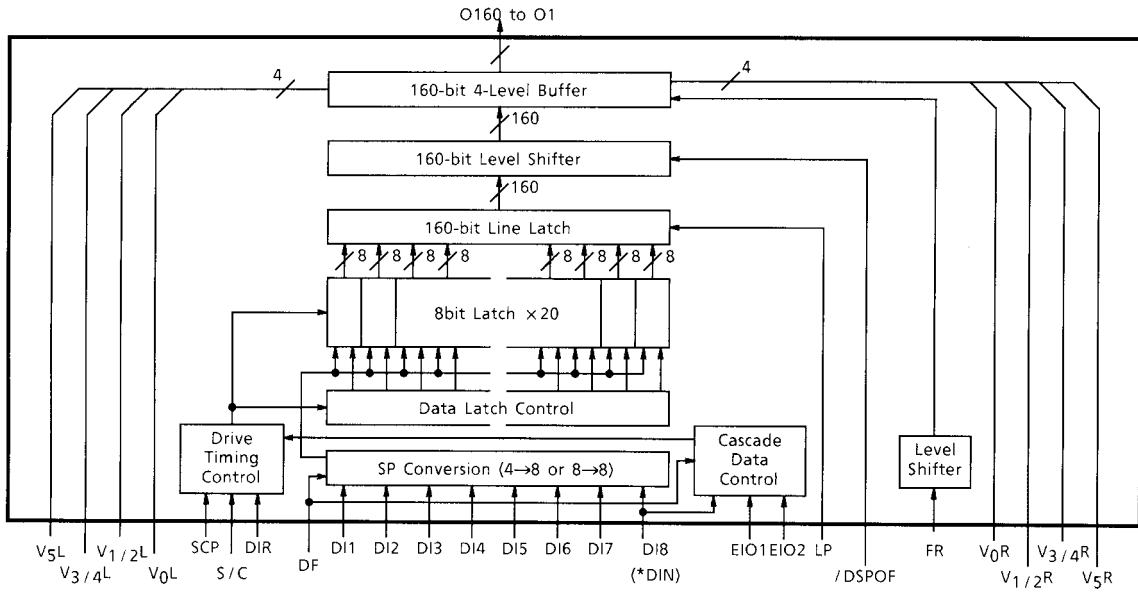
This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.

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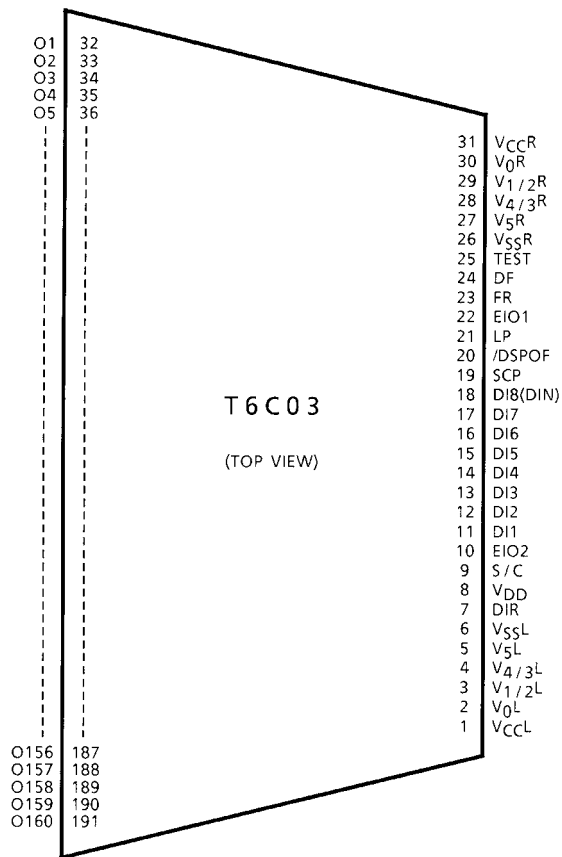
● The information contained herein is subject to change without notice.

Block Diagram



\* ROW MODE

**Pin Assignment**



Note: The above diagram shows the pin configuration of the LSI Chip, not that of the tape carrier package.



Pin Name	I / O	Functions	Level
V <sub>DD</sub>	—	Power supply for internal logic (+5.0 V)	—
V <sub>SS</sub>	—	Power supply for internal logic (0 V)	
V <sub>5L</sub> · R	—	Power supply for LCD drive circuit	
V <sub>3 / 4L</sub> · R	—	Power supply for LCD drive circuit	
V <sub>2 / 1L</sub> · R	—	Power supply for LCD drive circuit	
V <sub>0L</sub> · R	—	Power supply for LCD drive circuit	
V <sub>CC</sub> L · R, V <sub>SS</sub> L · R	—	Power supply for LCD drive circuit	

### Relation Between FR, Data Input and Output Level

F R	Data Input	/ Dspof	Output Level (Column Mode)	Output Level (Row Mode)
L	L	H	V <sub>3</sub>	V <sub>4</sub>
L	H	H	V <sub>5</sub>	V <sub>0</sub>
H	L	H	V <sub>2</sub>	V <sub>1</sub>
H	H	H	V <sub>0</sub>	V <sub>5</sub>
(Note)	(Note)	L	V <sub>5</sub>	V <sub>5</sub>

Note: Don't Care

## Data Input Format

### Column Mode

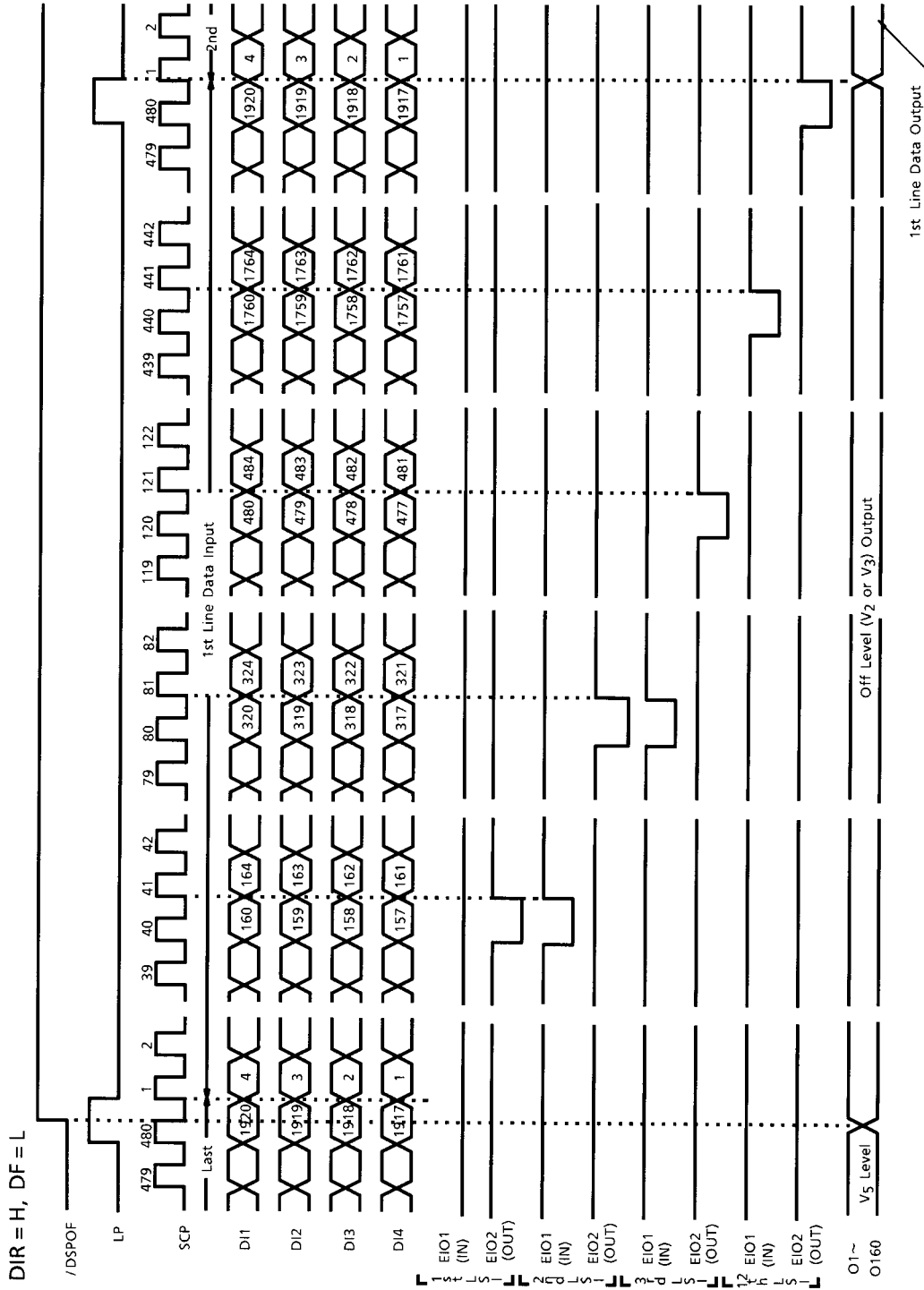
DIR	DF	BIT Mode	Enable Pin		(Note 1)	Input Data Line and Output Buffers							
			EIO1	EIO2		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	L	4-BIT	IN	OUT	L	O160	O159	O158	O157	—	—	—	—
					F	O4	O3	O2	O1	—	—	—	—
L			OUT	IN	L	O1	O2	O3	O4	—	—	—	—
					F	O157	O158	O159	O160	—	—	—	—
H	H	8-BIT	IN	OUT	L	O160	O159	O158	O157	O156	O155	O154	O153
					F	O8	O7	O6	O5	O4	O3	O2	O1
L			OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
					F	O153	O154	O155	O156	O157	O158	O159	O160

Note 1: L: Last Data  
F: First Data

### Row Mode

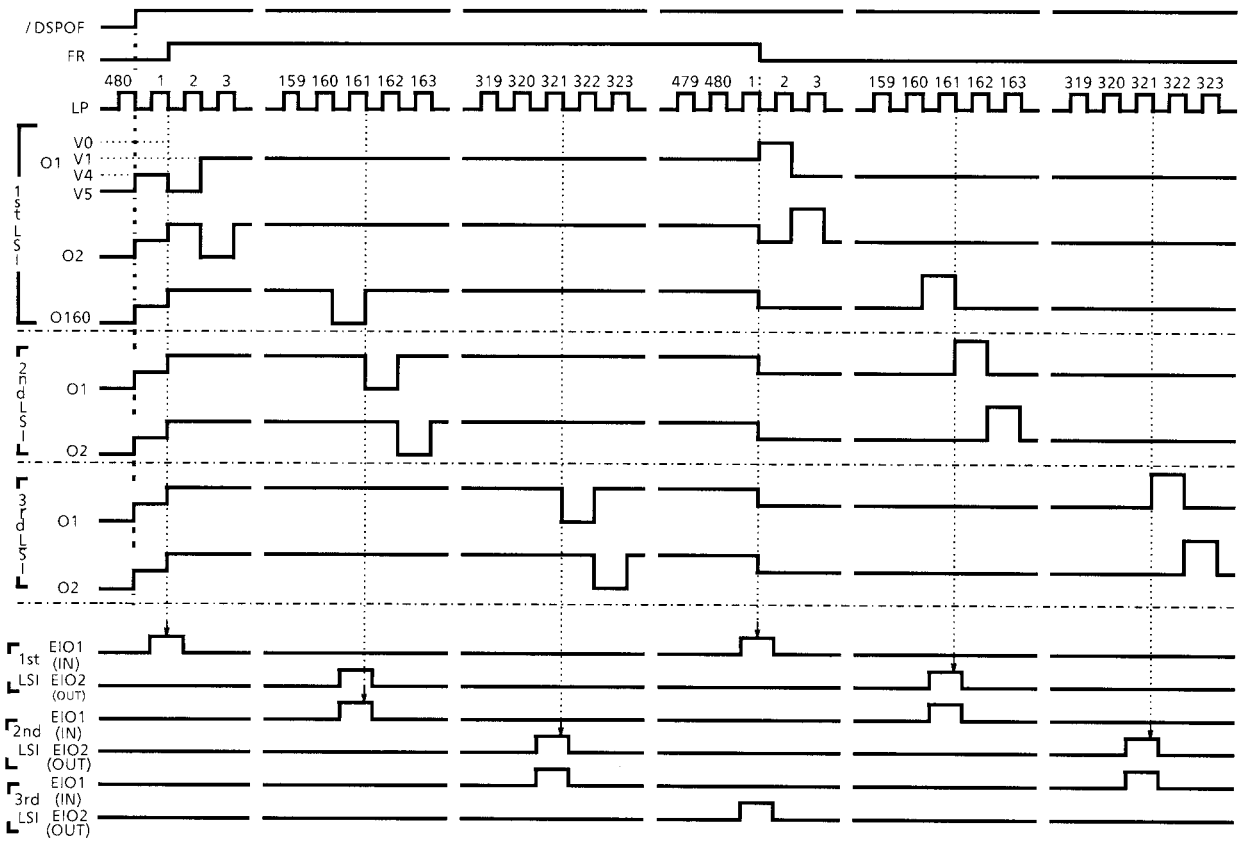
DIR	DF	Data Flow	Data Input Terminals		
			EIO1	EIO2	DIN
L	L	O160 → O1	OUT	IN	—
H		O1 → O160	IN	OUT	—
L	H	O160 → O81 O80 → O1	OUT	IN	IN
H		O1 → O80 O81 → O160	IN	OUT	IN

Timing Diagram (Column mode)



Timing Diagram (Row mode)

DIR = H, DUAL = L





## Absolute Maximum Ratings

(Ensure that the following conditions are maintained,  $V_{CC} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{SS}$ )

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage (1)	$V_{DD}$	$V_{DD}$	-0.3 to 7.0	V
Supply Voltage (2)	$V_{CC}$	$V_{CC}/R$	-0.3 to 45.0	V
Supply Voltage (3)	$V_0, V_2$	$V_{0L}/R, V_{2L}/R$	-0.3 to $V_{CC} + 0.3$	V
Supply Voltage (4)	$V_3, V_5$	$V_{3L}/R, V_{5L}/R$	-0.3 to 7.0	V
Input Voltage	$V_{IN}$	(Note 2)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	-20 to 75	°C
Storage Temperature	$T_{stg}$	—	-40 to 125	°C

Note 2: SCP, FR, LP, DIR, DF, S / C, EIO1, EIO2, DI1 to 8, / DSPOF, TEST

## Electrical Characteristics

### DC Characteristics

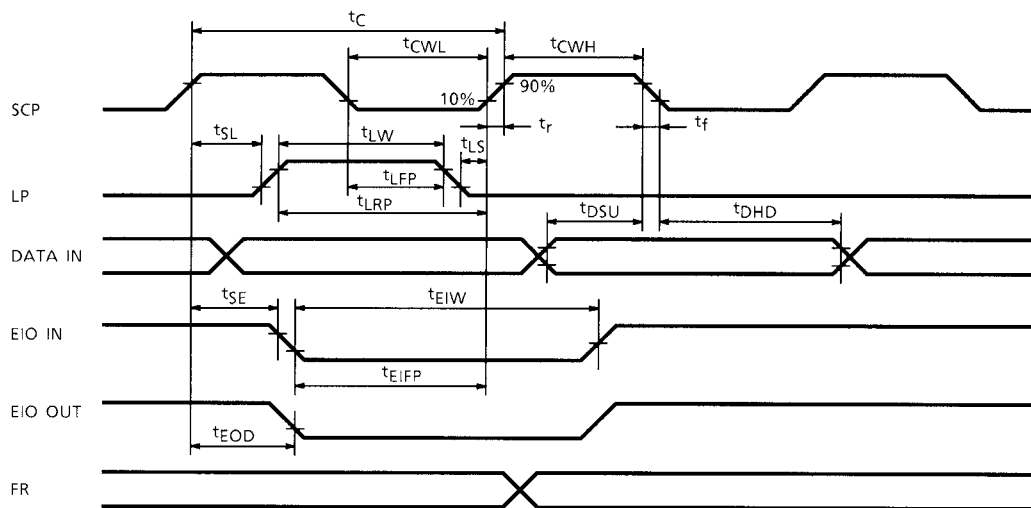
(Unless otherwise noted,  $V_{SS} = 0$  V,  $V_{DD} = 2.7$  to  $5.5$  V,  $T_a = -20$  to  $75^\circ\text{C}$ )

Item	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name	
Supply Voltage 1	$V_{DD}$	—	—	2.7	5.0	5.5	V	$V_{DD}$	
Supply Voltage 2	$V_{CC}$	—	—	14	—	42		$V_{CC}/R$	
Input Voltage	H Level	$V_{IH}$	(Note 2)	0.8 $V_{DD}$	—	$V_{DD}$	V	SCP, FR, LP, DIR, DF, S / C, EIO1, EIO2, DI1 to 8, / DSPOF, TEST	
	L Level	$V_{IL}$		0	—	0.2 $V_{DD}$			
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{DD} - 0.5$	—	$V_{DD}$			EIO1, EIO2
	L Level	$V_{OL}$	$I_{OL} = 0.5$ mA	0	—	0.5			
Output Resistance	H Level	$R_{OH}$	$V_{OUT} = V_0 - 0.5$ V (Note 3)	—	0.6	1.3	kΩ	O1 to O160	
	M Level	$R_{OM}$	$V_{OUT} = V_2 \pm 0.5$ V (Note 3)	—	0.6	1.3			
			$V_{OUT} = V_3 \pm 0.5$ V (Note 3)	—	0.6	1.3			
	L Level	$R_{OL}$	$V_{OUT} = V_5 + 0.5$ V (Note 3)	—	0.6	1.3			
Current Consumption (Note 4)	$I_{DD}$	—	$V_{DD} = 5.5$ V $V_{CC} = 42$ V $f_{LP} = 33$ kHz $f_{FR} = 8.3$ kHz $f_{scp} = 8.0$ MHz Input Data: every bit inverted $V_{IH} = 5.5$ V, $V_{IL} = 0$ V	—	—	4.0	mA	$V_{DD}$	

Note 3:  $V_{CC} = 20$  V, 1 / 13 bias

Note 4: Current consumption while the internal data receiver is operating

## AC Electrical Characteristics (Column mode)



### Test Conditions (1) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 5\text{ V} \pm 10\%$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	—	125	—	ns
SCP Pulse Width	$t_{CWL}$ , $t_{CWH}$	—	50	—	ns
Data Set-Up Time	$t_{DSU}$	—	50	—	ns
Data Hold Time	$t_{DHD}$	—	50	—	ns
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	(Note 5)	ns
LP Rise Time	$t_{LRP}$	—	50	—	ns
LP Fall Time	$t_{LFP}$	—	50	—	ns
LP Pulse Width	$t_{LW}$	—	45	—	ns
SCP-to-LP Delay Time	$t_{SL}$	—	40	—	ns
LP-to-SCP Delay Time	$t_{LS}$	—	40	—	ns
EIO IN Fall Time	$t_{EIFP}$	—	40	—	ns
EIO IN Pulse Width	$t_{EIW}$	—	40	—	ns
SCP-to-EIO Delay Time	$t_{SE}$	—	20	—	ns
EIO-OUT Delay Time	$t_{EOD}$	(Note 6)	—	80	ns

Note 5:  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50\text{ ns}$

Note 6:  $C_L = 30\text{ pF}$

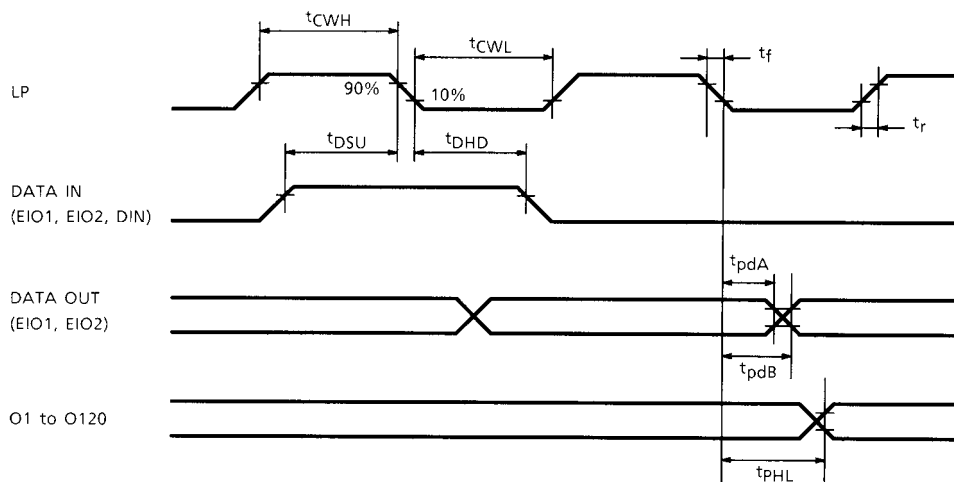
## Test Conditions (2) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 2.7\text{ to }4.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	—	500	—	ns
SCP Pulse Width	$t_{CWH}$ , $t_{CWL}$	—	240	—	ns
Data Set-Up Time	$t_{DSU}$	—	240	—	ns
Data Hold Time	$t_{DHD}$	—	240	—	ns
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	(Note 7)	ns
LP Rise Time	$t_{LRP}$	—	220	—	ns
LP Fall Time	$t_{LFP}$	—	240	—	ns
LP Pulse Width	$t_{LW}$	—	240	—	ns
SCP-to-LP Delay Time	$t_{SL}$	—	70	—	ns
LP-to-SCP Delay Time	$t_{LS}$	—	100	—	ns
EIO IN Fall Time	$t_{EIFP}$	—	240	—	ns
EIO IN Pulse Width	$t_{EIW}$	—	240	—	ns
SCP-to-EIO Delay Time	$t_{SE}$	—	50	—	ns
EIO-OUT Delay Time	$t_{EOD}$	(Note 8)	—	260	ns

Note 7:  $t_r$ ,  $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r$ ,  $t_f \leq 50\text{ ns}$

Note 8:  $C_L = 30\text{ pF}$

## AC Electrical Characteristics (Row mode)



### Test Conditions (1) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5\text{ to }5.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H	$t_{CWH}$	LP	30	—	ns
LP Pulse Width L	$t_{CWL}$	LP	195	—	ns
SCP Rise / Fall Time	$t_r, t_f$	LP, FR, EIO1, EIO2, DIN	—	20	ns
Data Set-up Time	$t_{DSU}$	EIO1, EIO2, DIN	80	—	ns
Data Hold Time	$t_{DHD}$	EIO1, EIO2, DIN	0	—	ns
EIO-OUT Delay Time A (Note 9)	$t_{pdA}$	EIO1, EIO2, DIN	5	—	ns
EIO-OUT Delay Time A (Note 9)	$t_{pdB}$	EIO1, EIO2, DIN	—	150	ns
LCD Drive Data Delat Time (Note 10)	$t_{pHL}$	O1 to O120	—	800	ns

### Test Conditions (2) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 2.7\text{ to }5.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H	$t_{CWH}$	LP	100	—	ns
LP Pulse Width L	$t_{CWL}$	LP	400	—	ns
SCP Rise / Fall Time	$t_r, t_f$	LP, FR, EIO1, EIO2, DIN	—	20	ns
Data Set-up Time	$t_{DSU}$	EIO1, EIO2, DIN	100	—	ns
Data Hold Time	$t_{DHD}$	EIO1, EIO2, DIN	0	—	ns
EIO-OUT Delay Time A (Note 9)	$t_{pdA}$	EIO1, EIO2, DIN	5	—	ns
EIO-OUT Delay Time A (Note 9)	$t_{pdB}$	EIO1, EIO2, DIN	—	400	ns
LCD Drive Data Delat Time (Note 10)	$t_{pHL}$	O1 to O120	—	1000	ns

Note 9:  $C_L = 30\text{ pF}$

Note 10:  $C_L = 20\text{ pF}$

Note: Insert the bypass capacitor ( $0.1\text{ }\mu\text{F}$ ) between  $V_{DD}$  and  $V_{SS}$ , to decrease power supply noise. Place the bypass capacitor as close to the LSI as possible.