

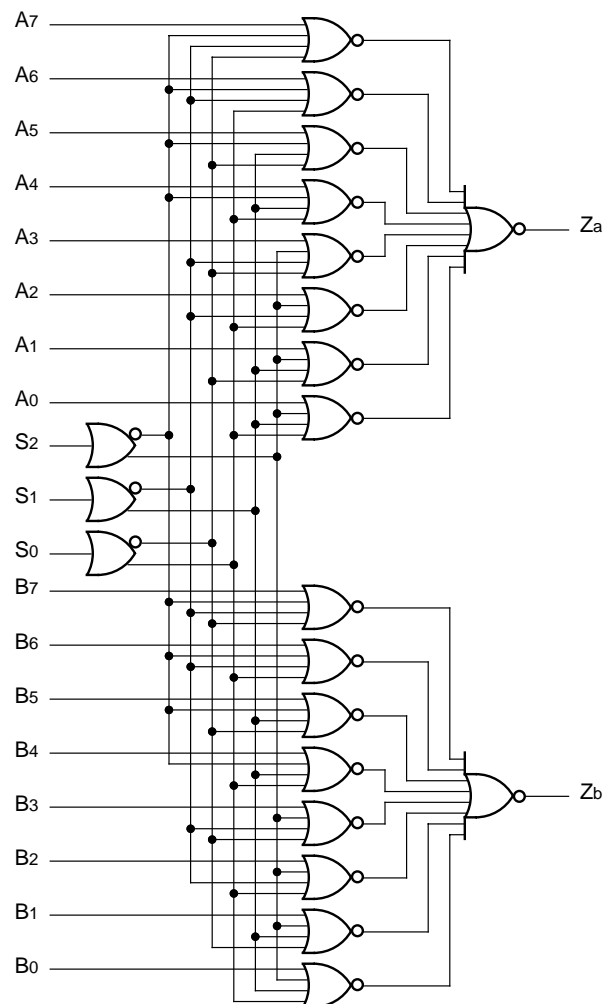
FEATURES

- Max. propagation delay of 900ps
- IEE min. of -92mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 60% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S363 is a dual 8-input multiplexer designed for use in new, high-performance ECL systems. The three Data Select inputs (S₀, S₁, S₂) determine the bits from each of the inputs (A_n, B_n) that will be passed on through the two outputs. The same bit will be selected from the two groups of 8 inputs. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



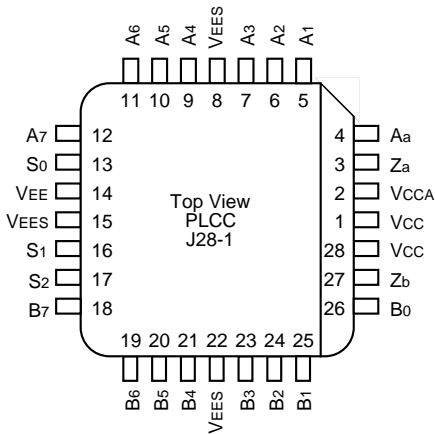
PACKAGE/ORDERING INFORMATION

Ordering Information

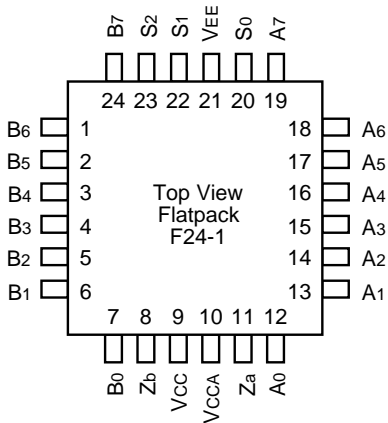
Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S363FC	F24-1	Commercial	SY100S363FC	Sn-Pb
SY100S363FCTR ⁽¹⁾	F24-1	Commercial	SY100S363FC	Sn-Pb
SY100S363JC	J28-1	Commercial	SY100S363JC	Sn-Pb
SY100S363JCTR ⁽¹⁾	J28-1	Commercial	SY100S363JC	Sn-Pb
SY100S363JZ ⁽²⁾	J28-1	Commercial	SY100S363JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S363JZTR ^(1, 2)	J28-1	Commercial	SY100S363JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

PIN NAMES

Pin	Function
S ₀ – S ₂	Data Select Inputs
A ₀ – A ₇	A Data Inputs
B ₀ – B ₇	B Data Inputs
Z _a , Z _b	Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Select			Inputs								Outputs
S ₂	S ₁	S ₀	Data								Z _a /Z _b
			A ₇ /B ₇	A ₆ /B ₆	A ₅ /B ₅	A ₄ /B ₄	A ₃ /B ₃	A ₂ /B ₂	A ₁ /B ₁	A ₀ /B ₀	
L	L	L								L	L
L	L	L								H	H
L	L	H							L		L
L	L	H							H		H
L	H	L						L			L
L	H	L						H			H
L	H	H					L				L
L	H	H					H				H
H	L	L				L					L
H	L	L				H					H
H	L	H			L						L
H	L	H			H						H
H	H	L		L							L
H	H	L		H							H
H	H	H	L								L
H	H	H	H								H

Note:

- H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current	—	—	200	μA	V _{IN} = V _{IH} (Max.)
	S _n A _n , B _n	—	—	200		
I _{EE}	Power Supply Current	-92	-66	-45	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS**CERPACK**

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

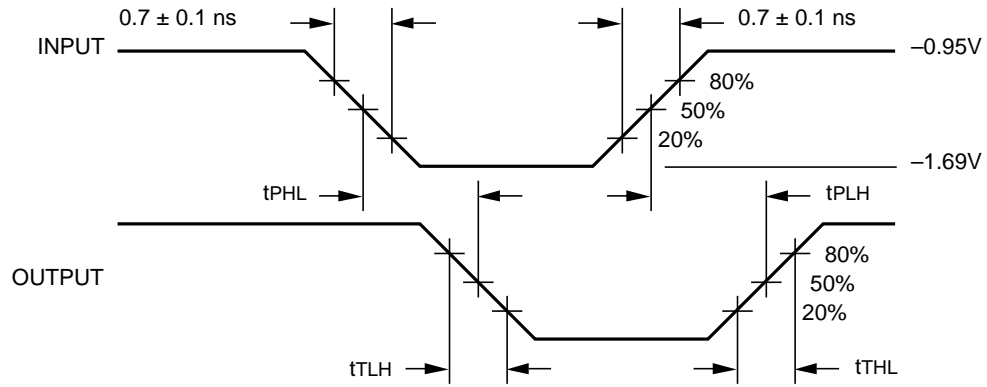
Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay A ₀ – A ₇ , B ₀ – B ₇ to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ – S ₂ to Output	400	1400	400	1400	400	1400	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	1000	300	1000	300	1000	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay A ₀ – A ₇ , B ₀ – B ₇ to Output	300	900	300	900	300	900	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ – S ₂ to Output	400	1300	400	1300	400	1300	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

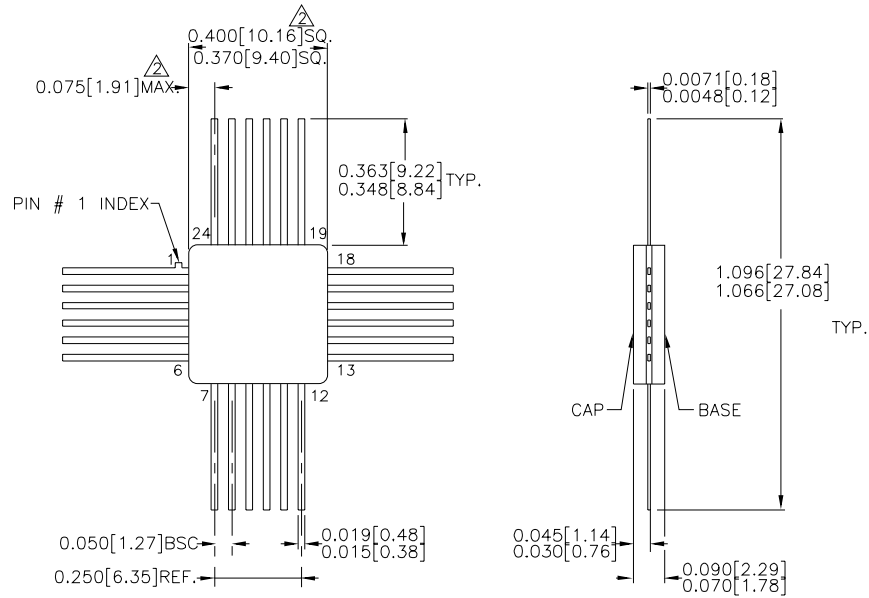


Propagation Delay and Transition Times

Note:

$V_{EE} = -4.2\text{V}$ to -5.5V unless otherwise specified; $V_{CC} = V_{CCA} = \text{GND}$

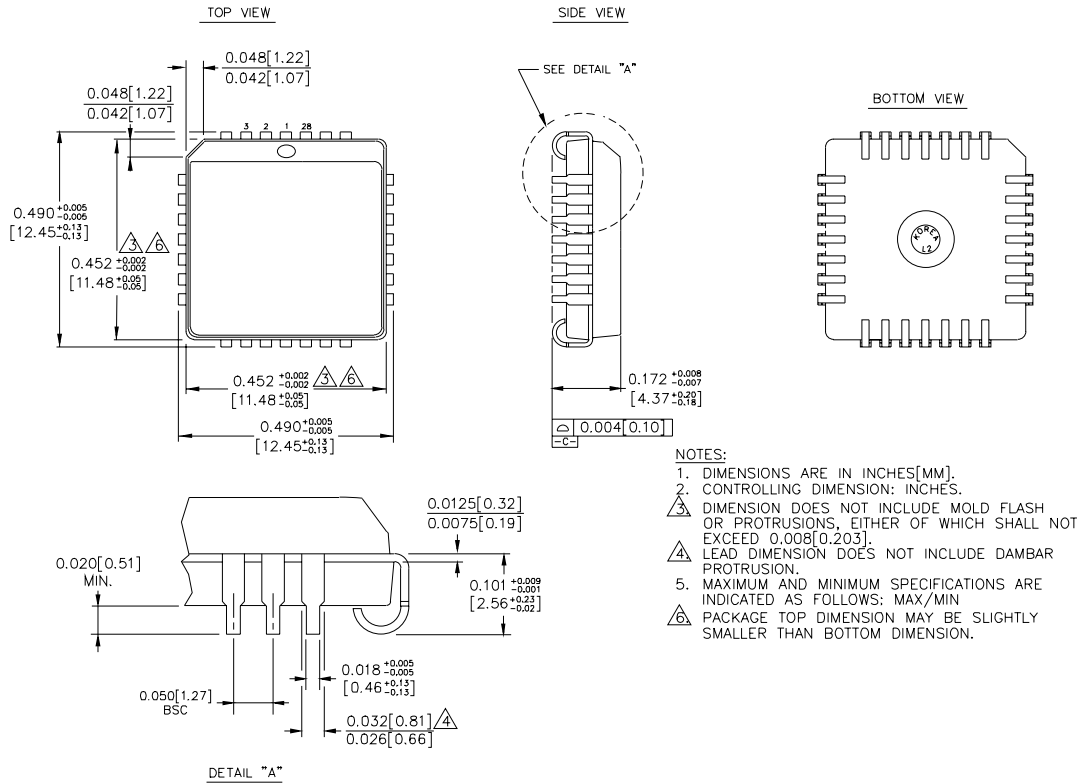
24-PIN CERPACK (F24-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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