



# DUAL SUPPLY OCTAL ECL-TO-TTL

Precision Edge®  
SY100HA643

## FEATURES

- ECL/TTL version of popular ECLinPS™ E111
- 400ps within device skew
- 800ps part-to-part skew
- Latch
- Differential internal design
- V<sub>BB</sub> output
- Dual supply
- Reset/Enable
- Multiple TTL and ECL power/ground pins
- Fully compatible with MC100H643
- Higher performance than H643 versions
- Industrial temperature availability
- Available in 28-pin PLCC package



Precision Edge®

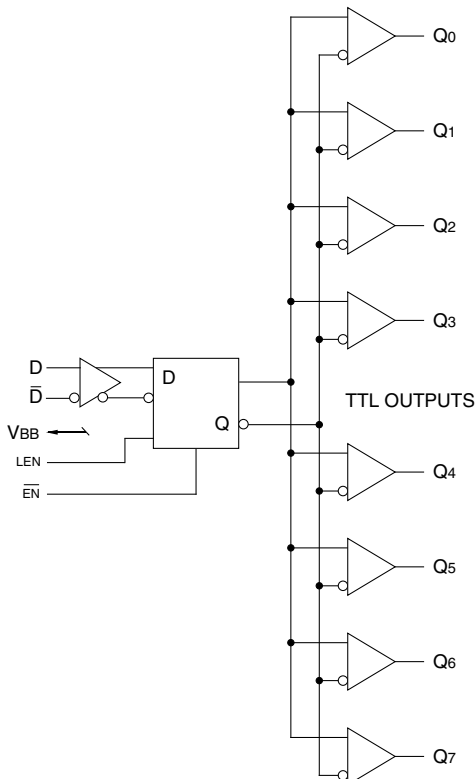
## DESCRIPTION

The SY100HA643 is an enhanced dual supply, low skew translating 1:8 clock driver. Devices in the Micrel H600 translators series utilize the 28-lead PLCC for optimal power pinning, signal flow through and electrical performance. The dual-supply HA643 is similar to the H641, which is a single-supply 1:9 version of the same function, with higher performance than the H643 versions.

The device features a 48mA TTL output stage, with AC performance specified into a 20pF load capacitance. A Latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin ( $\overline{EN}$ ) forces all outputs LOW.

The 100HA643 is compatible with 100K ECL logic levels.

## BLOCK DIAGRAM

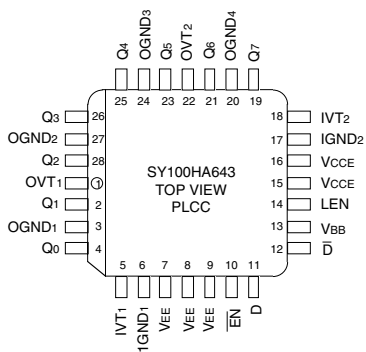


## PIN NAMES

Pin	Function
OGND	TTL Output Ground (0V)
OVTTL	Output V <sub>cc</sub> (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V <sub>cc</sub> (+5.0V)
V <sub>EE</sub>	ECL V <sub>EE</sub> (-5.2/-4.5V)
V <sub>CCE</sub>	ECL Ground (0V)
D, $\overline{D}$	Signal Input (ECL)
V <sub>BB</sub>	V <sub>BB</sub> Reference Output
Q <sub>0</sub> - Q <sub>7</sub>	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

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**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100HA643JC	J28-1	Commercial	SY100HA643JC	Sn-Pb
SY100HA643JCTR <sup>(2)</sup>	J28-1	Commercial	SY100HA643JC	Sn-Pb
SY100HA643JI	J28-1	Industrial	SY100HA643JI	Sn-Pb
SY100HA643JITR <sup>(2)</sup>	J28-1	Industrial	SY100HA643JI	Sn-Pb
SY100HA643JY <sup>(3)</sup>	J28-1	Industrial	SY100HA643JY with Pb-Free bar-line indicator	Matte-Sn
SY100HA643JYTR <sup>(2, 3)</sup>	J28-1	Industrial	SY100HA643JY with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**TRUTH TABLE**

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L

**DC CHARACTERISTICS**

IVT = OVT = 5.0V ±5%; VEE = -4.2V to -5.5V; VCC = GND

Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>EE</sub>	Power Supply	—	58	—	58	—	58	—	58	mA	VEE Pins Total all OVT and IVT pins
I <sub>CCCL</sub>		—	83	—	83	—	83	—	83	mA	
I <sub>CCCH</sub>		—	73	—	73	—	73	—	73	mA	
V <sub>OH</sub>	TTL Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I <sub>OH</sub> = -3.0mA I <sub>OH</sub> = -15mA
V <sub>OL</sub>	TTL Output LOW Voltage	—	0.5	—	0.5	—	0.5	—	0.5	V	I <sub>OL</sub> = 48mA
I <sub>OS</sub>	TTL Output Short Circuit Current	-80	-200	-80	-200	-80	-200	-80	-200	mA	V <sub>OUT</sub> = 0V
I <sub>IH</sub>	ECL Input HIGH Current	—	225	—	225	—	175	—	175	μA	
I <sub>IL</sub>	ECL Input LOW Current	0.5	—	0.5	—	0.5	—	0.5	—	μA	
V <sub>IH</sub>	ECL Input HIGH Voltage	—	—	-1165	-880	-1165	-880	-1165	-880	mV	
V <sub>IL</sub>	ECL Input LOW Voltage	—	—	-1810	-1475	-1810	-1475	-1810	-1475	mV	
V <sub>BB</sub>	ECL Output Reference Voltage	-1380	-1260	-1380	-1260	-1380	-1260	-1380	-1260	mV	

**AC CHARACTERISTICS**

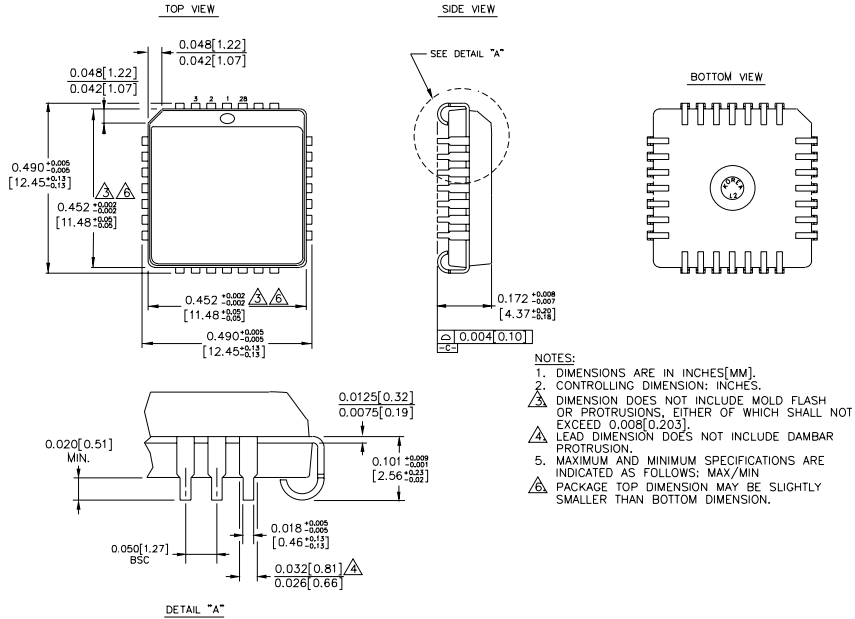
IVT = OVT = 5.0V ±5%; VEE = -4.2V to -5.5V ; VCCE = GND

Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>IH</sub>	Propagation Delay to Output D LEN EN	2.3	3.1	2.3	3.1	2.3	3.1	2.3	3.1	ns	CL = 20pF
t <sub>skew</sub>	Within-Device Skew <sup>(1)</sup>	—	0.4	—	0.4	—	0.4	—	0.4	ns	
t <sub>PW</sub>	Pulse Width Out <sup>(2)</sup> HIGH or LOW @ FOUT = 100MHz	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	ns	CL = 20pF
t <sub>S</sub>	Setup Time D	0.75	—	0.75	—	0.75	—	0.75	—	ns	
t <sub>H</sub>	Hold Time D	0.75	—	0.75	—	0.75	—	0.75	—	ns	
t <sub>RR</sub>	Recovery Time LEN EN	1.25 1.25	— —	1.25 1.25	— —	1.25 1.25	— —	1.25 1.25	— —	ns ns	
t <sub>PW</sub>	Minimum Pulse Width LEN EN	1.5 1.5	— —	1.5 1.5	— —	1.5 1.5	— —	1.5 1.5	— —	ns ns	
t <sub>r</sub> t <sub>f</sub>	Rise / Fall times 0.8V — 2.0V	—	1.5	—	1.5	—	1.5	—	1.5	ns	CL = 20pF
f <sub>MAX</sub>	Max. Input Frequency <sup>(3,4)</sup>	160	—	160	—	160	—	160	—	MHz	CL = 20pF

**Notes:**

1. Within-Device skew defined as identical transitions on similar paths through a device.
2. Pulse width is defined relative to 1.5V measurement points on the output waveform.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f<sub>MAX</sub> value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

**28-PIN PLCC (J28-1)**



Rev. 03

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