

STW47NM50

N-CHANNEL 500V - 0.065Ω - 45A TO-247

MDmesh[™]Power MOSFET

ADVANCED DATA

TYPE	V_{DSS}	R _{DS(on)}	R _{ds(on)} *Q _g	ID
STW47NM50	500V	< 0.085Ω	5.6 Ω*nC	45 A

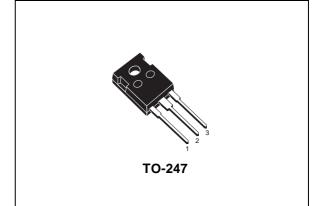
- TYPICAL $R_{DS}(on) = 0.065\Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

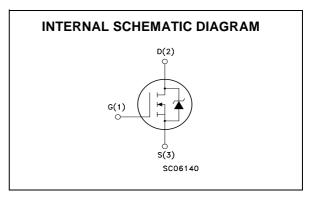
DESCRIPTION

The MDmesh[™] is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH[™] horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh[™] family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.





Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R_{GS} = 20 k Ω)	500	V
V_{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	45	А
I _D	Drain Current (continuous) at T _C = 100°C	28.4	А
I _{DM} (•)	Drain Current (pulsed)	180	А
PTOT	Total Dissipation at $T_C = 25^{\circ}C$	417	W
	Derating Factor	2.08	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
Tj	Max. Operating Junction Temperature	150	°C

ABSOLUTE MAXIMUM RATINGS

 $({\ensuremath{\bullet}}) \ensuremath{\mathsf{Pulse}}$ width limited by safe operating area

(1) $I_{SD} \leq 45A$, di/dt $\leq 400A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

January 2003

STW47NM50

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.3	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
ΤI	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	20	A
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25 \text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 35 \text{ V}$)	810	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	500			V
I _{DSS}	Zero Gate Voltage	V _{DS} = Max Rating			10	μA
	Drain Current (V _{GS} = 0)	V_{DS} = Max Rating, T_{C} = 125 °C			100	μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 30 V$			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 22.5 A		0.065	0.085	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	$\label{eq:VDS} \begin{split} V_{DS} &> I_{D(on)} \; x \; R_{DS(on)max,} \\ I_{D} &= 22.5 A \end{split}$		20		S
Ciss	Input Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		3700		pF
Coss	Output Capacitance			610		pF
C _{rss}	Reverse Transfer Capacitance			50		pF
C _{oss eq.} (2)	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to 400V		325		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.7		Ω

Image: Pulse duration = 300 μs, duty cycle 1.5 %.
Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

ELECTRICAL CHARACTERISTICS (CONTINUED)

•	5	V	V	I	I	C	Η	IN	IG	U	IN	

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	V _{DD} = 250V, I _D = 22.5 A		40		ns
tr	Rise Time	$R_G = 4.7\Omega V_{GS} = 10 V$ (see test circuit, Figure 3)		35		ns
Qg	Total Gate Charge	V _{DD} = 400 V, I _D = 45 A,		87	117	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		23		nC
Q _{gd}	Gate-Drain Charge			42		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{r(Voff)}	Off-voltage Rise Time	$V_{DD} = 400 \text{ V}, \text{ I}_{D} = 45 \text{ A},$		18		ns
t _f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10 V$ (see test circuit, Figure 5)		23		ns
t _c	Cross-over Time			44		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current				45	А
I _{SDM} (2)	Source-drain Current (pulsed)				180	А
V _{SD} (1)	Forward On Voltage	I _{SD} = 45 A, V _{GS} = 0			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$\begin{split} I_{SD} &= 40 \text{ A, } \text{di/dt} = 100 \text{A/} \mu \text{s,} \\ V_{DD} &= 100 \text{ V, } \text{T}_{\text{j}} = 25^{\circ}\text{C} \\ (\text{see test circuit, Figure 5}) \end{split}$		520 7.8 30		ns μC Α
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$\begin{split} I_{SD} &= 40 \text{ A, } \text{di/dt} = 100 \text{A/}\mu\text{s,} \\ V_{DD} &= 100 \text{ V, } \text{T}_{\text{j}} = 150^{\circ}\text{C} \\ (\text{see test circuit, Figure 5}) \end{split}$		680 11.2 33		ns µC A

Note:1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.2. Pulse width limited by safe operating area.

STW47NM50

Fig. 1: Unclamped Inductive Load Test Circuit

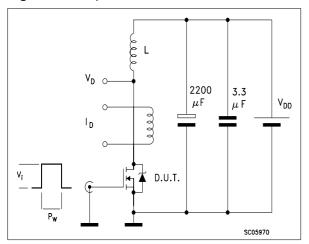


Fig. 3: Switching Times Test Circuit For Resistive Load

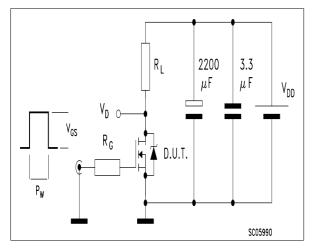


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

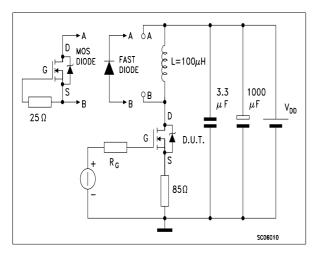


Fig. 2: Unclamped Inductive Waveform

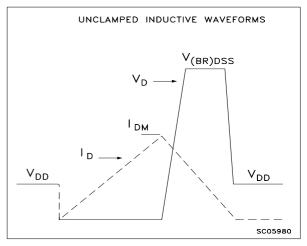
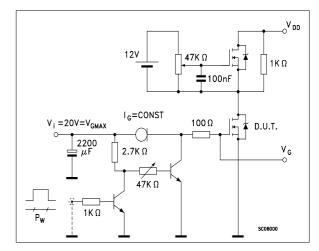
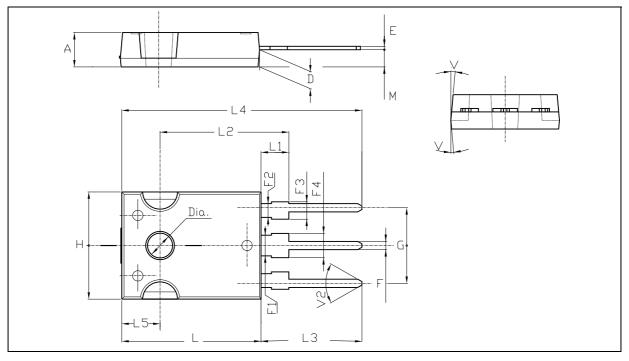


Fig. 4: Gate Charge test Circuit



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
Е	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
Н	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
М	2		3	0.07		0.11
V		5°			5°	
V2	,	60°			60°	
Dia	3.55		3.65	0.14		0.143



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics. © The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved STMicroelectronics GROUP OF COMPANIES Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© http://www.st.com