



# STV8162 - STV8162D

## +5 V, +5 V and +8 V Triple-Voltage Regulator with Disable and Reset Functions

DATASHEET

### Key Features

- Input Voltage range between 7 V and 18 V
- Output Currents up to 600 mA
- Fixed Precision Output 1 voltage of 5 V  $\pm$  2%
- Fixed Precision Output 2 voltage of 5 V  $\pm$  2%
- Fixed Precision Output 3 voltage of 8 V  $\pm$  2%
- Output 1 with Reset facility
- Outputs 2 and 3 can be disabled by digital input
- Short Circuit Protection on each output
- Thermal Protection
- Low Dropout Voltages

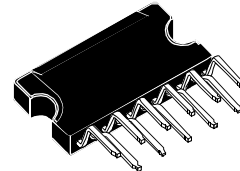
### DESCRIPTION

The STV8162 and STV8162D are monolithic triple positive voltage regulators designed to provide three fixed precision output voltages of 5 V, 5 V and 8 V for currents up to 0.6 A.

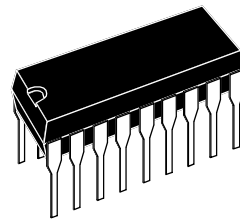
An internal reset circuit generates a reset pulse when the voltage of Output 1 drops below the regulated voltage value.

Outputs 2 and 3 can be disabled by a digital input.

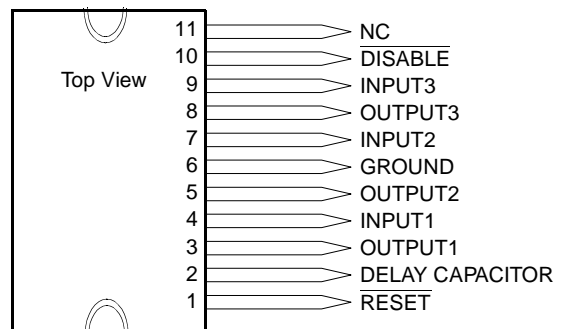
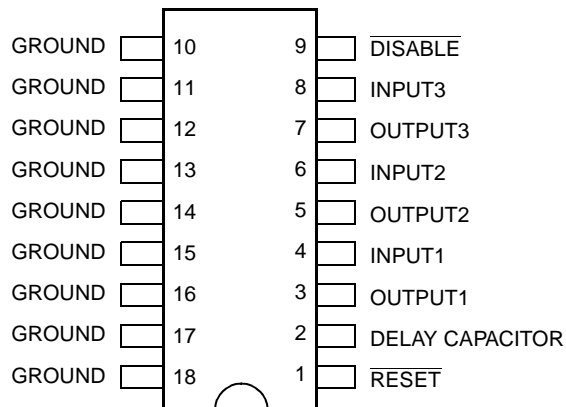
Short-circuit and thermal protections are included in all versions.



**Clipwatt 11**  
Order Code: STV8162



**Power DIP 18 (9 + 9)**  
Order Code: STV8162D



# 1 GENERAL INFORMATION

Figure 1: STV8162 Block Diagram

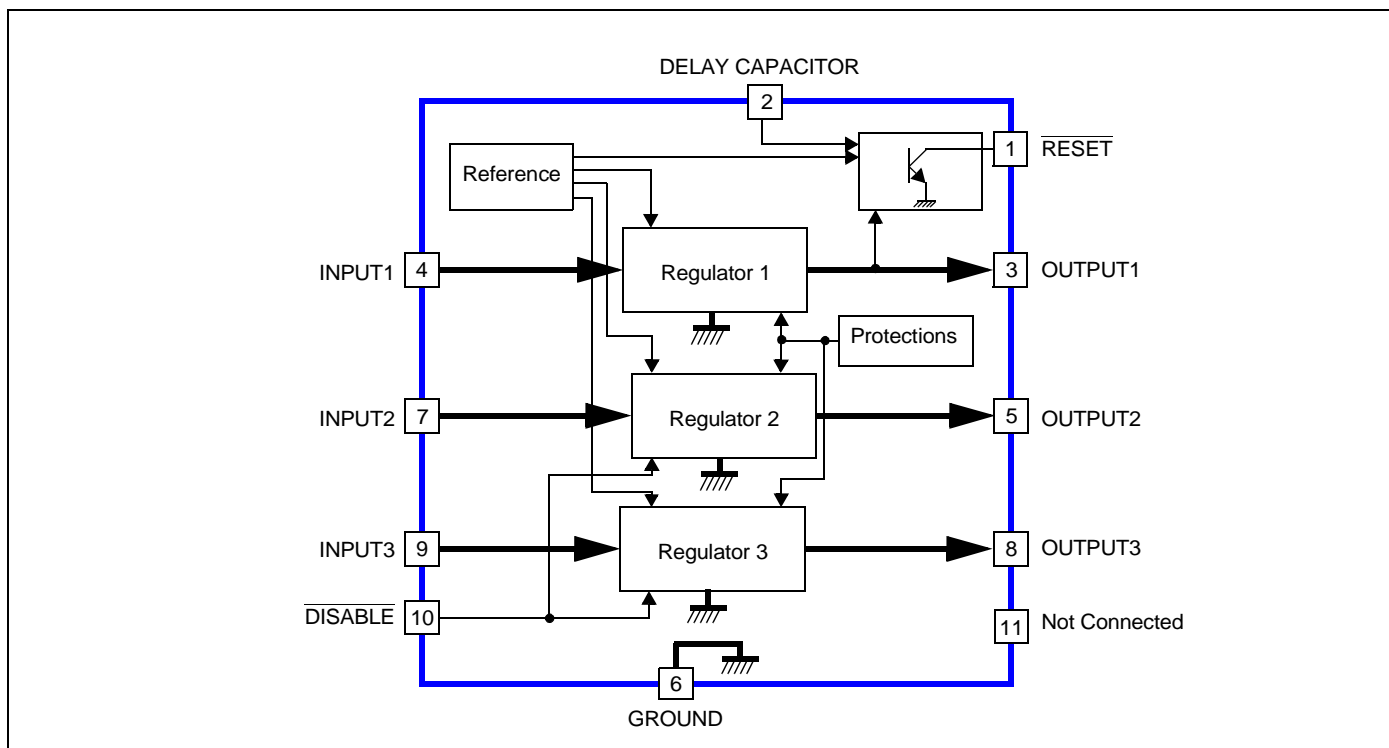
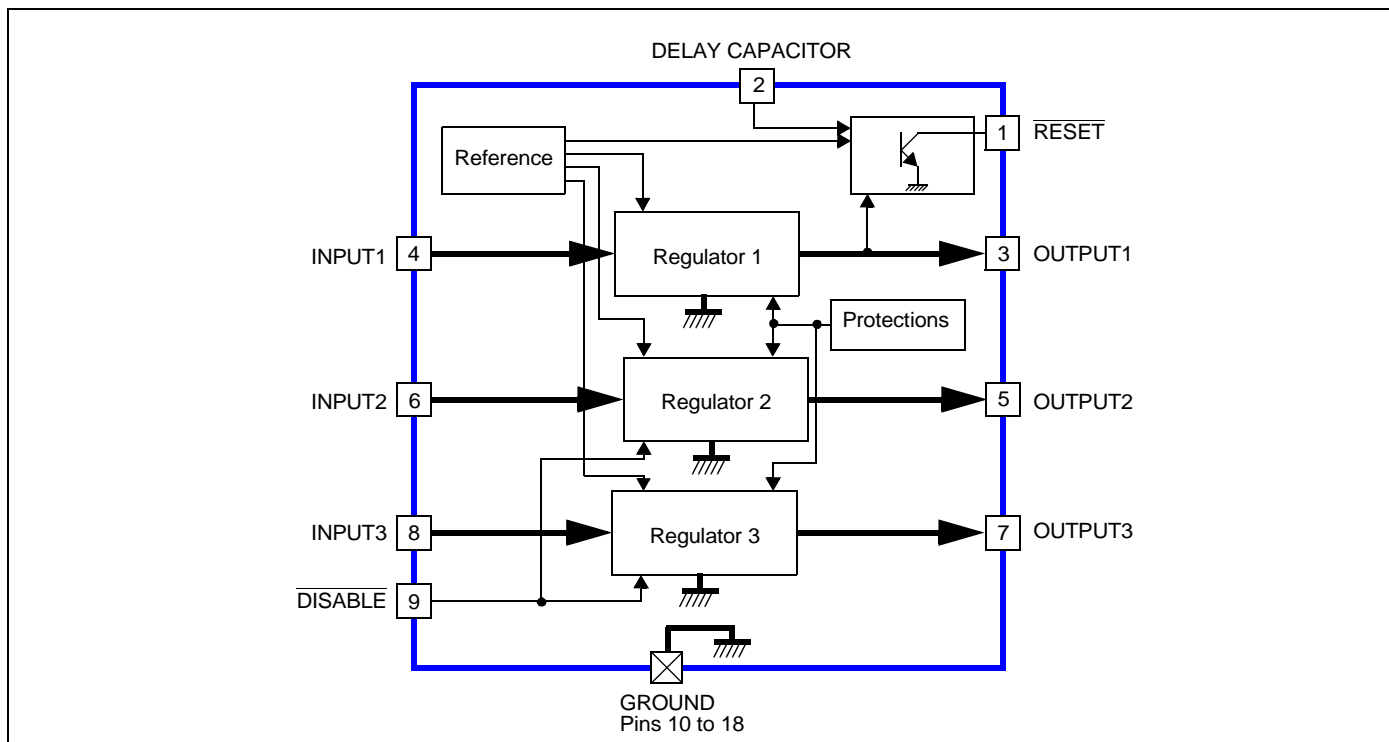


Figure 2: STV8162D Block Diagram



## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_{IN}$	DC Input Voltage at pins INPUT1, INPUT2 and INPUT3	20	V
$V_{DIS}$	Disable Input Voltage at pin $\overline{DISABLE}$	20	V
$V_{RST}$	Output Voltage at pin $\overline{RESET}$	20	V
$I_{OUTPUT}$	Output Currents	Internally Limited	
$P_t$	Power Dissipation	Internally Limited	
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_J$	Junction Temperature	0 to +150	°C

### 2.2 Thermal Data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction-to-Case Thermal Resistance	STV8162 3 STV8162D 15	°C/W
$R_{thJA}$	Junction-to-Ambient Thermal Resistance <sup>1</sup>	STV8162 ≥10 STV8162D 56	°C/W
$T_J$	Maximum Recommended Junction Temperature	140	°C
$T_{OPER}$	Operating Free Air Temperature Range	0 to +70	°C

1. Mounted on board. For more information, refer to [Section 5](#).

### 2.3 Electrical Characteristics

$T_{AMB} = 25^\circ\text{C}$ ,  $V_{IN1} = 7\text{V}$ ,  $V_{IN2} = 7\text{V}$  and  $V_{IN3} = 10\text{V}$ , unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{OUT1}$	Output Voltage	$I_{OUT1} = 10\text{mA}$	4.90	5.00	5.10	V
$V_{OUT2}$	Output Voltage	$I_{OUT2} = 10\text{mA}$	4.90	5.00	5.10	V
$V_{OUT3}$	Output Voltage	$I_{OUT3} = 10\text{mA}$	7.84	8.00	8.16	V
$V_{OUT1}$	Output Voltage	$7\text{V} < V_{IN1} < 12\text{V}$ $5\text{mA} < I_{OUT1} < 600\text{mA}$	4.80		5.20	V
$V_{OUT2}$	Output Voltage	$7\text{V} < V_{IN2} < 12\text{V}$ $5\text{mA} < I_{OUT2} < 600\text{mA}$	4.80		5.20	V
$V_{OUT3}$	Output Voltage	$10\text{V} < V_{IN3} < 15\text{V}$ $5\text{mA} < I_{OUT3} < 600\text{mA}$	7.68		8.32	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IO1</sub>	Dropout Voltage	I <sub>OUT1</sub> = 0.6 A		1	1.4	V
V <sub>IO2</sub>	Dropout Voltage	I <sub>OUT2</sub> = 0.6 A		1	1.4	V
V <sub>IO3</sub>	Dropout Voltage	I <sub>OUT3</sub> = 0.6 A		1	1.4	V
V <sub>OUT1LI</sub>	Line Regulation	7 V < V <sub>IN1</sub> < 12 V, I <sub>OUT1</sub> = 200 mA			50	mV
V <sub>OUT2LI</sub>	Line Regulation	7 V < V <sub>IN2</sub> < 12 V, I <sub>OUT2</sub> = 200 mA			50	mV
V <sub>OUT3LI</sub>	Line Regulation	10 V < V <sub>IN3</sub> < 15 V, I <sub>OUT3</sub> = 200 mA			80	mV
V <sub>OUT1LO</sub>	Load Regulation	5 mA < I <sub>OUT1</sub> < 600 mA			100	mV
V <sub>OUT2LO</sub>	Load Regulation	5 mA < I <sub>OUT2</sub> < 600 mA			100	mV
V <sub>OUT3LO</sub>	Load Regulation	5 mA < I <sub>OUT3</sub> < 600 mA			160	mV
I <sub>Q</sub>	Quiescent Current	I <sub>OUT1</sub> = 10 mA Outputs 2 and 3 disabled		2.2	3.0	mA
V <sub>O1RST</sub>	Reset Threshold Voltage	K = V <sub>OUT1</sub>	K-0.4	K-0.25	K-0.10	V
V <sub>RTH</sub>	Reset Threshold Hysteresis	See circuit description.	30	75	120	mV
t <sub>RD</sub>	Reset Pulse Delay	C <sub>e</sub> = 100 nF See circuit description.		25		ms
V <sub>RL</sub>	Saturation Voltage in Reset Condition	I <sub>RESET</sub> = 5 mA			0.4	V
I <sub>RH</sub>	Leakage Current in Normal Condition, at RESET pin	V <sub>RESET</sub> = 10 V			10	μA
K <sub>OUT1</sub> K <sub>OUT2</sub> K <sub>OUT3</sub>	Output Voltage Thermal Drift	T <sub>J</sub> = 0 to 125°C $K_{OUT} = \frac{\Delta V_{OUT} \cdot 10^6}{\Delta T \cdot V_{OUT}}$		100		ppm/°C
I <sub>OUT1SC</sub>	Short Circuit Output Current	V <sub>IN1</sub> = 7 V	0.8	1.3	1.8	A
I <sub>OUT2SC</sub>	Short Circuit Output Current	V <sub>IN1</sub> = 7 V	0.8	1.3	1.8	A
I <sub>OUT3SC</sub>	Short Circuit Output Current	V <sub>IN3</sub> = 10 V	0.8	1.3	1.8	A
V <sub>DISH</sub>	Voltage High Level at $\overline{\text{DISABLE}}$ pin (Outputs 2 and 3 active)		2			V
V <sub>DISL</sub>	Voltage Low Level at $\overline{\text{DISABLE}}$ pin (Outputs 2 and 3 disabled)				0.8	V
I <sub>DIS</sub>	Bias Current at $\overline{\text{DISABLE}}$ pin	0 V < V <sub>DISABLE</sub> < 7 V	-100		2	μA
T <sub>JSD</sub>	Junction Temperature for Thermal Shutdown			150		°C
T <sub>SDH</sub>	Thermal Shutdown Temperature Hysteresis			15		°C

### 3 Circuit Description

The STV8162 and STV8162D are triple-voltage regulators with Reset and Disable functions.

The three regulation parts are supplied from a single voltage reference circuit trimmed by zener zapping during EWS testing. Since the supply voltage of this voltage reference is connected to pin INPUT1 ( $V_{IN1}$ ), the second and third regulators will not work if pin INPUT1 is not supplied.

The output stages are designed using a Darlington configuration with a typical dropout voltage of 1.0 V.

**IMPORTANT:** *In all applications, all three inputs must be polarized. If Outputs 2 or 3 are not used, the corresponding inputs must be connected to Input 1.*

The Disable circuit will switch off pins OUTPUT2 and OUTPUT3 if a voltage less than 0.8 V is applied to pin  $\overline{\text{DISABLE}}$ .

The Reset circuit checks the voltage at pin OUTPUT1. If this voltage drops below  $V_{OUT1}-0.25$  V (4.75 V Typ.), the "a" comparator (Figure 3) rapidly discharges the external capacitor ( $C_e$ ) and the reset output immediately switches to low. When the voltage at pin OUTPUT1 exceeds  $V_{OUT1}-0.175$  V (4.825 V Typ.), the  $V_{C_e}$  voltage increases linearly to the reference voltage ( $V_{REF} = 2.5$  V) corresponding to a Reset Pulse Delay ( $t_{RD}$ ) as shown in Figure 4.

$$t_{RD} = \frac{C_e \times 2.5V}{10\mu A}$$

Afterwards, the reset output returns to high. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9 V).

## 4 Application Diagrams

Figure 3: Reset Diagram

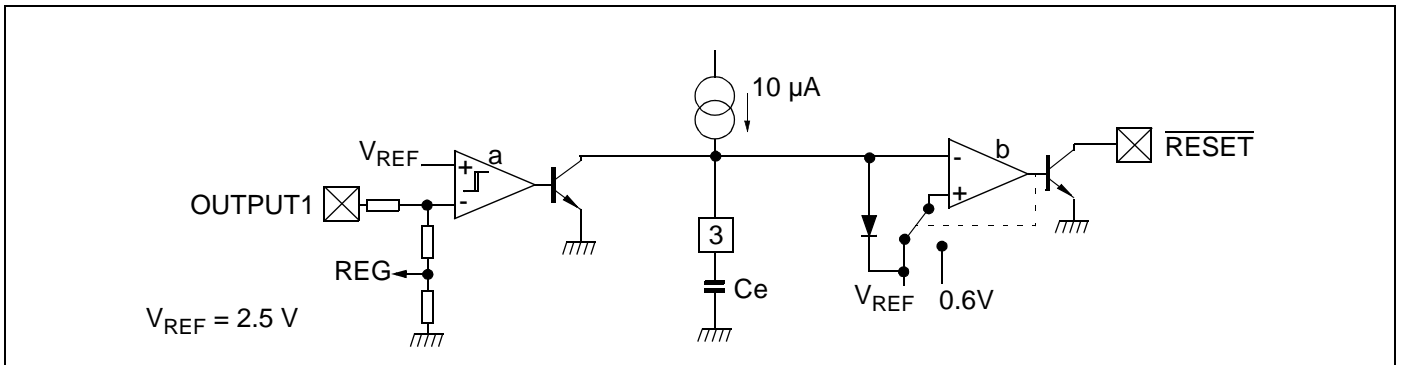


Figure 4: Internal Reset Voltage

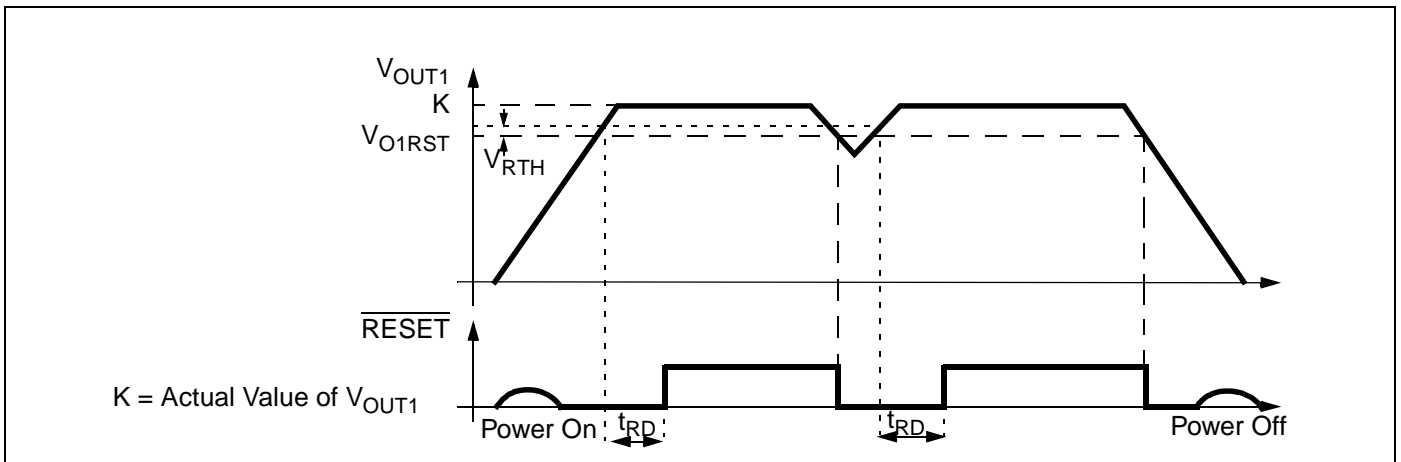


Figure 5: STV8162 Typical Application

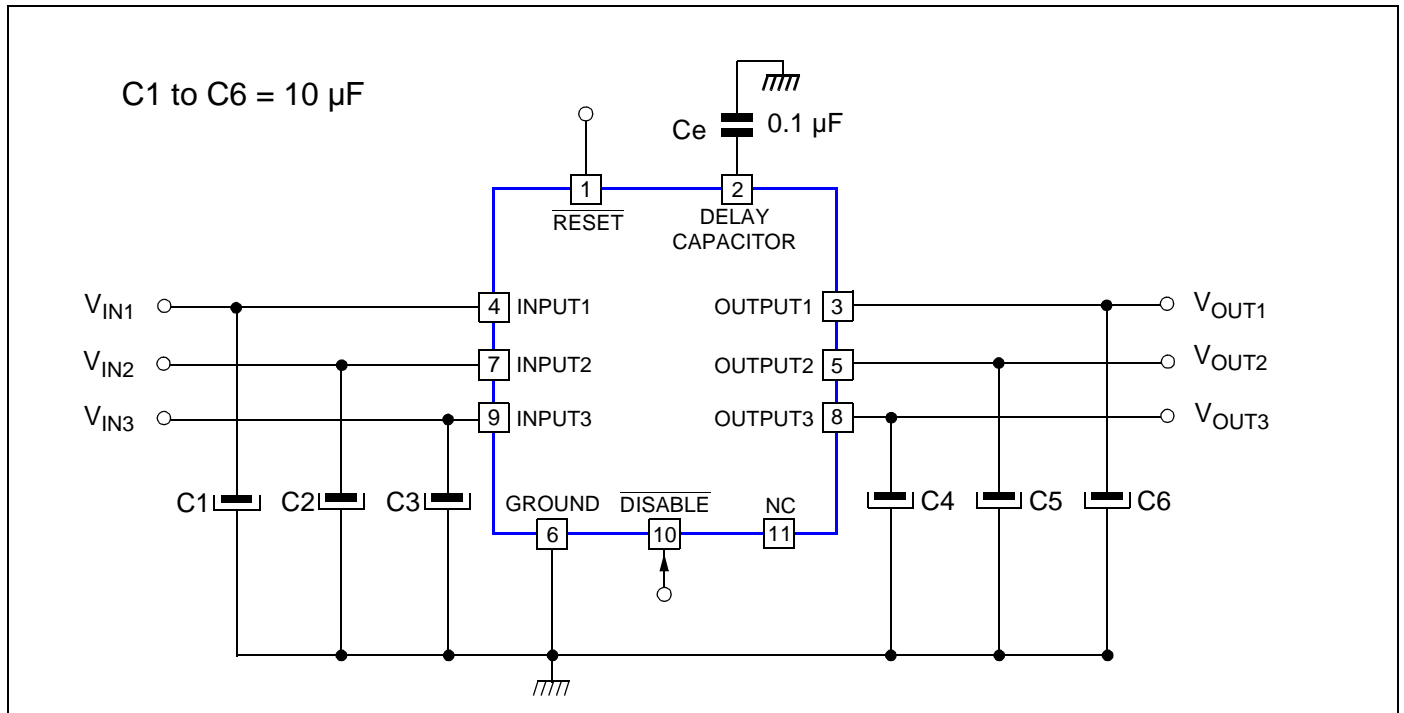
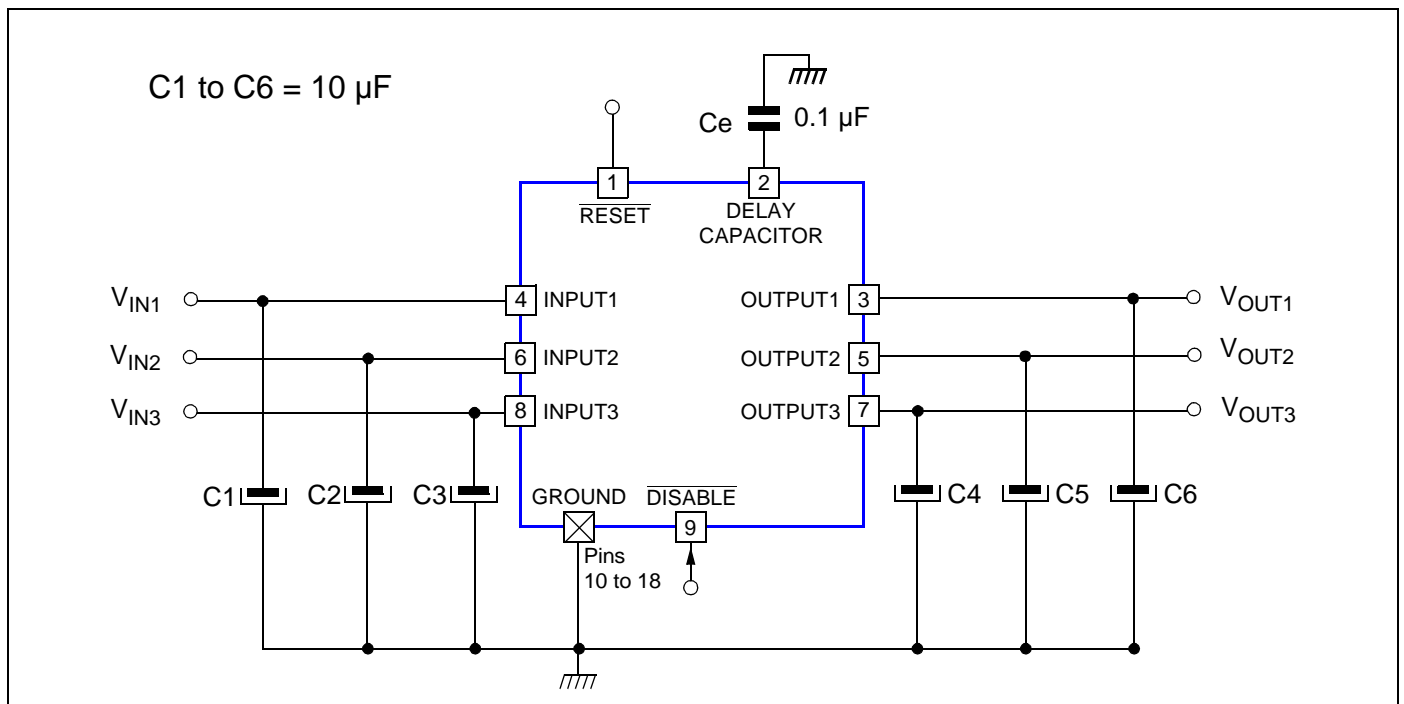


Figure 6: STV8162D Typical Application



## 5 Power Dissipation and Layout Indications

The power is mainly dissipated by the three device buffers. It can be calculated by the equation:

$$P = (V_{IN1} - V_{OUT1}) \times I_{OUT1} + (V_{IN2} - V_{OUT2}) \times I_{OUT2} + (V_{IN3} - V_{OUT3}) \times I_{OUT3}$$

The following table lists the different  $R_{thJA}$  values of these packages with or without a heat sink and the corresponding maximum power dissipation assuming:

- Maximum Ambient Temperature = 70° C
- Maximum Junction Temperature = 140° C

Device	Heat Sink	$R_{thJA}$ in °C/W	$P_{MAX}$ in W
STV8162	No	50	1.4
	Yes	15	4.6
STV8162D	No	56 to 40	1.25 to 1.75
	Yes	32	2.2

Figure 7: Thermal Resistance (Junction-to-Ambient) of DIP18 Package without Heat Sink

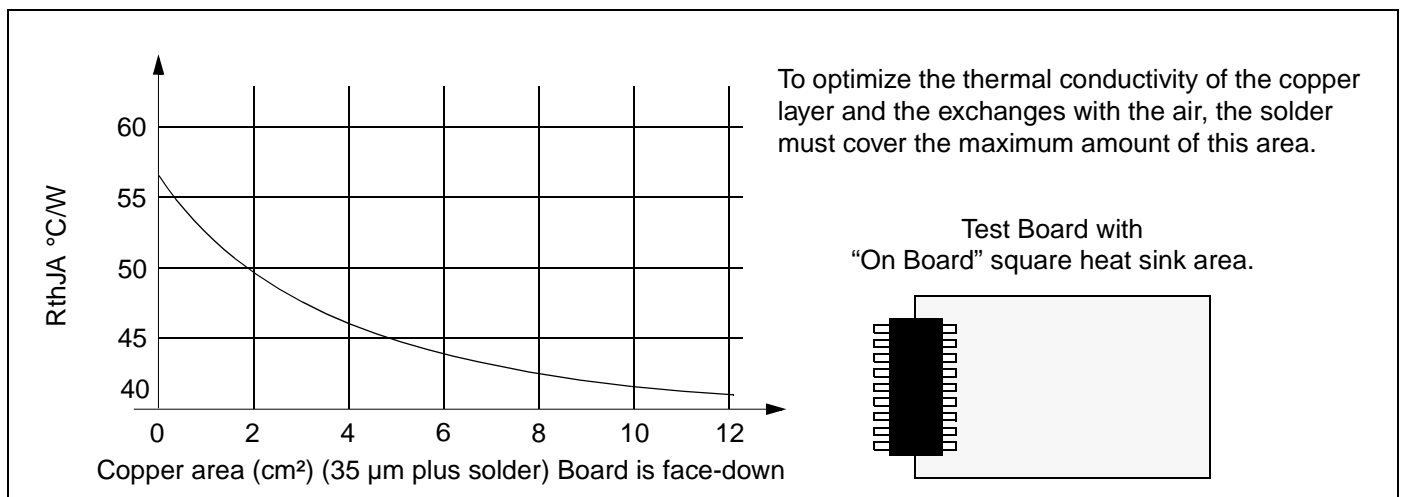
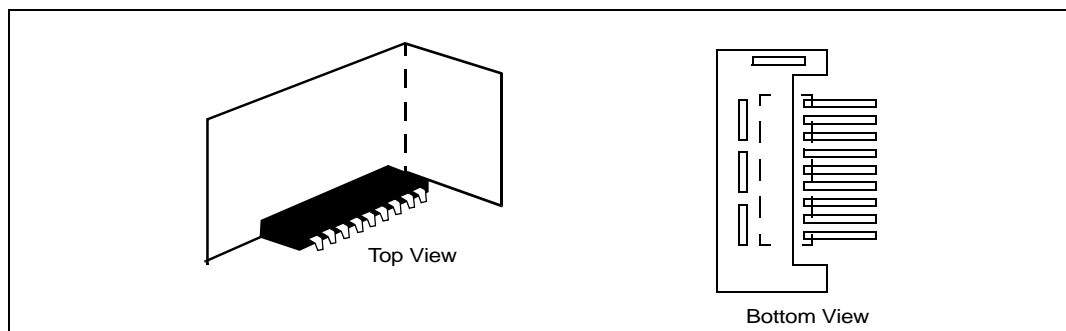


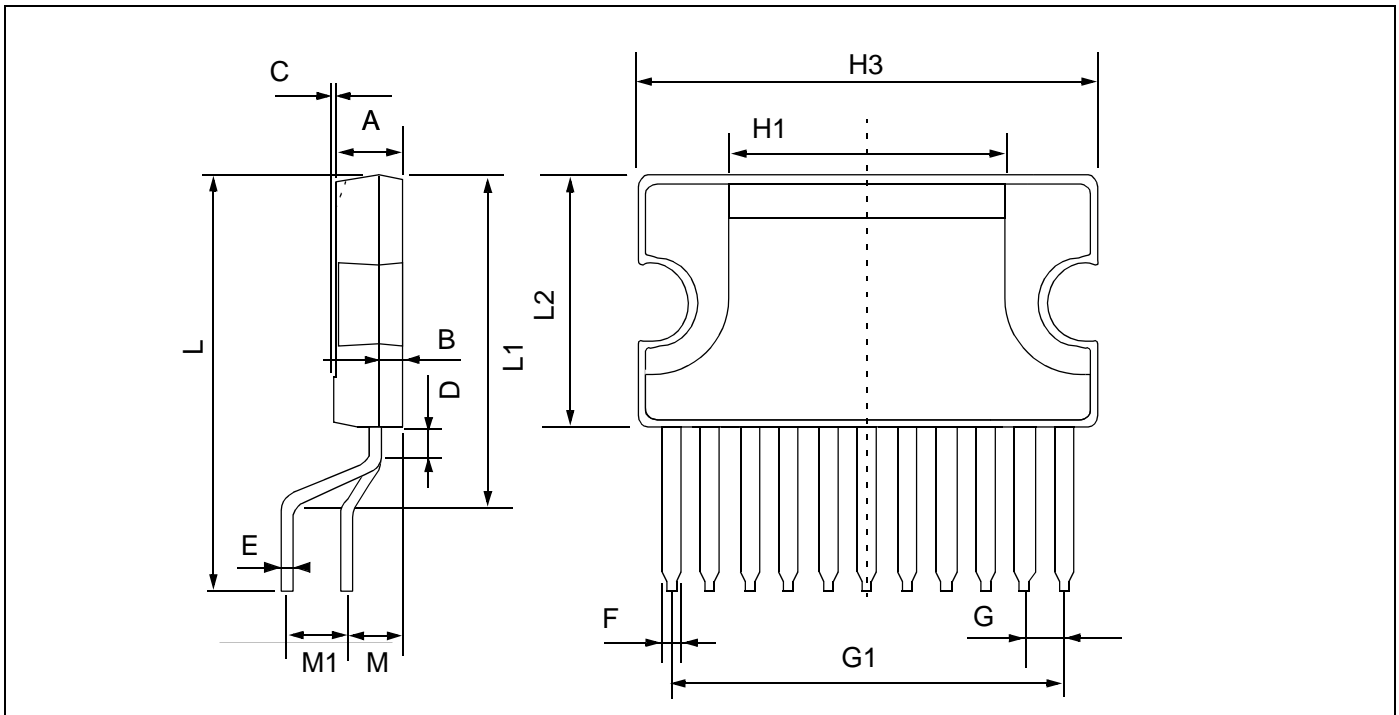
Figure 8: Metal plate mounted near the STV8162D for heat sinking





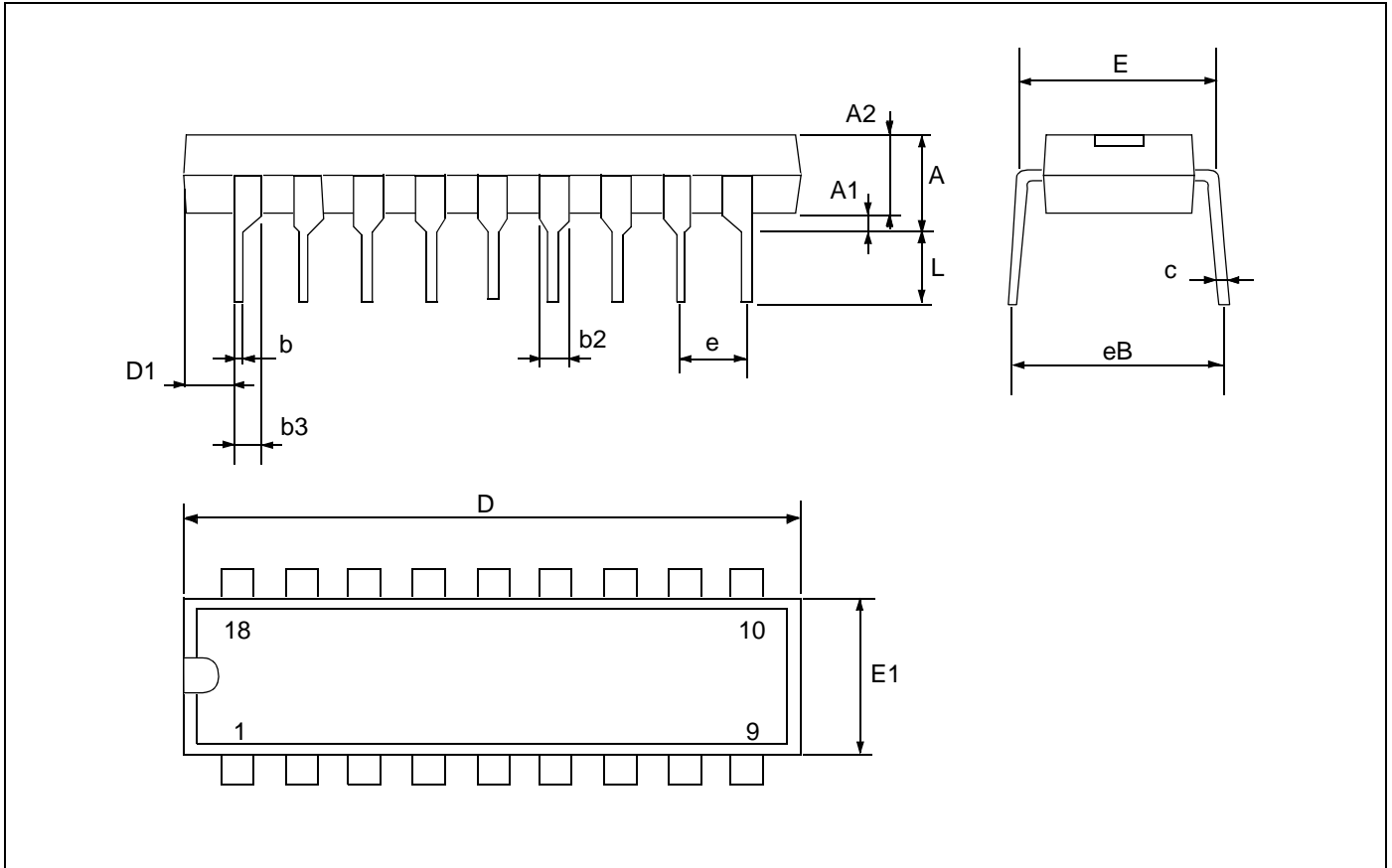
## 6 Package Mechanical Data

Figure 9: 11-pin Plastic Clipwatt Package



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.20			0.126
B			1.05			0.041
C		0.15			0.006	
D		1.50			0.059	
E	0.49	0.55		0.019	0.002	
F	0.80		0.91	0.031		0.036
G	1.57	1.70	1.83	0.062	0.067	0.072
H1		12.00			0.480	
H2		18.60			0.732	
H3	19.85			0.781		
L		17.90			0.700	
L1		14.45			0.569	
L2	10.70	11.00	11.20	0.421	0.433	0.441
L3		5.50			0.217	
M		2.54			0.100	
M1		2.54			0.100	
	<b>Number of Pins</b>					
N	11					

Figure 10: 18-pin Plastic Dual In-line Power Package



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
b3	0.76	0.99	1.14	0.030	0.039	0.045
c	0.20	0.25	0.36	0.008	0.010	0.014
D	22.35	22.86	23.37	0.880	0.900	0.920
D1	0.13			0.005		
e		2.54			0.100	
eB			10.92			0.430
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150

## 7 Revision History

Table 1: Summary of Modifications

Version	Date	Main Changes
0.2	January 2000	First Edition
0.3	November 2002	Addition of PDIP18 package.

**NOTES:**

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