



# STS17NH3LL

N-channel 30V - 0.004Ω - 17A - SO-8  
STripFET™ Power MOSFET for DC-DC conversion

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS17NH3LL	30V	<0.0057Ω	17A <sup>(1)</sup>

1. This value is rated according to R<sub>thj-pcb</sub>

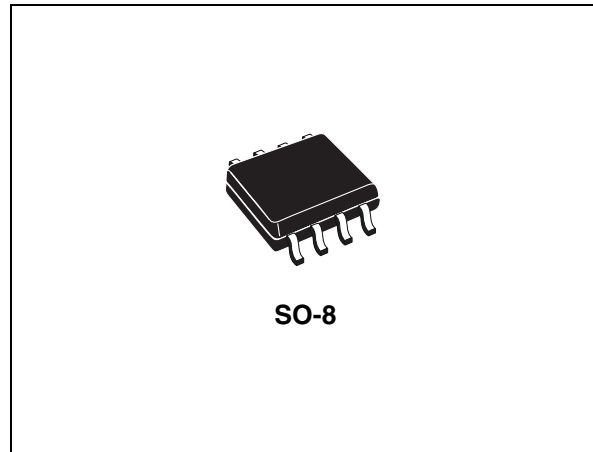
- Optimal R<sub>DS(on)</sub> x Q<sub>g</sub> trade-off @ 4.5 V
- Conduction losses reduced
- Improved junction-case thermal resistance
- Low threshold device

## Description

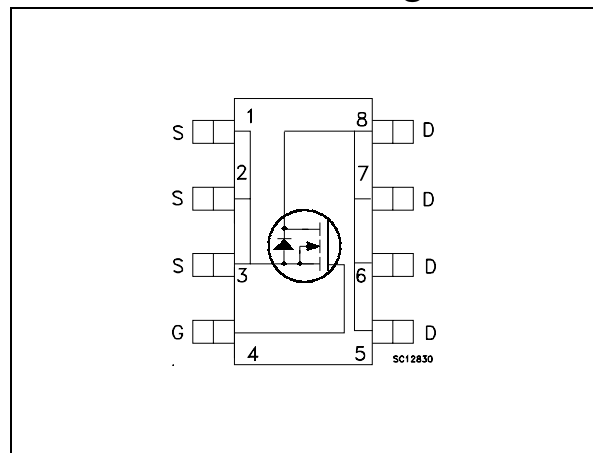
This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This process coupled to unique metallization techniques realizes the most advanced low voltage Power MOSFET in SO-8 ever produced.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STS17NH3LL	17H3LL-	SO-8	Tape & reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate- source voltage	$\pm 16$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	17	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	10.6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	68	A
$P_{tot}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	2.7	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature		

1. This value is rated according to  $R_{thj-pcb}$
2. Pulse width limited by safe operating area

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient max	47	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2oz of Cu and  $t < 10\text{sec}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 8.5A$ $V_{GS} = 4.5V, I_D = 8.5A$		0.004 0.005	0.0057 0.0075	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS}=25V, f=1MHz, V_{GS} = 0$		1810 565 41		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}=15V, I_D=17A$ $V_{GS}=4.5V$ <i>(see Figure 13)</i>		18 4.8 5.3	24	nC nC nC
$R_G$	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain	0.5	1.5	3	$\Omega$

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 15V$ , $I_D = 8.5A$ $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see Figure 15)		8 65		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 15V$ , $I_D = 8.5A$ $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see Figure 15)		38 20		ns ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				17	A
$I_{SDM}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 17A$ , $V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17A$ , $di/dt = 100A/\mu s$		22		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 15V$ , $T_j = 25^\circ C$		32		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14)		1.9		A

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

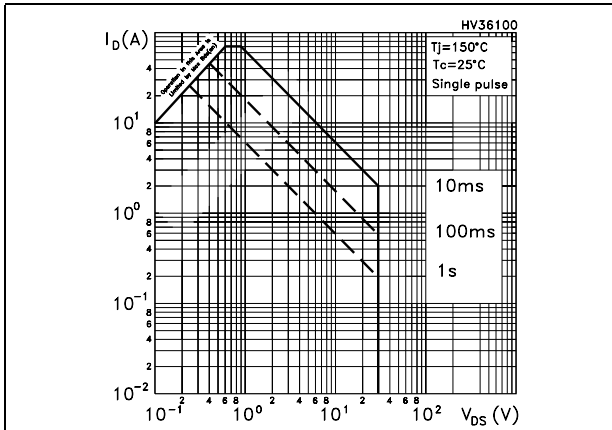


Figure 2. Thermal impedance

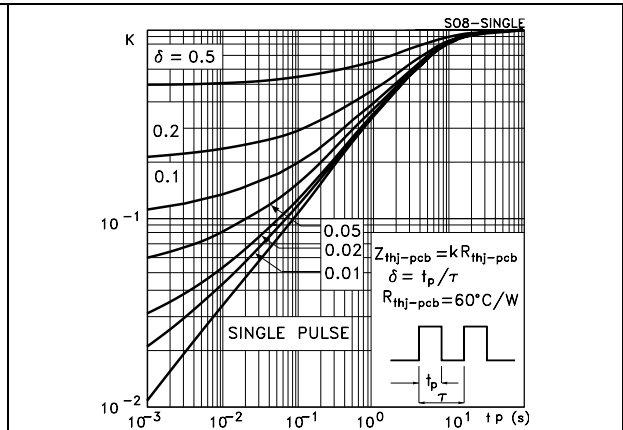


Figure 3. Output characteristics

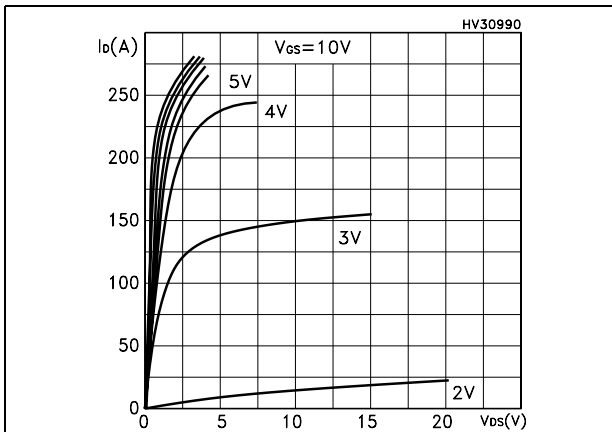


Figure 4. Transfer characteristics

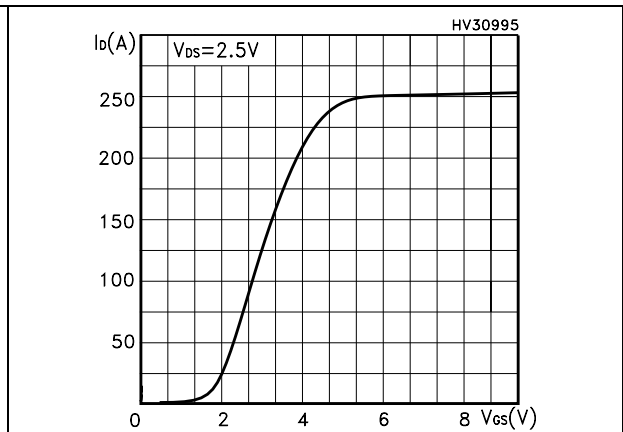


Figure 5. Normalized  $B_{V_{DS}}$  vs temperature

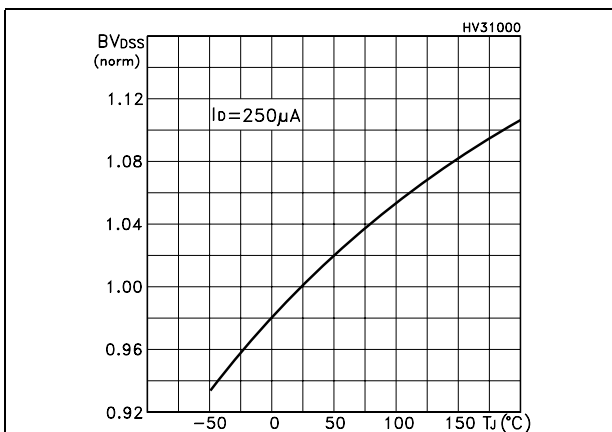


Figure 6. Static drain-source on resistance

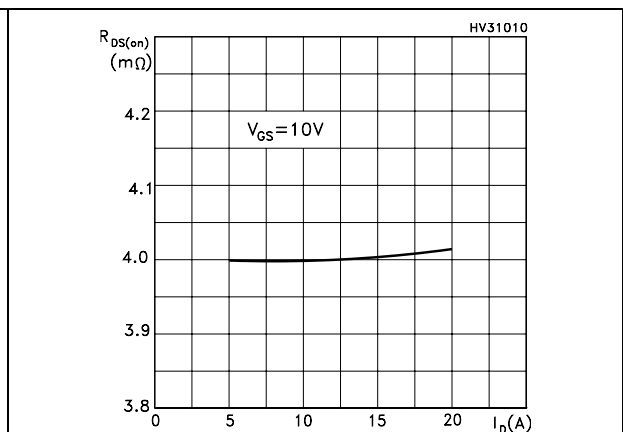


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

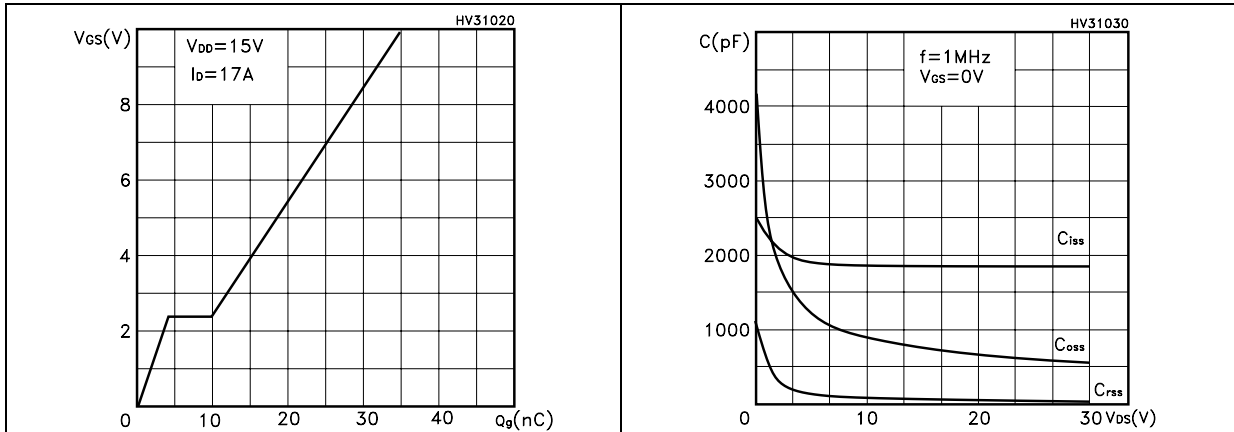


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

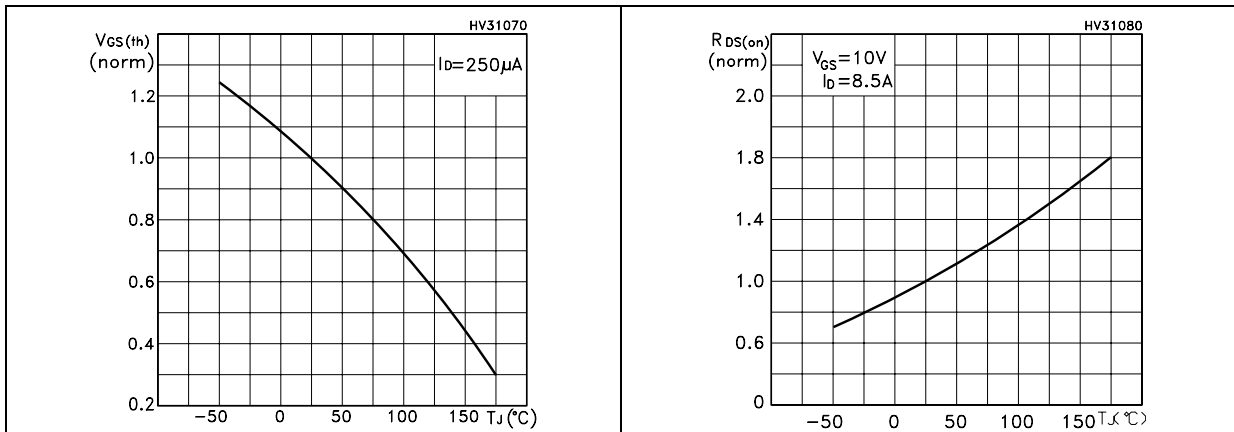
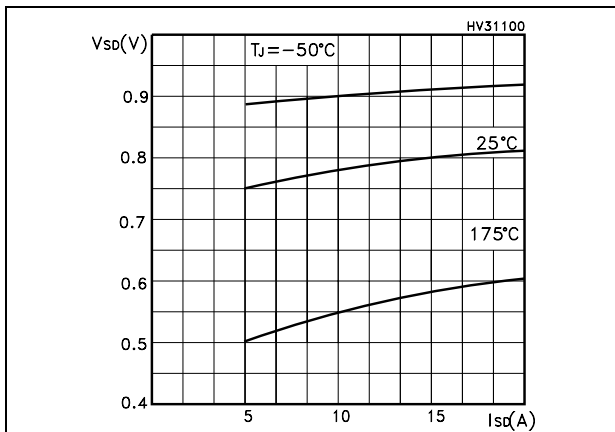


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

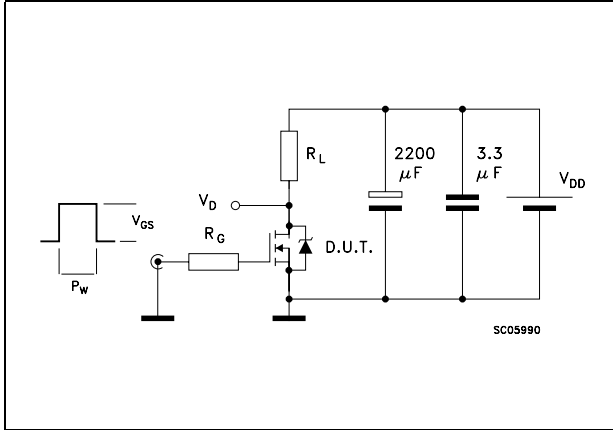


Figure 13. Gate charge test circuit

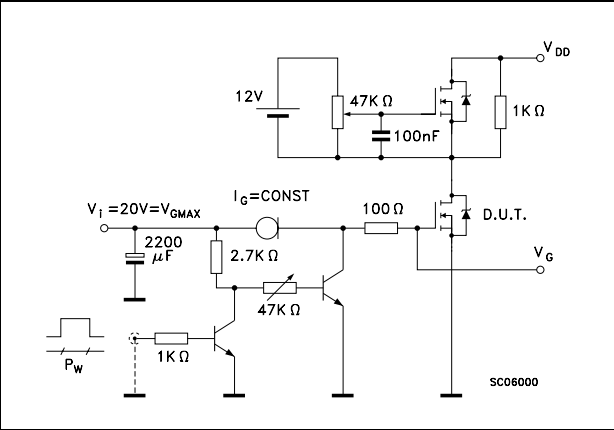


Figure 14. Test circuit for inductive load switching and diode recovery times

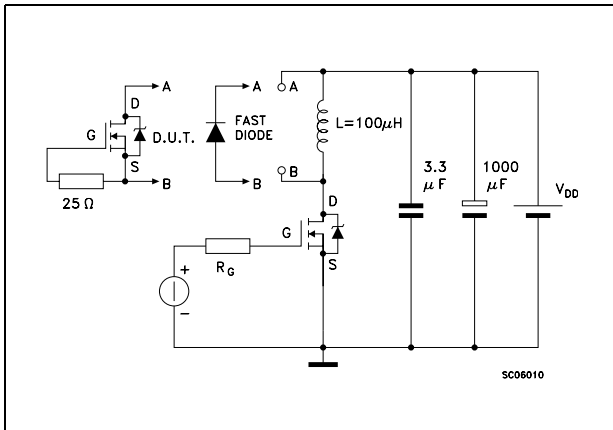


Figure 15. Unclamped inductive load test circuit

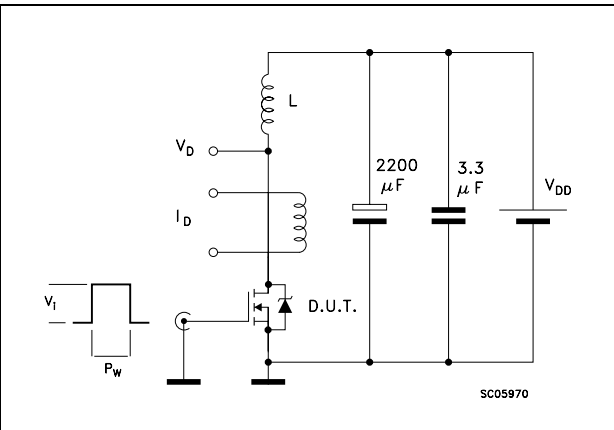


Figure 16. Unclamped inductive waveform

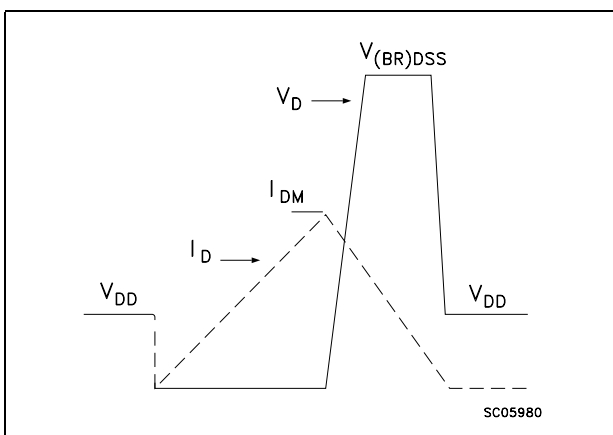
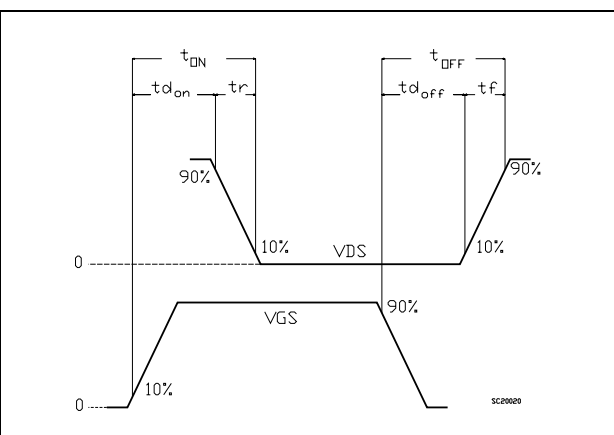


Figure 17. Switching time waveform



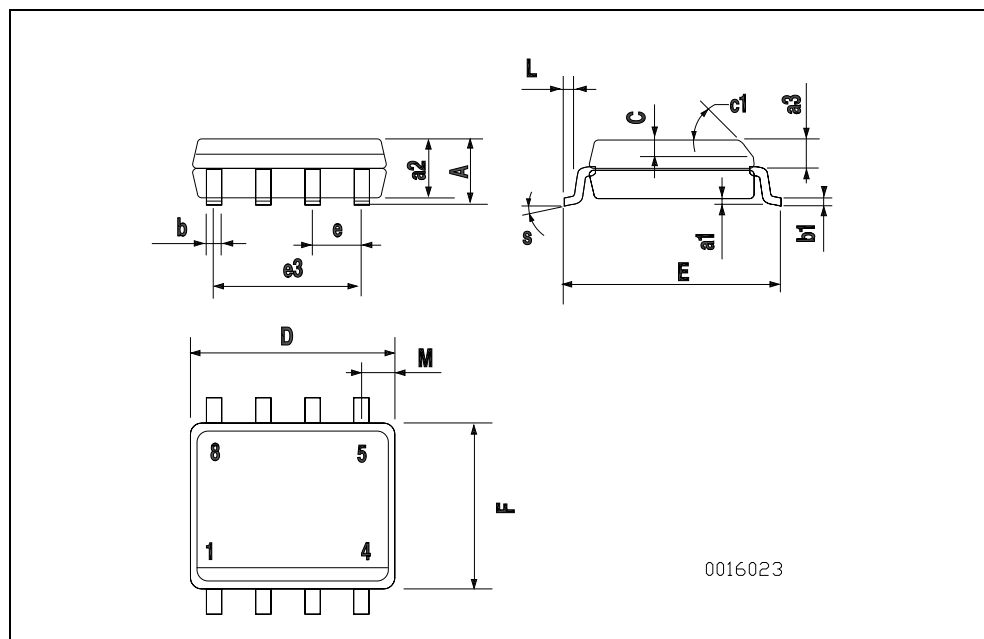


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
01-Aug-2006	1	First release
09-Jan-2007	2	Complete version

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