



STB135N10 STP135N10

N-CHANNEL 100V - 0.007 Ω - 135A D²PAK/TO-220 LOW GATE CHARGE STripFET™ POWER MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB135N10	100 V	<0.009 Ω	135 A(*)
STP135N10	100 V	<0.009 Ω	135 A(*)

- TYPICAL R_{DS(on)} = 0.007Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

This MOSFET is the result of STMicroelectronics's well established and consolidated STripFET technology utilizing the most recent layout optimization. The device exhibits extremely low on-resistance, gate charge and diode's reverse recovery charge Q_{rr} making it the ideal switch in a very large spectrum of applications such as Automotive, Consumer, Telecom and Industrial.

APPLICATIONS

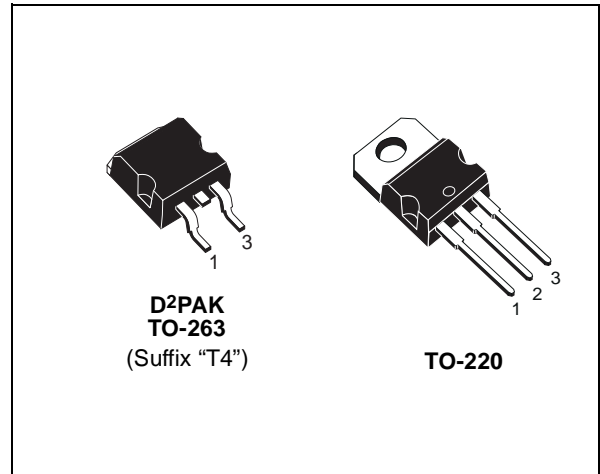
- PRIMARY SWITCH IN TELECOM DC-DC CONVERTER
- HIGH-EFFICIENCY DC-DC CONVERTERS
- 42V AUTOMOTIVE APPLICATIONS
- SYNCHRONOUS RECTIFICATION
- DIESEL INJECTION
- PWM UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

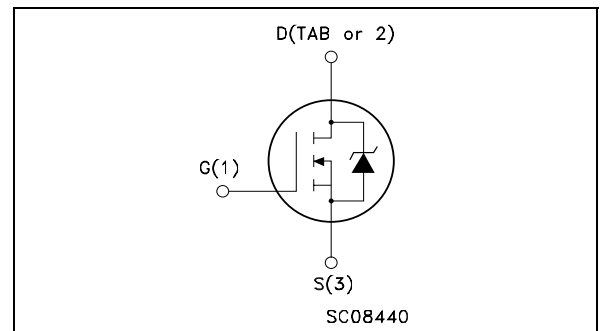
Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate- source Voltage	± 20	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	135	A
I _D	Drain Current (continuous) at T _C = 100°C	96	A
I _{DM} (1)	Drain Current (pulsed)	540	A
P _{tot}	Total Dissipation at T _C = 25°C	150	W
	Derating Factor	1	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	TBD	V/ns
E _{AS} (3)	Single Pulse Avalanche Energy	TBD	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(1) Pulse width limited by safe operating area.

(*) Value limited by wire bonding



INTERNAL SCHEMATIC DIAGRAM



STB135N10 STP135N10**THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)
OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (5)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2		4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 67.5 A		0.007	0.009	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (5)	Forward Transconductance	V _{DS} = 25 V I _D = 67.5 A		TBD		S
C _{iss}	Input Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		6350		pF
C _{oss}	Output Capacitance			890		pF
C _{rss}	Reverse Transfer Capacitance			250		pF

STB135N10 STP135N10

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 67.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 50\text{ V}$ $I_D = 135\text{ A}$ $V_{GS} = 5\text{ V}$		TBD TBD TBD	95	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 67.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain Current Source-drain Current (pulsed)				135 540	A A
$V_{SD}^{(5)}$	Forward On Voltage	$I_{SD} = 135\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 135\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns μC A

(1) Pulse width limited by safe operating area.

(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Fig. 1: Unclamped Inductive Load Test Circuit

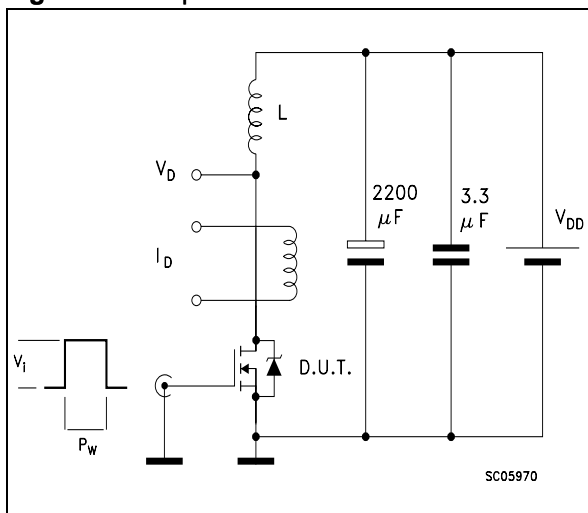


Fig. 2: Unclamped Inductive Waveform

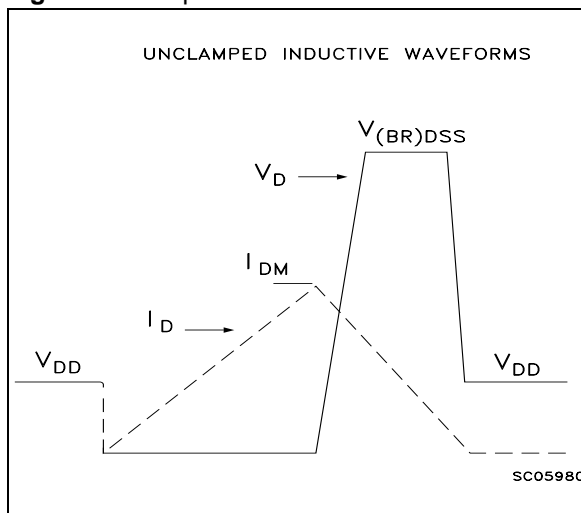


Fig. 3: Switching Times Test Circuits For Resistive Load

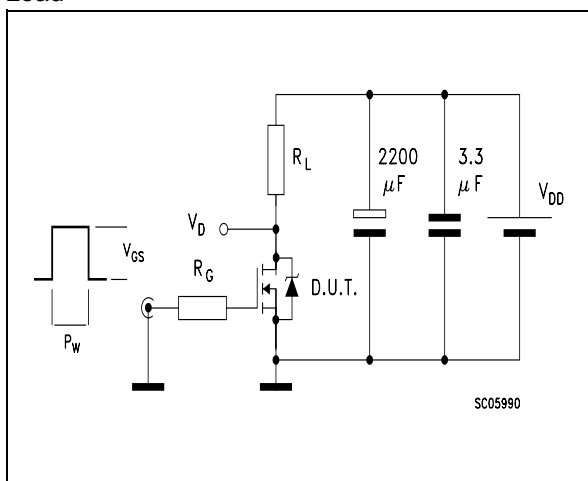


Fig. 4: Gate Charge test Circuit

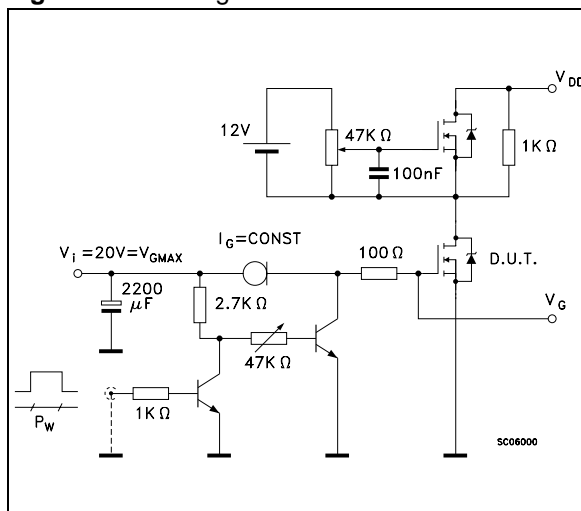
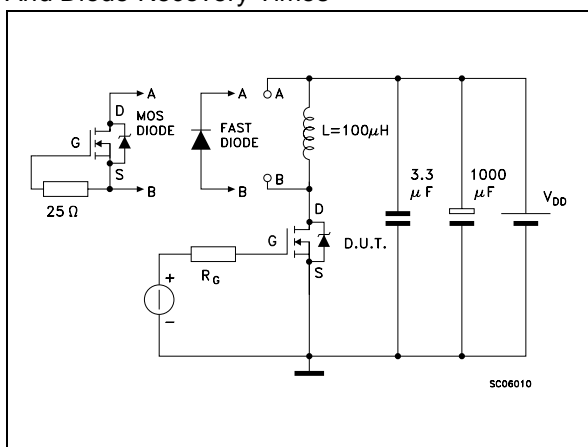
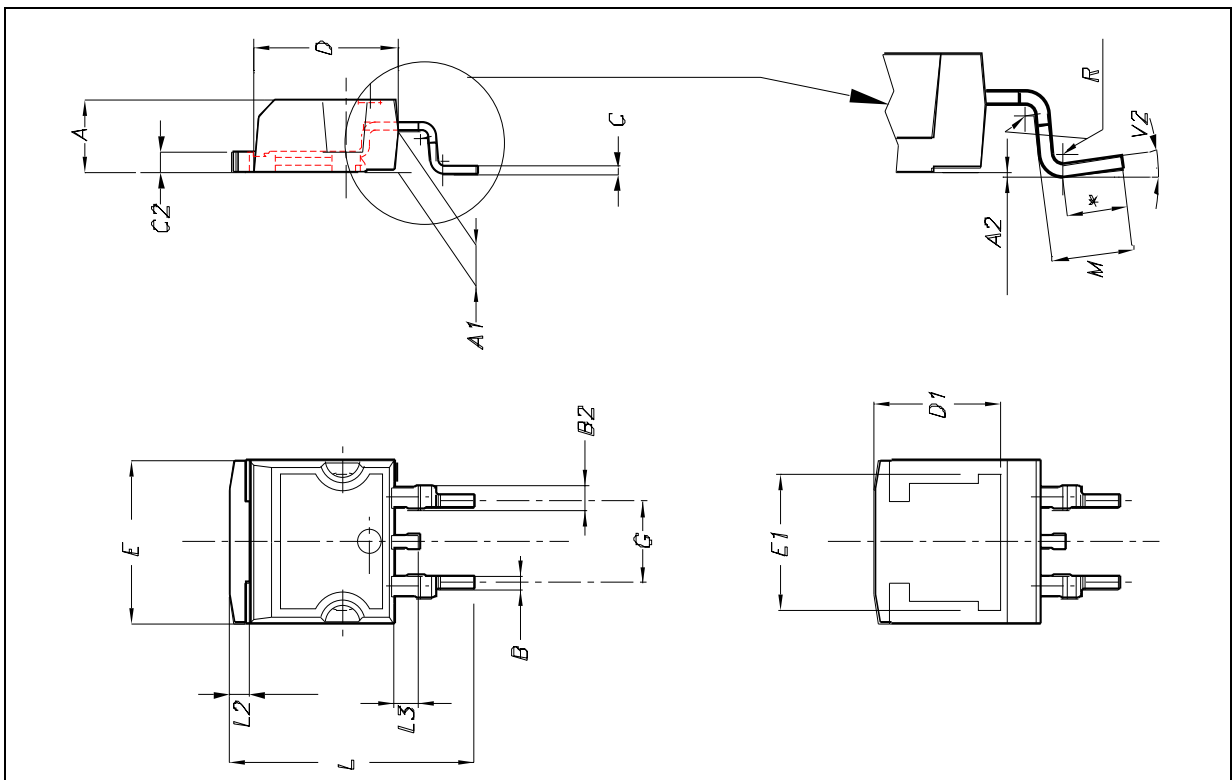


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



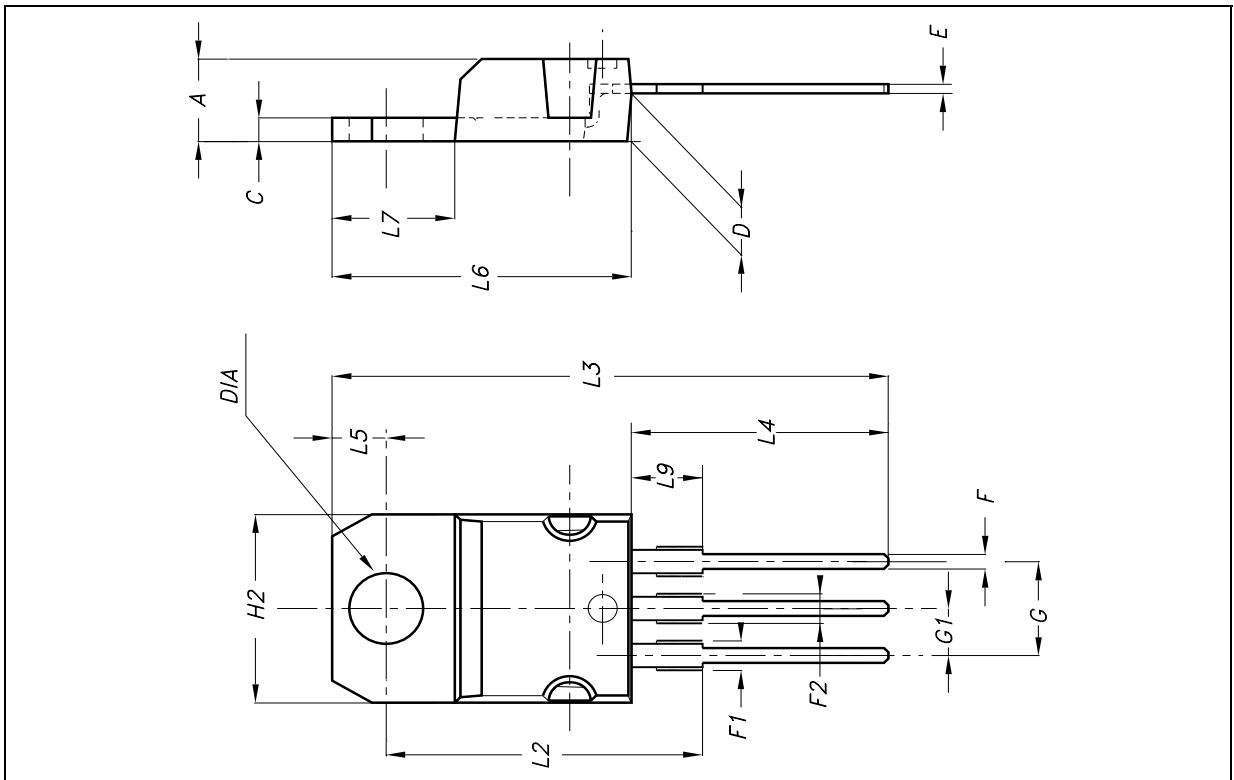
D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



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