STP120NF04

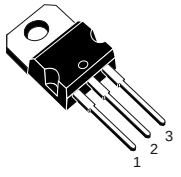
N-CHANNEL 40V - 0.0047Ω - 120A TO-220
STripFET™II MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D (1)	Pw
STP120NF04	40 V	< 0.0050Ω	120 A	300 W

- TYPICAL $R_{DS}(on)$ = 0.0047 Ω
- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

Figure 1: Package

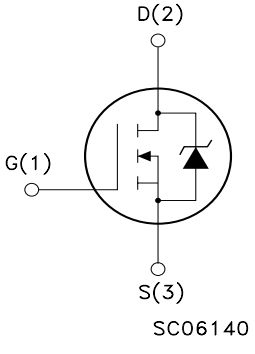


TO-220

DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 2: Internal Schematic Diagram



APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED

Table 2: Order Codes

Part Number	Marking	Package	Packaging
STP120NF04	P120NF04	TO-220	TUBE

Rev. 1

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	40	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	40	V
V_{GS}	Gate- source Voltage	± 20	V
I_D (#)	Drain Current (continuos) at T_C = 25°C	120	A
I_D	Drain Current (continuos) at T_C = 100°C	120	A
I_{DM} (•)	Drain Current (pulsed)	480	A
P_{TOT}	Total Dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	6	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	1.2	J
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	°C

(●) Pulse width limited by safe operating area
(1) I_{SD} ≤120A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$
(2) Starting T_j = 25°C, I_d = 60A, V_{DD}=30 V
(#) Current Limited by Package

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-pcb	Thermal Resistance Junction-pcb Max	See Curve on page 6	°C/W
Rthj-amb	Thermal Resistance Junction-ambient (Free air) Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	40			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2.8		4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 50 A		0.0047	0.0050	Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > =15 V , I_D =50 A		150		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		5100		pF
C_{oss}	Output Capacitance			1300		pF
C_{rss}	Reverse Transfer Capacitance			160		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 20 V, I_D = 60 A R_G = 4.7Ω V_{GS} = 10 V (see, Figure 20)		35 220		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 32V, I_D = 120 A, V_{GS} = 10V (see, Figure 22)		110 35 35	150	nC nC nC

Table 8: Switching

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 20 V, I_D = 60 A R_G = 4.7Ω V_{GS} = 10 V (see Figure 20)		80 50		ns ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				120 480	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 120 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 120 A, di/dt = 100A/µs V_{DD} = 20V, T_j = 150°C (see test circuit, Figure 21)		75 185 5		ns nC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

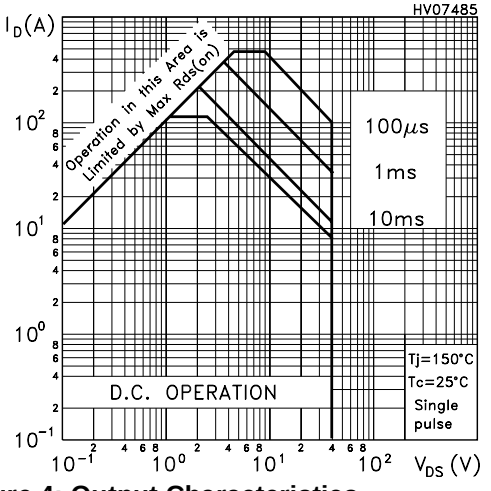


Figure 4: Output Characteristics

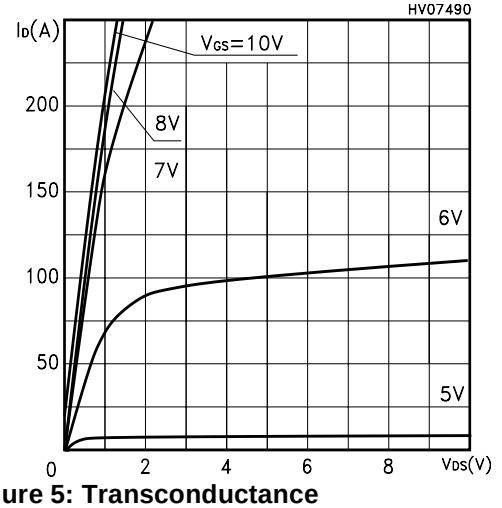


Figure 5: Transconductance

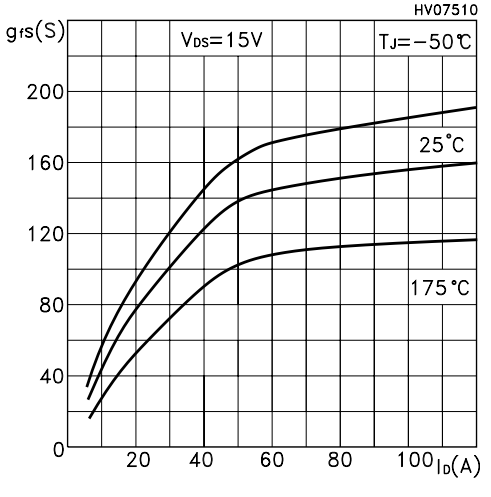


Figure 6: Thermal Impedance

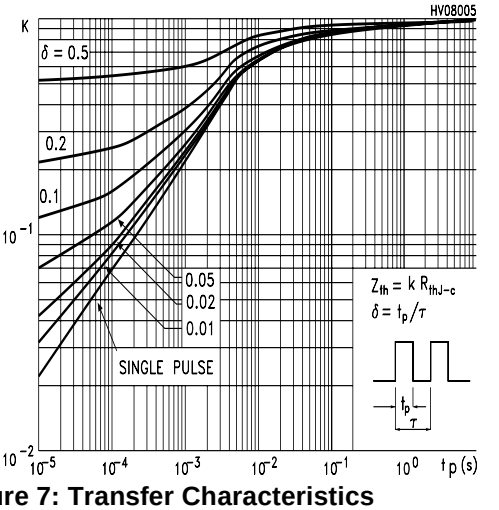


Figure 7: Transfer Characteristics

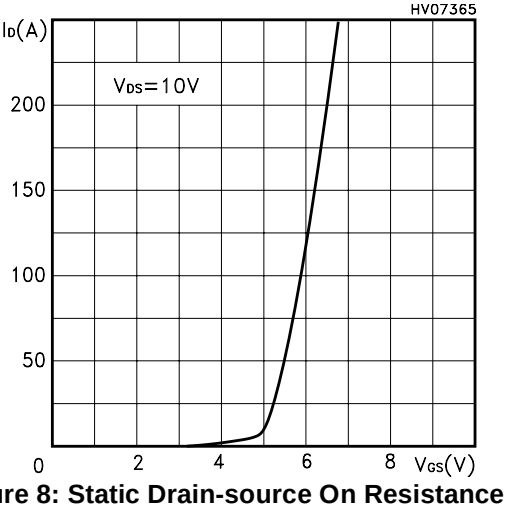


Figure 8: Static Drain-source On Resistance

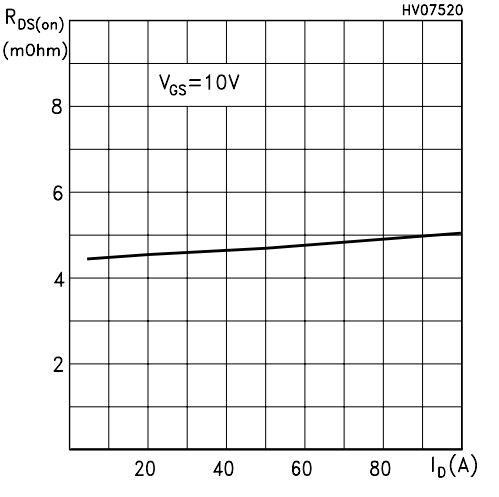


Figure 9: Gate Charge vs Gate-source Voltage

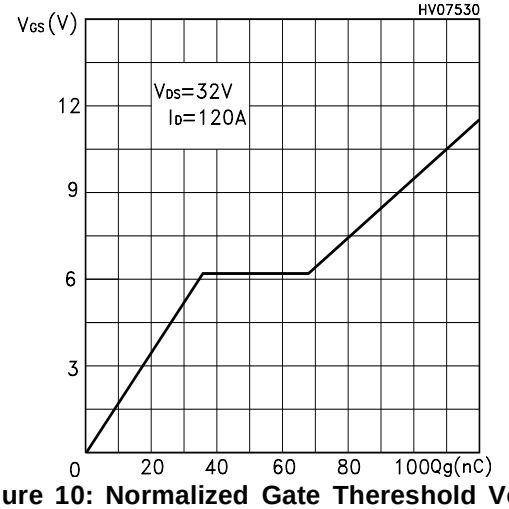


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

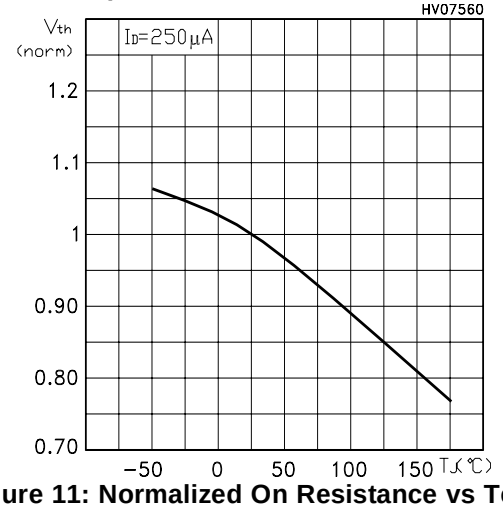


Figure 11: Normalized On Resistance vs Temperature

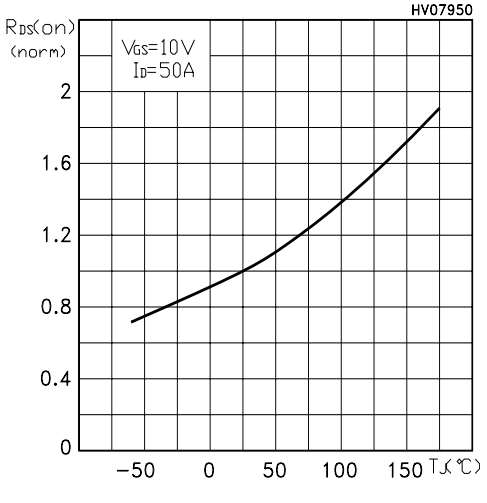


Figure 12: Capacitance Variation

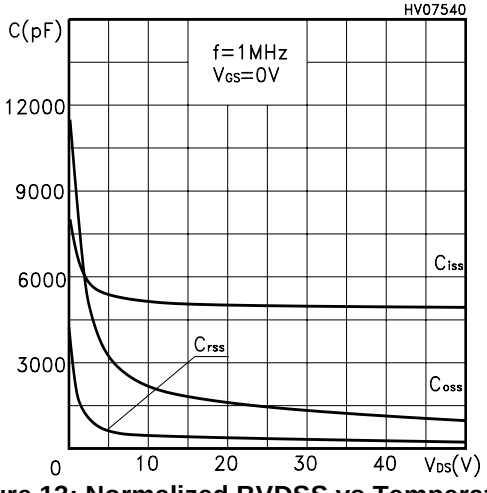


Figure 13: Normalized BVDSS vs Temperature

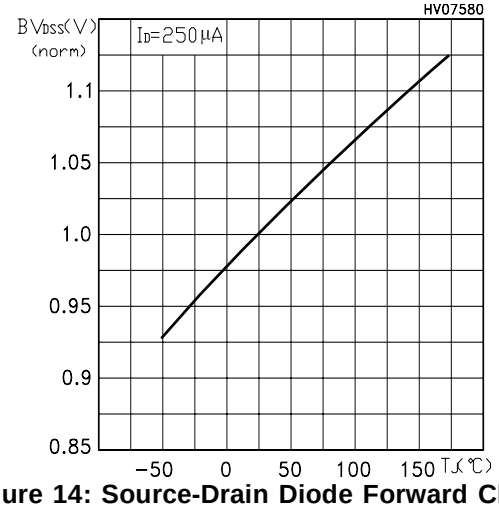


Figure 14: Source-Drain Diode Forward Characteristics

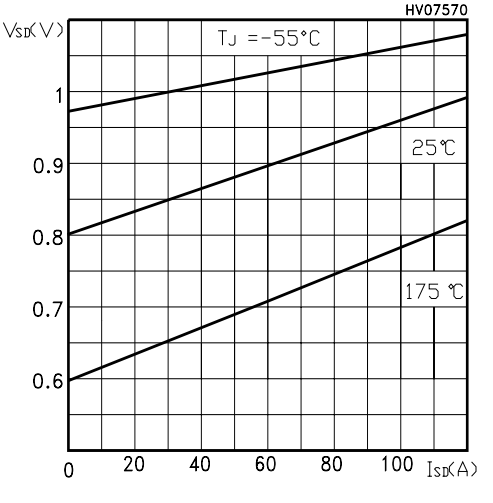


Figure 15: Power Derating vs Tc

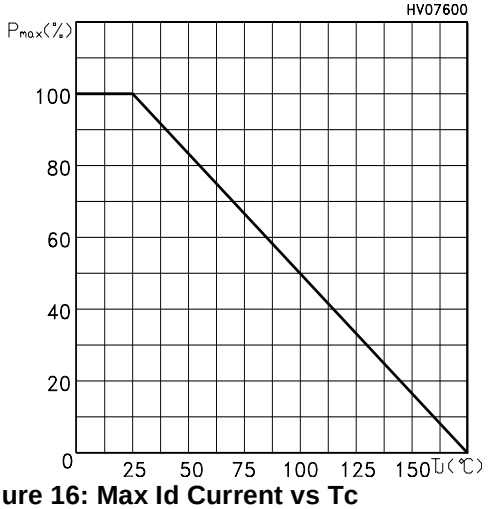


Figure 16: Max Id Current vs Tc

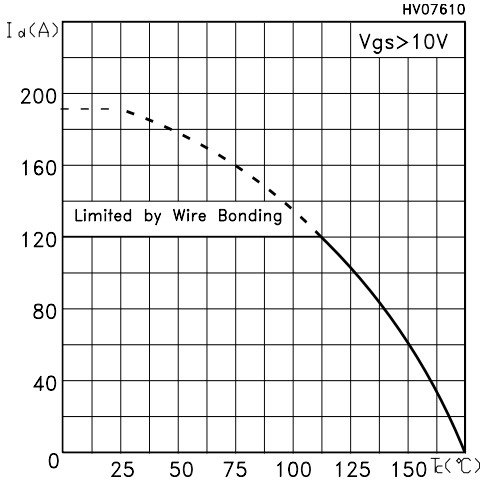


Figure 17: Thermal Resistance Rthj-a vs PCB Copper Area

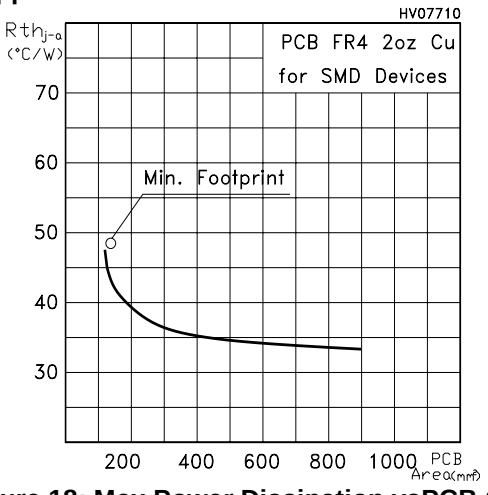


Figure 18: Max Power Dissipation vsPCB Copper Area

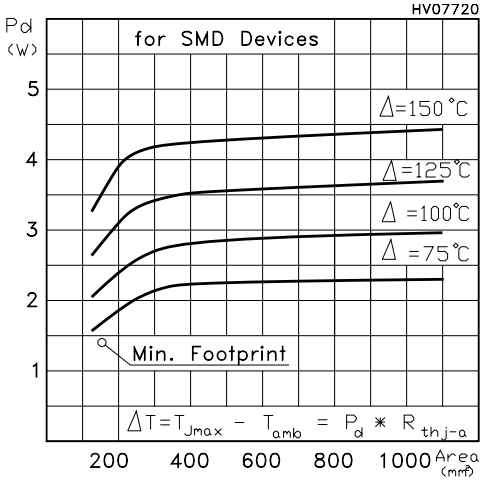
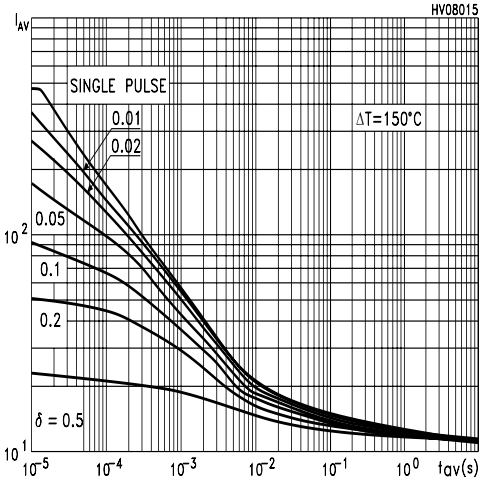


Figure 19: Allowable Iav vs Time in Avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

To derate above 25 °C, at fixed I_{AV}, the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

Where:

$Z_{th} = K * R_{th}$ is the value coming from Normalized Thermal Response at fixed pulse width equal to T_{AV}.

Figure 20: Switching Times Test Circuit For Resistive Load

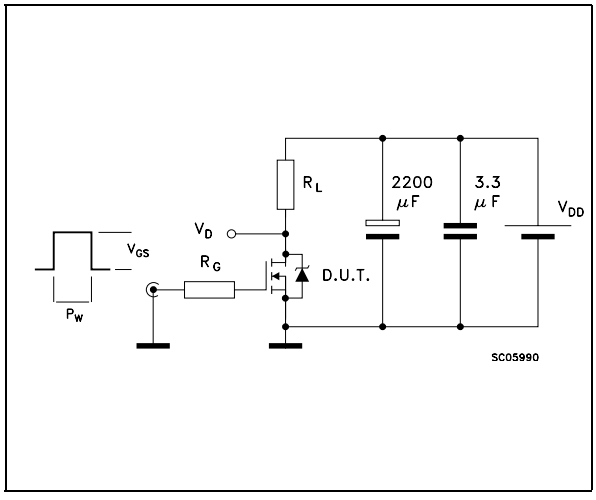


Figure 21: Test Circuit For Diode Recovery Times

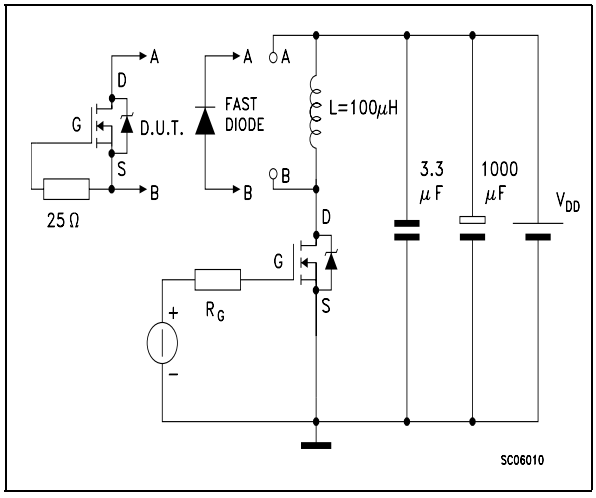
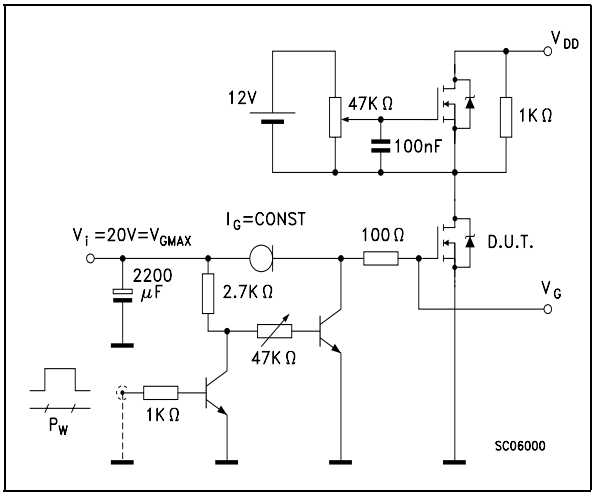


Figure 22: Gate Charge Test Circuit



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

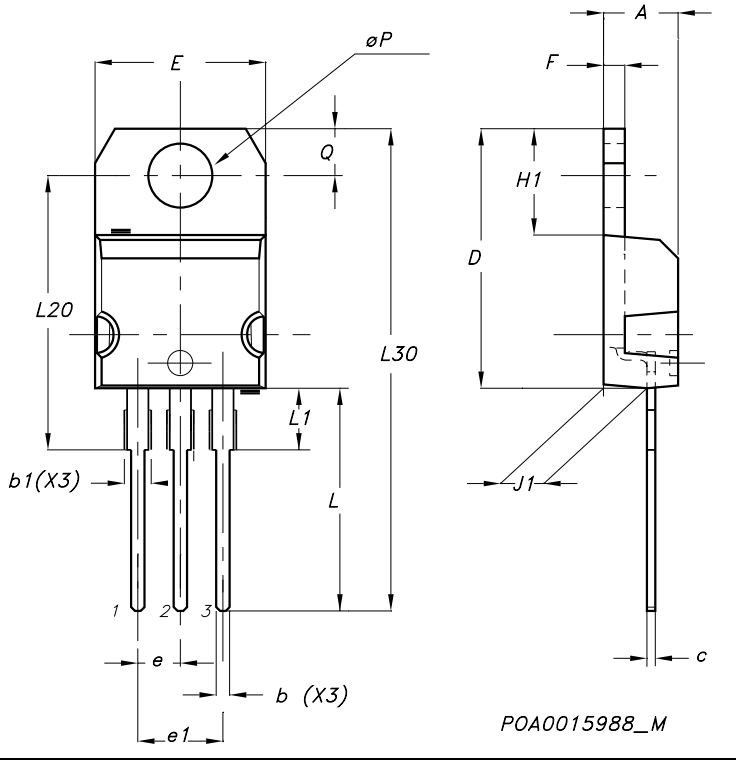


Table 10: Revision History

Date	Revision	Description of Changes
15-Feb-2005	1	First Release.