

**-1.7A**

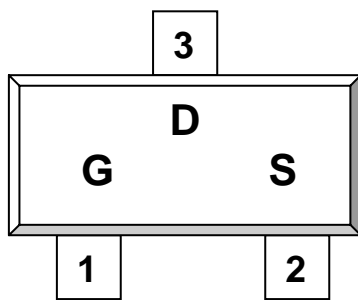
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**DESCRIPTION**

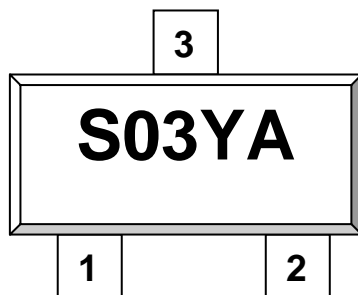
The ST2303 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION****SOT-23-3L**

1.Gate 2.Source 3.Drain

**FEATURE**

- -30V/-2.6A,  $R_{DS(ON)} = 130\text{m-ohm}$  @VGS = -10V
- -30V/-2.0A,  $R_{DS(ON)} = 180\text{m-ohm}$  @VGS = -4.5V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

S: Subcontractor Y: Year Code W: Process Code

**STANSON TECHNOLOGY**120 Bentley Square, Mountain View, Ca 94040 USA  
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**P Channel Enhancement Mode MOSFET      ST2303**

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**ABSOLUTE MAXIMUM RATINGS** (Ta = 25 Unless otherwise noted )

<b>Parameter</b>	<b>Symbol</b>	<b>Typical</b>	<b>Unit</b>
Drain-Source Voltage	V <sub>DSS</sub>	-30	V
Gate-Source Voltage	V <sub>GSS</sub>	+20	V
Continuous Drain Current (T <sub>J</sub> =150 )	I <sub>D</sub>	T <sub>A</sub> =25	A
		T <sub>A</sub> =70	-2.0
Pulsed Drain Current	I <sub>DM</sub>	-10	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.25	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25	W
		T <sub>A</sub> =70	0.8
Operation Junction Temperature	T <sub>J</sub>	150	
Storage Temperature Range	T <sub>STG</sub>	-55/150	
Thermal Resistance-Junction to Ambient	R <sub>JA</sub>	100	/W

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**ELECTRICAL CHARACTERISTICS ( Ta = 25    Unless otherwise noted )**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-10\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=+20V$			+100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-30V, V_{GS}=0V$			-1	uA
		$V_{DS}=-30V, V_{GS}=0V$ $T_J=55$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -5V, V_{GS}=-10V$	-6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-2.6A$		0.095	0.130	
		$V_{GS}=-4.5V, I_D=-2.0A$		0.125	0.180	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-1.7V$		2.4		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.25A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-10V$ $I_D = -1.7A$		5.8	10	nC
Gate-Source Charge	$Q_{gs}$			0.8		
Gate-Drain Charge	$Q_{gd}$			1.5		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $F=1MHz$		226		PF
Output Capacitance	$C_{oss}$			87		
Reverse Transfer Capacitance	$C_{rss}$			19		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6$		9	20	nS
	$t_r$			9	20	
Turn-Off Time	$t_{d(off)}$			18	35	
	$t_f$			6	20	



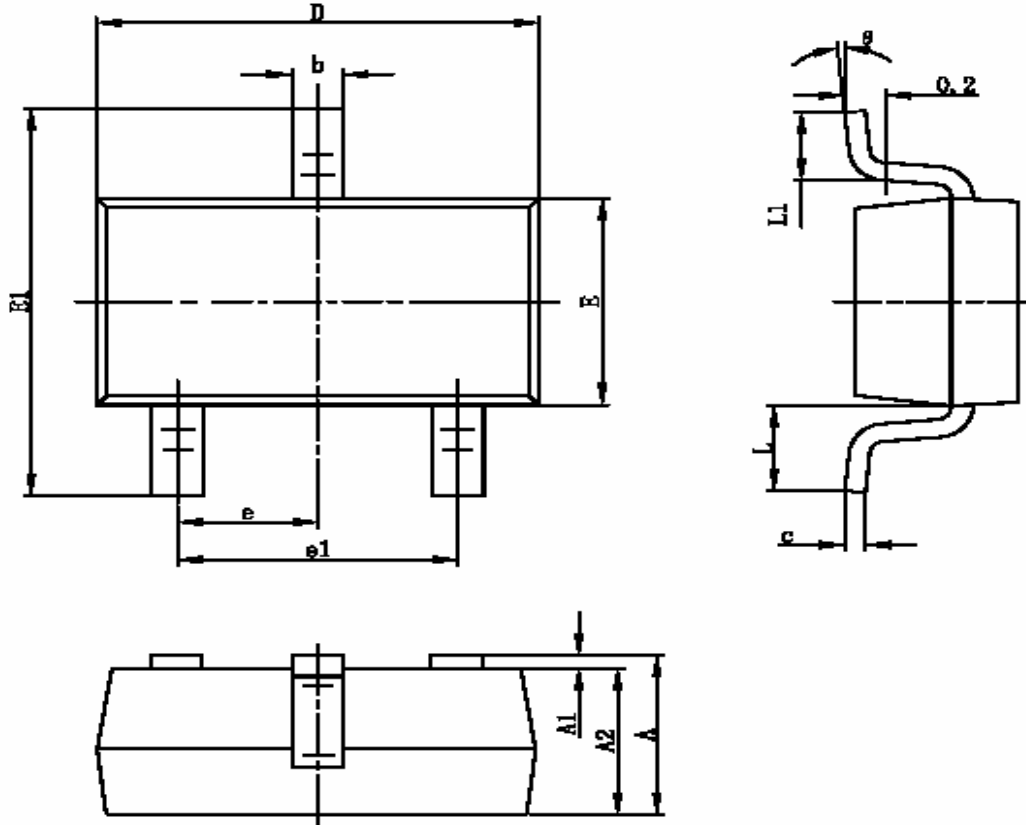
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SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



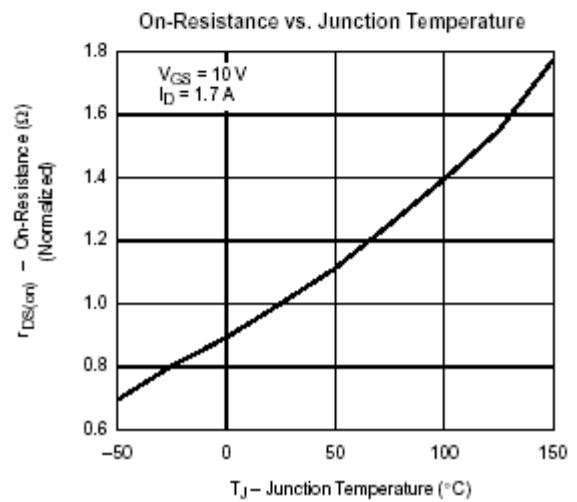
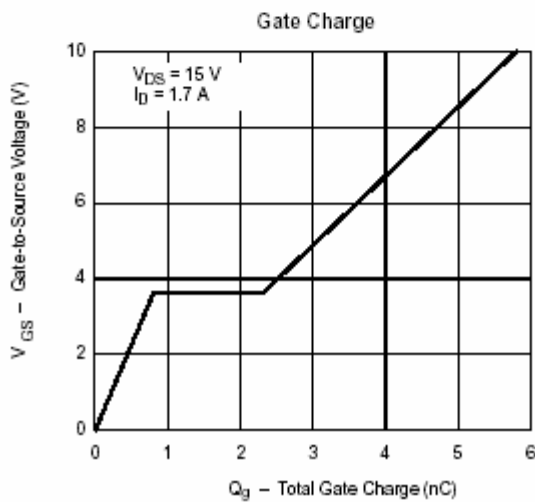
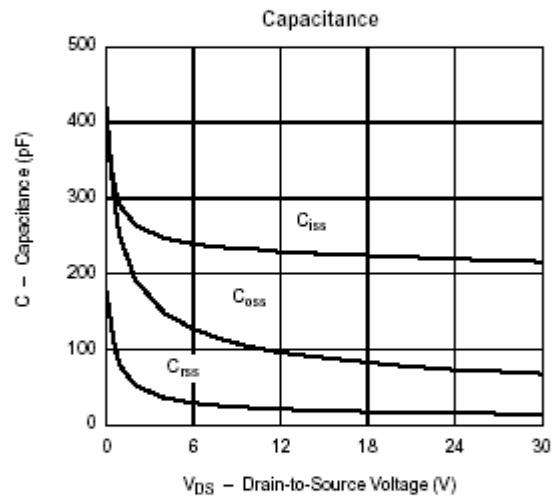
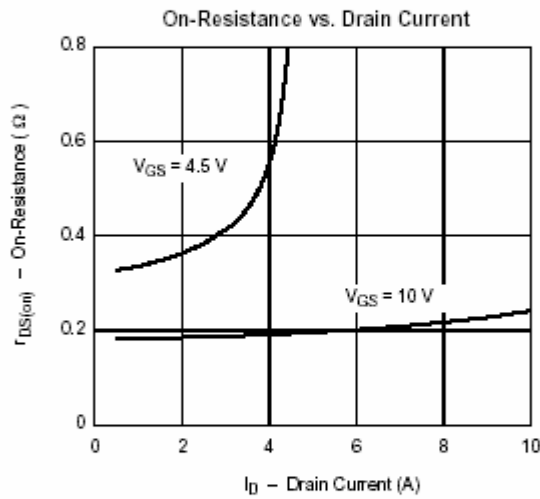
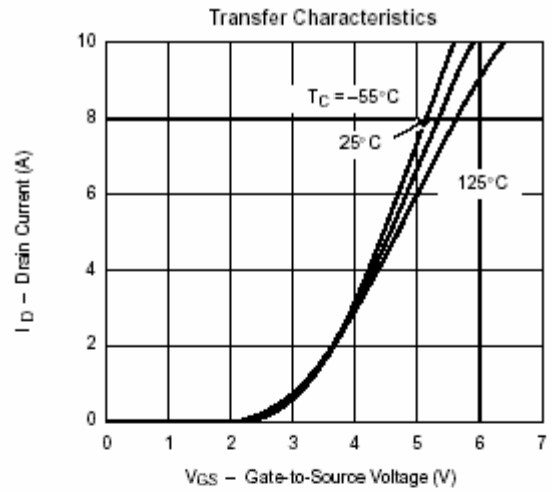
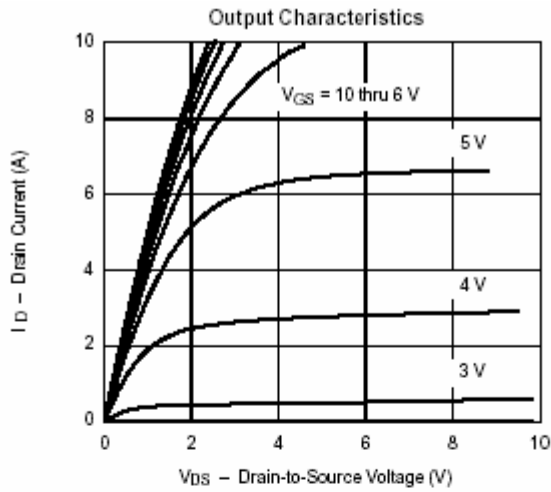
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TYPICAL CHARACTERISTICS (25 Unless noted)



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