SENSITRON
SEMICONDUCTOR

SPM6M020-060D

TECHNICAL DATA
Datasheet 4982, Rev. –

Three-Phase MOSFET BRIDGE, With Gate Driver and Optical Isolation, 600 VOLT, 20 AMP

ELECTRICAL CHARACTERISTICS PER IGBT DEVICE (Tj=25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MOSFET SPECIFICATIONS					
Drain to Source Breakdown Voltage I_C = 250 μA, V_{GS} = 0V	BV_{CSS}	600	-		V
Continuous Drain Current T_C = 25 ^{O}C T_C = 90 ^{O}C	I_D	-	-	20 10	A
Pulsed Drain Current, 1mS	I_{DM}			40	A
Gate to Source Voltage	V_{GS}	-	-	+/-20	V
Gate-Source Leakage Current , V_{GS} = +/-20V	I_{GSS}			+/- 100	nA
Gate Threshold Voltage, I_C=1mA	$V_{GS(TH)}$	2.0		4.0	V
Zero Gate Voltage Drain Current V_{CS} = 600 V, V_{GE}=0V T_i=25°C V_{CS}= 480 V, V_{GE}=0V T_i=125°C	I_{CSS}	-	- 	 250 500	 μA μA
On-State Resistance, T_C = 25 ^{O}C T_C = 150 ^{O}C I_D = 10A, V_{CC} = 15V,	R_{DSon}	-	0.19 0.43	0.20	V
Input Capacitance Output Capacitance Reverse Transfer Cap. V_{CS} = 25 V, V_{GE} = 0 V, f = 1 MHz	C_{iss} C_{oss} C_{res}		2400 780 50		pF
Over-Temperature Shutdown					
Over-Temperature Shutdown	Tsd	100	107	115	^{o}C
Over-Temperature Output	Tso		10		mV/^{o}C
Temperature Sensor Output DC Offset			+0.0		mV
Accuracy, at temperature range from 0 ^{o}C to 125 ^{o}C			+/-1.0	+/-2.0	^{o}C
Over-Temperature Shutdown Hysteresis			20		^{o}C

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Gate Driver , - 40°C <T$_C$< 125°C

Description	Symbol				Unit
Supply Voltage	VCC	10	15	20	V
Input On Current	HIN, LIN	2		5.0	mA
Opto-Isolator Logic High Input Threshold	I$_{th}$	-	1.6	-	mA
Input Reverse Breakdown Voltage	BV$_{in}$	5.0	-	-	V
Input Forward Voltage @ I$_{in}$ = 5mA	V$_F$	-	1.5	1.7	V
Under Voltage Lockout	VCCUV	11.5	-	12.5	V
ITRIP Reference Voltage [1]	Itrip-ref	1.60	1.65	1.7	V
Input-to-Output Turn On Delay	t$_{ond}$	-	500	700	nsec
Output Turn On Rise Time	t$_r$	-	20	30	
Input-to-Output Turn Off Delay	t$_{offd}$	-	550	750	
Output Turn Off Fall Time	t$_f$	-	20	30	
At (VDD=200V, RD=20Ω, ID=10A), T$_j$ = 25 to 125 ^{O}C					
Input-Output Isolation Voltage	-	1500	-	-	V

Module

Description	Symbol				Unit
Maximum operating Junction Temperature	T$_{jmax}$	-40	-	150	^{o}C
Maximum Storage Junction Temperature	T$_{jmax}$	-55	-	150	^{o}C
Maximum Thermal Resistance (Junction to Module base plate) per Mosfet	R$_{\theta JB}$	-	-	0.80	^{o}C/W
DC Bus Absolute Maximum Voltage	V+			600	V
DC Bus Recommended Voltage	V+	100		400	V
DC Bus Absolute Maximum Current, T$_C$= 25 ^{O}C [2]	Idc			20	A

(1) ITRIP Cycle-by cycle current limit is internally set to 17A peak. The set point can be lowered by connecting a resistor between Itrip-ref and Gnd. The set point can be increased by connecting a resistor between Itrip-ref and +5V ref

(2) At elevated case temperature above 25°C, the device shall be derated so that the power MOSFETs maximum Junction temperature is 150°C.
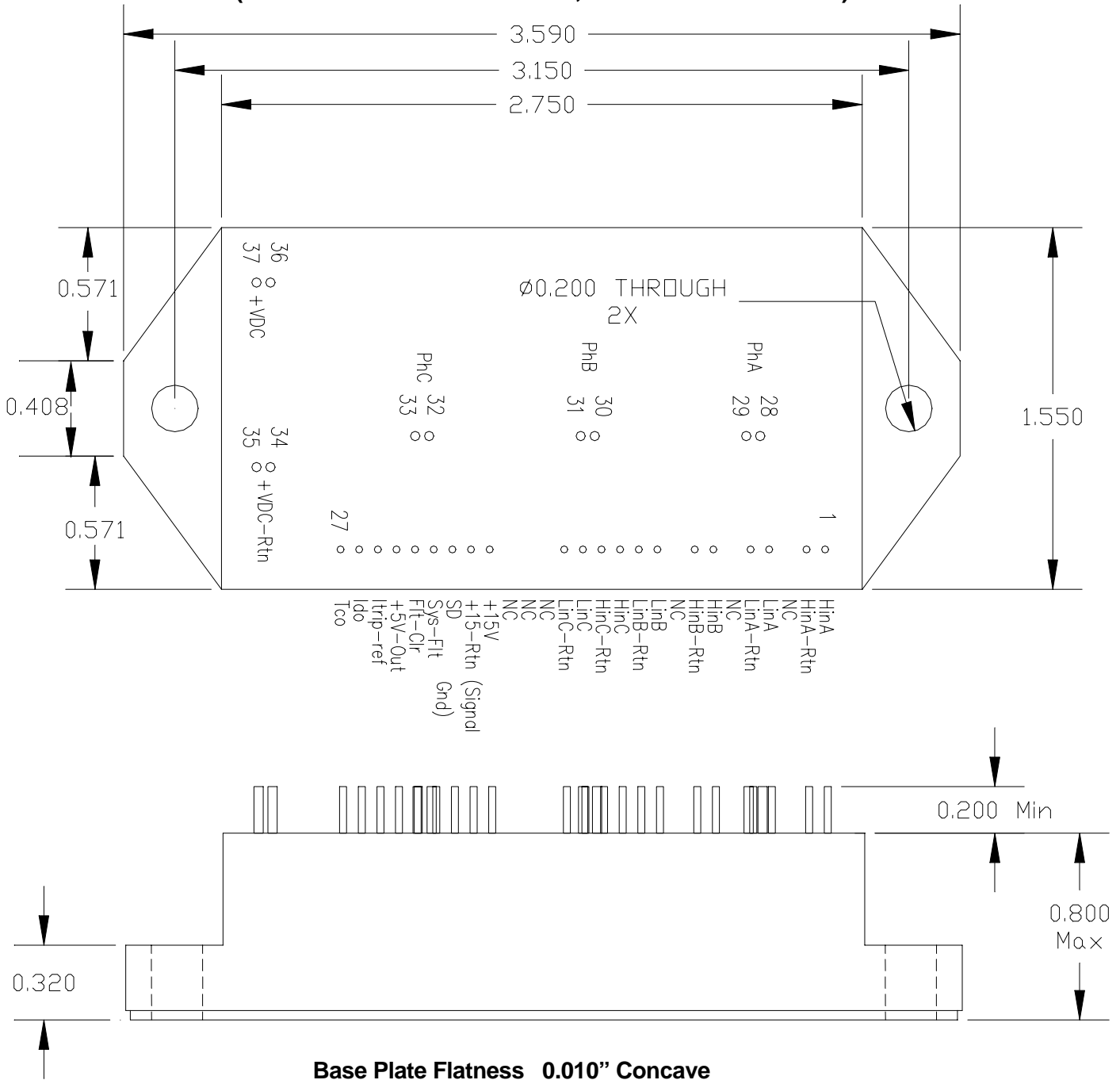
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Pin Description

Pin Number	Function	Pin Number	Function
1	Isolated Input for High-side IGBT of Phase A	18	NC
2	Return for Input at 1	19	+15V Input
3	NC	20	+15V Rtn (Signal Ground) [2]
4	Isolated Input for Low-side IGBT of Phase A	21	SD [2]
5	Return for Input at 4	22	Fault Output [2]
6	NC	23	Fault Clear Input [2]
7	Isolated Input for High-side IGBT of Phase B	24	+5V Output
8	Return for Input at 7	25	Over-Current Trip Set Point [2]
9	NC	26	DC Bus Current Output with Total Gain of 0.10 V/A
10	Isolated Input for Low-side IGBT of Phase B	27	Case Temperature Output with Gain of 0.010 V/°C
11	Return for Input at 10	28 &29	Phase A Output
12	Isolated Input for High-side IGBT of Phase C	30 & 31	Phase B Output
13	Return for Input at 12	32 & 33	Phase C Output
14	Isolated Input for Low-side IGBT of Phase C	34 & 35	DC Bus "+VDC Return"
15	Return for Input at 14	36 & 37	DC Bus "+VDC" Input
16	NC	Case	Isolated From All Terminals
17	NC		

(2) See Pin Description.

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Package Drawing Top View
(All dimensions are in inches, tolerance is +/- 0.010")

Base Plate Flatness   0.010" Concave

Figure 2.   Mechanical Outlines

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Package Pin Locations
(All dimensions are in inches; tolerance is +/- 0.005" except otherwise specified)
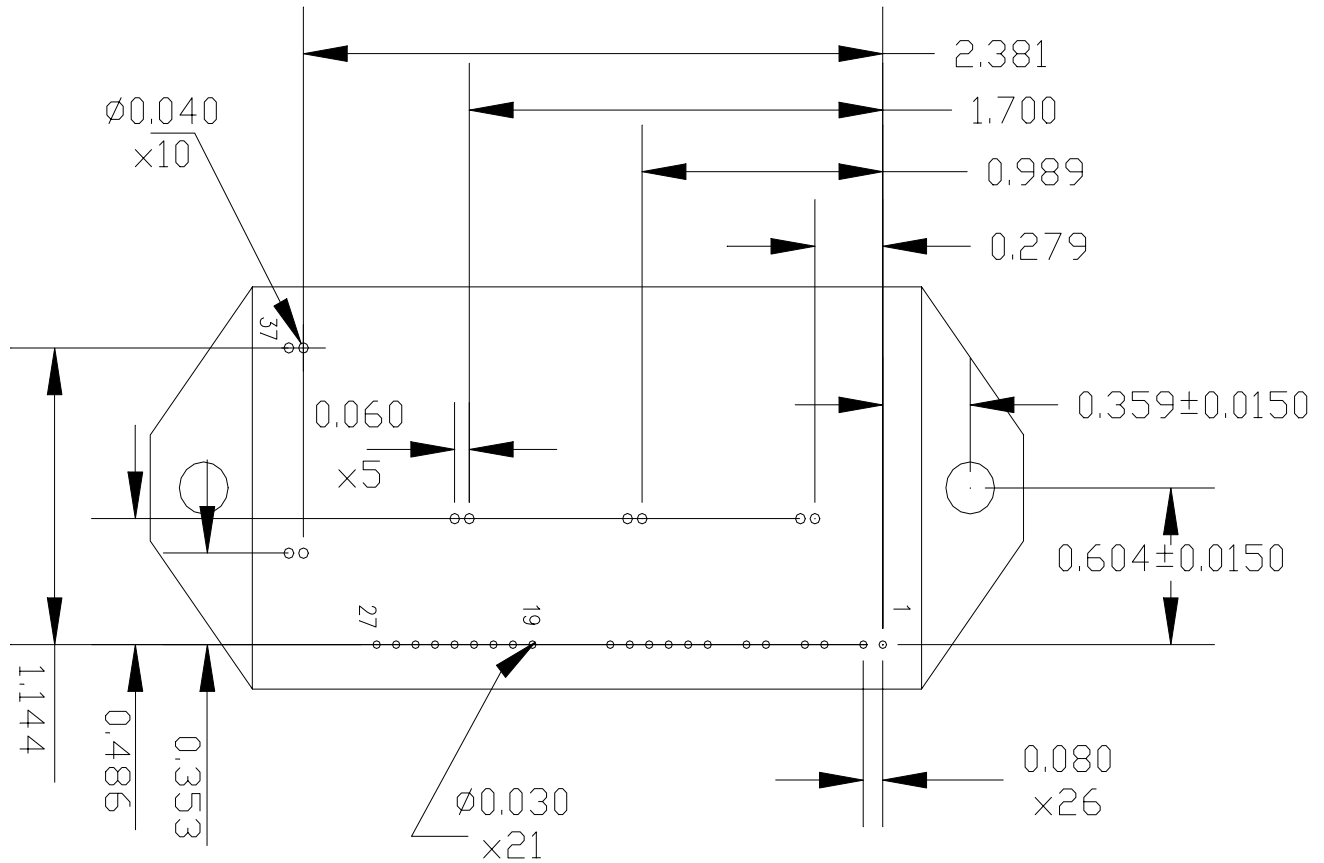
Figure 3.   Mechanical Outlines

Package Material:
 Base: Copper
 Frame: Epoxy Molded
 Case: Epoxy Molded
 Power Terminals: Copper

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Normalized Thermal Impedance Curves for Each MOSFET
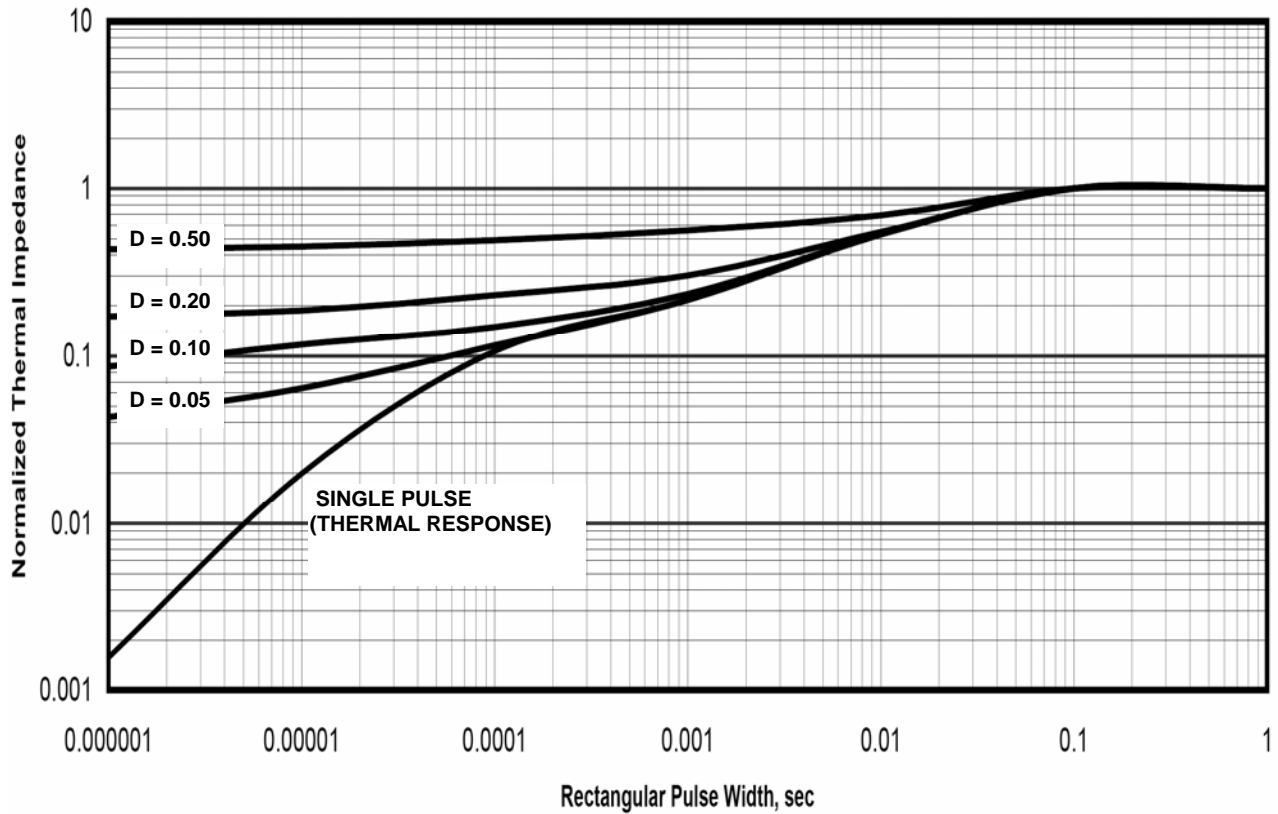
Figure 4. Normalized Transient Thermal Impedance, Junction-to-Case

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Pin Descriptions

LinA (Pin 1), is an isolated drive input for Low-side IGBT of Phase A.

LinA-R (Pin 2), Return for Input at Pin1.

HinA (Pin 4), is an isolated drive input for High-side IGBT of Phase A.

HinA-R (Pin 5), Return for Input at Pin4.

LinB- (Pin 7), is an isolated drive input for Low-side IGBT of Phase B.

LinB-R (Pin 8), Return for Input at Pin7.

NC (Pins,3,6, 9,16,17,18), NC

HinB (Pin 10), is an isolated drive input for High-side IGBT of Phase B.

HinB-R (Pin 11), Return for Input at Pin10.

LinC (Pin 12), is an isolated drive input for Low-side IGBT of Phase C.

LinC-R (Pin 13), Return for Input at Pin12.

HinC (Pin 14), is an isolated drive input for High-side IGBT of Phase C.

HinC-R (Pin 15), Return for Input at Pin14.

Recommended input turn-on current for all six drive signals is 5-8mA.
For higher noise immunity the tri-state differential buffer, DS34C87, is recommended as shown in Fig. 5.

Note : Connect LinA to non-inverting output for a non-inverting input logic.
Connect LinA to inverting output for an inverting input logic.
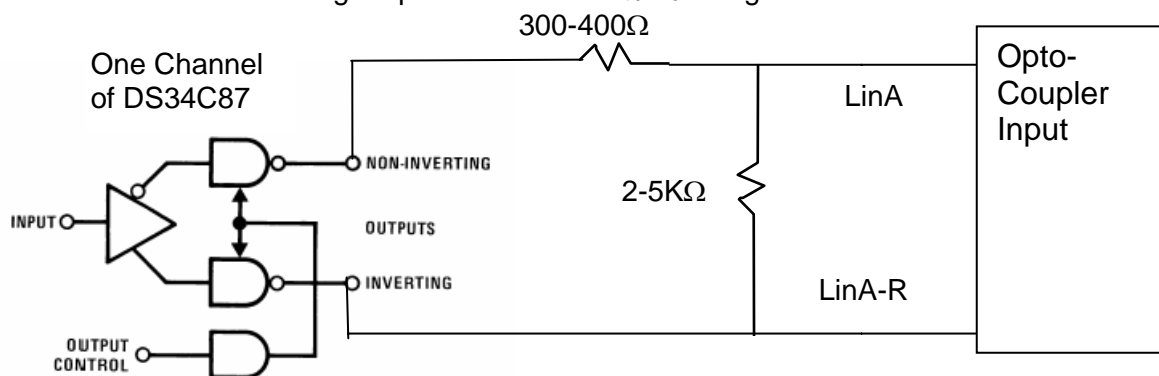
Fig. 5. Input Signal Buffer

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Vcc (Pin 19), is the +15V input biasing supply connection for the controller. Under-voltage lockout
 keeps all outputs off for Vcc below 10.5V. Vcc pin should be connected to an isolated 15V power supply.
 Vcc recommended limits are 14V to 16V , and shall not exceed 18V. The return of Vcc is pin 21.
Recommended supply capability is about 70mA.

+15V Rtn (Pin 20), is signal ground. This pin is internally connected to DC Bus return.
No external connection shall be established between Signal Gnd and +VDC Rtn.

SD (Pin 21), is a dual function input/output pin. It is an active low input. It is internally pulled high to +5V
 by 2.74K Ω. As a low input it shuts down all IGBTs regardless of the Hin and Lin signals.
SD is internally activated due to desaturation protection, over-temperature shutdown, or over-current
 shutdown.
Desaturation shutdown is a latching feature.
SD can be used to shutdown all IGBTs except the brake IGBT by an external command. An open
 collector switch shall be used to pull down SD externally.
Also, SD can be used as a fault condition output. Low output at SD indicates a latching fault situation.

Flt (Pin 22), is a dual function input/output pin. It is an active low input. It is internally pulled high to +5V by
 2.74K Ω. If pulled down, it will freeze the status of all the six IGBTs regardless of the Hin and Lin signals.
As an output, Pin 22, reports desaturation protection activation. When desaturation protection is activated
 a low output for about 9 μsec is reported.
If any other protection feature is activated, it will not be reported by Pin 22.

Flt-Clr(Pin 23), is a fault clear input. It can be used to reset a latching fault condition, due to desaturation
 protection.
Pin 23 an active high input. It is internally pulled down by 2.0KΩ. A latching fault due to desaturation can be
 cleared by pulling this input high to +5V by 200-500Ω, or to +15V by 3-5KΩ.
It is recommended to activate fault clear input for more than 100 μsec at startup.

**+5V Output (Pin 24),** is a +5V output. Maximum output current is 20mA.

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Itrip-Ref (Pin 25), is an adjustable voltage divider reference for over-current shutdown. Internal pull-up to +5V by 31.6KΩ, pull down to ground is 10.0KΩ, and hysteresis resistance of 49.9KΩ. The internal set point is 1.65V, corresponding to over-current shutdown of 35A. The re-start delay time is about 50 usec.

Idco (Pin 26), is an absolute value current sense output of DC bus current. The sensor gain is 0.05V/A. The internal impedance of this output is 1KΩ, and internal filter capacitance is 1nF. The frequency response bandwidth of this signal is about 200KHz.

TCo (Pin 27), is an analog output of case temperature sensor. The sensor output gain is 10.0mV/^{o}C, with 0.0 V DC offset. This sensor can measure positive ^{o}C. The internal impedance of this output is 8.87KΩ. The internal block diagram of the temperature sensor is shown in Fig. 6.
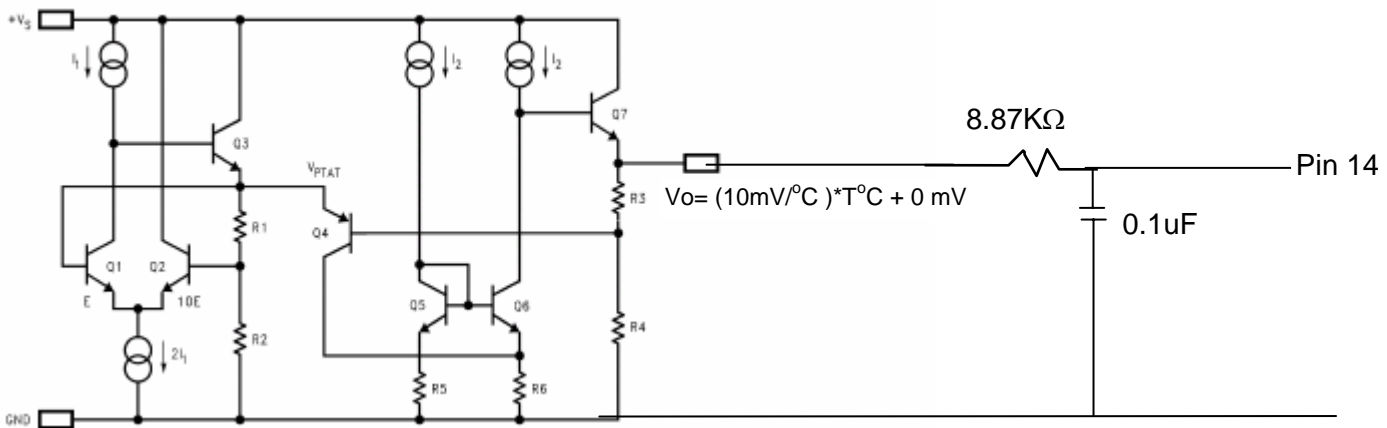
Fig. 6 Temperature Sensor Internal Block Diagram

The output voltage reading vs temperature will be:
TCo = + 0.25V at Tc=25°C
TCo = + 1.25V at Tc=125°C

PhA (Pins 28, 29), is Phase A output.

PhB (Pins 30, 31), is Phase B output.

PhC (Pins 32, 33), is Phase C output.

+VDC Rtn (Pins 34, 35), is DC Bus return.

+VDC (Pins 36, 37), is +DC Bus input.

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Application Notes

a- System Start Up Sequence:

Activate fault clear input for about 100 μsec at startup. The micro-controller enable output is inverted and fed to the second DS34C87 control input. When the controller is in disable mode, the Flt-clr is enabled and Phase C low-side IGBT is turned on. This allows for the bootstrap circuit of the high-side IGBT of Phase C to be charged. At the same time, the high-side bootstrap circuits of Phases A and B will charge through the motor winding. Once the controller is enabled, PWM signals of all channels should start.
Fig. 7 shows a recommended startup circuit.

Notes:
1- Gnd1 and Gnd2 are isolated grounds from each other.
2- The +5V power supply used for DS34C87 is an isolated power supply.
3- The +15V power supply used for SPM6G070-060D is an isolated power supply.
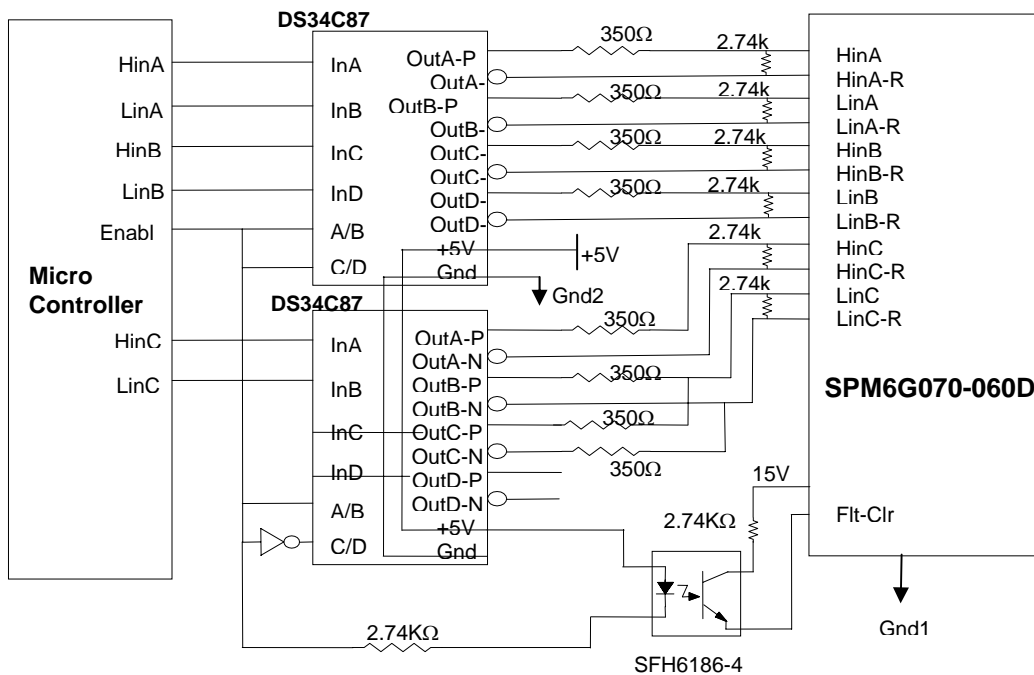
Fig. 7 Input Interface and Startup Circuit

Truth Table For DS34C87

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

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b- DC Bus Charging from 15V
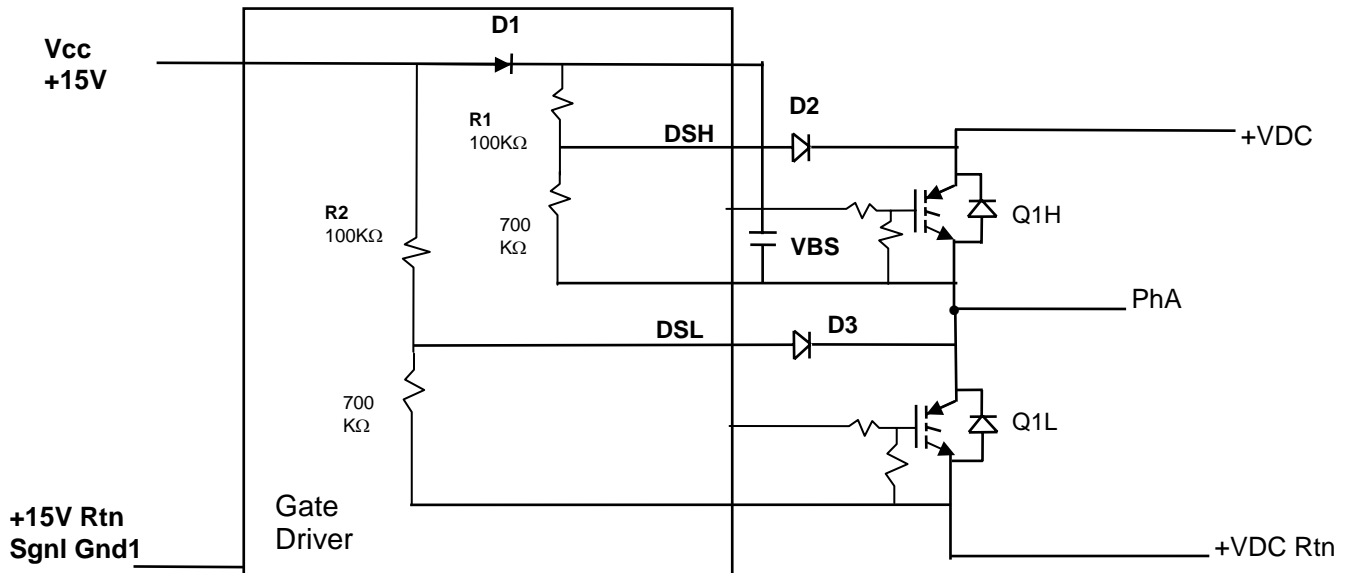
Figure 8.   Charging Path from 15V Supply to DC Bus when DC Bus is off

- Each IGBT is protected against desaturation.
- D2 is the desaturation sense diode for the high-side IGBT
- D3 is the desaturation sense diode for the low-side IGBT
- When the DC bus voltage is not applied or below 15V, there is a charging path from the 15V supply to the DC bus through D2 and D3 and the corresponding pull up 100K Ohm resistor. The charging current is 0.15mA per IGBT. Total charging current is about 1.5mA.
- **Do not apply PWM signal if the DC bus voltage is below 20V.**

c- Active Bias For Desaturation Detection Circuit:

The desaturation detection is done by diode D2 for the high side IGBT Q1H, and by diode D3 for the low side IGBT Q1L. The internal detection circuit, input DSH for the high-side and input DSL for the low-side, is biased by the local supply voltage VCC for the low side and VBS for the high side. When the IGBT is on the corresponding detection diode is on. The current flowing through the diode is determined by the internal pull resistor, R1 for the high side and R2 for the low side. To minimize the current drain from VCC and VBS, R1 and R2 are set to be 100KΩ. Lower value of R1 will overload the bootstrap circuit and reduce the bootstrap capacitor holding time.

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To increase the circuit noise immunity, an active bias circuit is used to lower R1 and R2 when the corresponding IGBT is off by monitoring the input voltage at both DSH, DSL inputs. If the inputs at DSH drops below 7V the active bias is disabled. The active bias circuits result in reducing R1 or R2 to about 110 Ω when the corresponding input is above 8V, as shown in Fig. 9. This active circuit results in higher noise immunity.
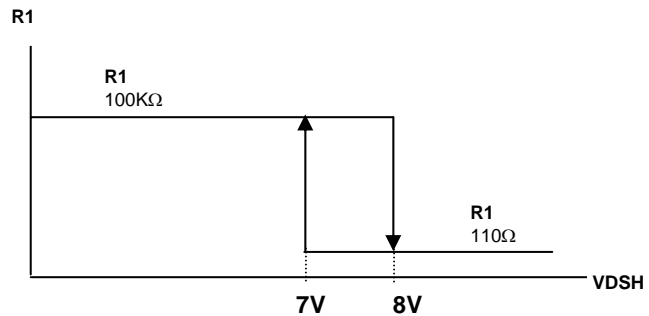

Figure 9.   Active Bias for DSH and DSL Internal Inputs

d- Limitation With Trapezoidal Motor Drive

In trapezoidal motor drives, two phases are conducting while the third phase is off at any time. In Fig. 10 shows the voltage waveform across one phase, during intervals t1 and t2, the IGBT is off while the active bias circuit is above 8V, and below 15V. This results in activating the active pull up circuit and reducing the corresponding R1 or R2 down to about 110 Ω. A high current will flow from VCC or VBS through R2 or R1 and the motor winding during intervals t1, and t2. This results in draining the bootstrap capacitor voltage quickly.

- **Contact the factory for adjustments to satisfy trapezoidal motor drive applications using this module. The adjustment will disable the internal pull up circuit.**
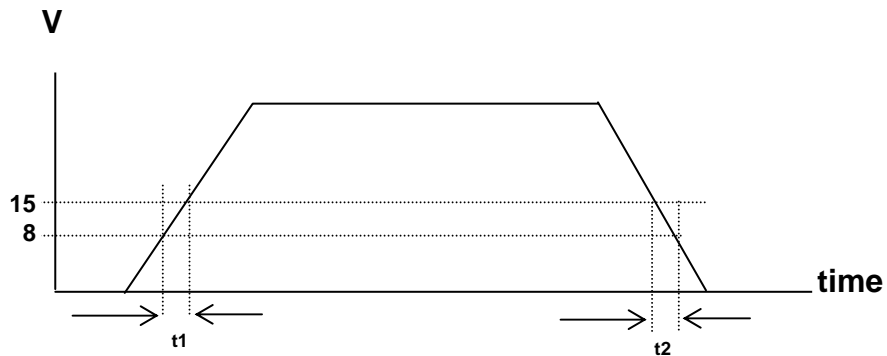
Figure 10.   Active Bias for DSH and DSL Internal Inputs

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