

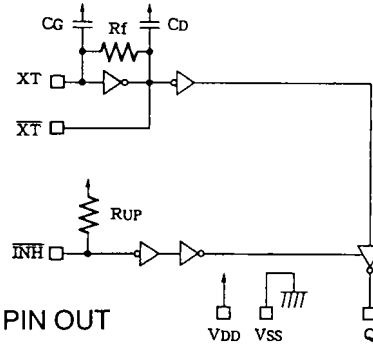
■ OVERVIEW

The SM5613 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and an output buffer with low current consumption. There are many kinds of type-capacitor for oscillation on chip or not, output level-TTL or CMOS, output drivability - 10TTL or 10LSTTL. (Refer to the SERIES TABLE).

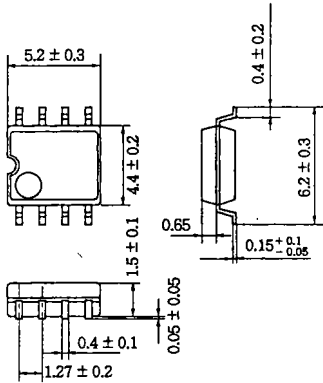
■ FEATURES

- Operating voltage (4.5 ~ 5.5V)
- Built-in feed back resistance of oscillating circuit
- 3-state function
- Available up to 50MHz
- Low current consumption
- Chip form, 8-pin SOP
- Molybdenum gate C-MOS
- For third overtone wave use

■ BLOCK DIAGRAM



■ PACKAGE DIMENSION (UNIT: mm)



■ PIN COORDINATES

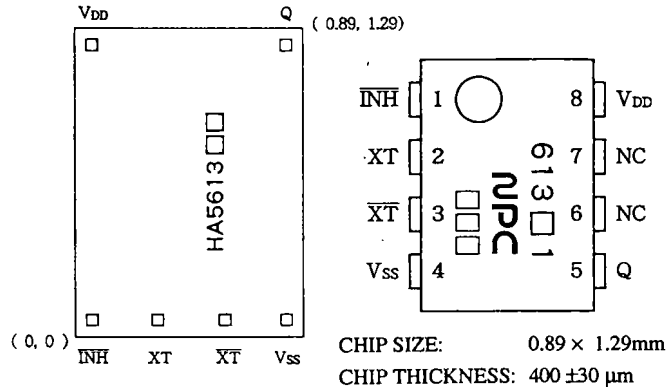
UNIT:  $\mu\text{m}$

NAME	X	Y
INH	145	140
XT	345	140
XT	545	140
V <sub>SS</sub>	745	140
Q	745	1150
V <sub>DD</sub>	145	1155

■ PIN OUT

• 8 PIN SOP

(TOP VIEW)



■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
XT	Output terminal for oscillating
INH	"L"; High impedance On-chip pull-up resistance
V <sub>DD</sub>	Power supply
V <sub>SS</sub>	Ground
Q	Output ( $f_o$ )

$f_o$ : Oscillating frequency

## ■ ABSOLUTE MAXIMUM RATING (V<sub>SS</sub>=0V)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V <sub>DD</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Storage temperature	T <sub>STG1</sub>	-65 to +150	°C
	T <sub>STG2</sub>	-40 to +125	
Output current	I <sub>OUT</sub>	H series 10	mA
		N, K series 25	
* Power dissipation	P <sub>W</sub>	200	mW
* Soldering temperature	T <sub>SLD</sub>	255	°C
* Soldering time	t <sub>SLD</sub>	10	S

Note: \* mark is useful at SOP package.

## ■ RECOMMENDED OPERATIONAL CONDITIONS (V<sub>SS</sub>=0V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V <sub>DD</sub>	4.0	5.0	6.0	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>	-40		+85	°C

## ■ ELECTRICAL CHARACTERISTICS

### 1. N series

(V<sub>SS</sub>=0V, T<sub>a</sub>=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
H-level output voltage	V <sub>OH</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OH</sub> =16.0mA	3.9	4.2	V
			V <sub>DD</sub> =4.0V, I <sub>OH</sub> =14.4mA	3.4	3.7	
L-level output voltage	V <sub>OL</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OL</sub> =16.0mA		0.3	V
			V <sub>DD</sub> =4.0V, I <sub>OL</sub> =14.4mA		0.3	
Output leak current	I <sub>Z</sub>	Q pin, Fig. 1, INH="L", V <sub>DD</sub> =6.0V	V <sub>OH</sub> =V <sub>DD</sub>		10	μA
			V <sub>OL</sub> =V <sub>SS</sub>		10	
H-level input voltage	V <sub>IH</sub>	INH pin	V <sub>DD</sub> =5±0.5V	2.0		V
			V <sub>DD</sub> =5±1.0V	2.2		
L-level input voltage	V <sub>IL</sub>	INH pin	V <sub>DD</sub> =5±1.0V		0.8	V
Current consumption	I <sub>DD1</sub>	Load circuit 1, Fig. 2, INH=OPEN, CL=15pF	V <sub>DD</sub> =5V, T <sub>a</sub> =25°C		25	mA
			V <sub>DD</sub> =5.5V		40	
	V <sub>DD</sub> =6.0V			45		
	V <sub>DD</sub> =5V, T <sub>a</sub> =25°C			35		
I <sub>DD2</sub>	Load circuit 1, Fig. 2, INH=OPEN, CL=50pF	V <sub>DD</sub> =5.5V		38	50	
		V <sub>DD</sub> =5.5V		50		
INH pin pull-up resistance	R <sub>UP</sub>	Fig. 3		50	250	kΩ
Feedback resistance	R <sub>f</sub>	Fig. 4	V <sub>DD</sub> =5±0.5V	1.0	5.0	MΩ
			V <sub>DD</sub> =5±1.0V	0.9	5.5	
Internal capacitor	C <sub>G</sub>	Design value		8.5	12	pF
	C <sub>D</sub>			12	17	

## 2. K series

(V<sub>SS</sub>=0V, T<sub>a</sub>=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
H-level output voltage	V <sub>OH</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OH</sub> =16.0mA	3.9	4.2	V	
			V <sub>DD</sub> =4.0V, I <sub>OH</sub> =14.4mA	3.4	3.7		
L-level output voltage	V <sub>OL</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OL</sub> =16.0mA		0.3	0.4	V
			V <sub>DD</sub> =4.0V, I <sub>OL</sub> =14.4mA		0.3	0.4	
Output leak current	I <sub>Z</sub>	Q pin, Fig. 1, INH="L", V <sub>DD</sub> =6.0V	V <sub>OH</sub> =V <sub>DD</sub>			10	μA
			V <sub>OL</sub> =V <sub>SS</sub>				
H-level input voltage	V <sub>IH</sub>	INH pin	V <sub>DD</sub> =5±0.5V	2.0			V
			V <sub>DD</sub> =5±1.0V	2.2			
L-level input voltage	V <sub>IL</sub>	INH pin	V <sub>DD</sub> =5±1.0V			0.8	V
Current consumption	I <sub>DDI</sub>	Load circuit 1, Fig. 2, INH=OPEN, CL=15pF	V <sub>DD</sub> =5V, T <sub>a</sub> =25°C		25	28	mA
			V <sub>DD</sub> =5.5V			40	
			V <sub>DD</sub> =6.0V			45	
INH pin pull-up resistance	R <sub>UP</sub>	Fig. 3		50		250	kΩ
Feedback resistance	R <sub>f</sub>	Fig. 4	V <sub>DD</sub> =5±0.5V	1.0		5.0	MΩ
			V <sub>DD</sub> =5±1.0V	0.9		5.5	
Internal capacitor	C <sub>G</sub>	Design value		8.5	12	15.5	pF
	C <sub>D</sub>			12	17	22	

## 3. H series

(V<sub>SS</sub>=0V, T<sub>a</sub>=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
H-level output voltage	V <sub>OH</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OH</sub> =4.0mA	3.9	4.2	V	
			V <sub>DD</sub> =4.0V, I <sub>OH</sub> =3.6mA	3.4	3.7		
L-level output voltage	V <sub>OL</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OL</sub> =4.0mA		0.3	0.5	V
			V <sub>DD</sub> =4.0V, I <sub>OL</sub> =3.6mA		0.3	0.5	
Output leak current	I <sub>Z</sub>	Q pin, Fig. 1, INH="L", V <sub>DD</sub> =6.0V	V <sub>OH</sub> =V <sub>DD</sub>			10	μA
			V <sub>OL</sub> =V <sub>SS</sub>				
H-level input voltage	V <sub>IH</sub>	INH pin	V <sub>DD</sub> =5±0.5V	2.0			V
			V <sub>DD</sub> =5±1.0V	2.2			
L-level input voltage	V <sub>IL</sub>	INH pin	V <sub>DD</sub> =5±1.0V			0.8	V
Current consumption	I <sub>DDI</sub>	Load circuit 1, Fig. 2, INH=OPEN, CL=15pF	V <sub>DD</sub> =5V, T <sub>a</sub> =25°C		20	25	mA
			V <sub>DD</sub> =5.5V			35	
			V <sub>DD</sub> =6.0V			40	
INH pin pull-up resistance	R <sub>UP</sub>	Fig. 3		50		250	kΩ
Feedback resistance	R <sub>f</sub>	Fig. 4	V <sub>DD</sub> =5±0.5V	1.0		5.0	MΩ
			V <sub>DD</sub> =5±1.0V	0.9		5.5	
Internal capacitor	C <sub>G</sub>	Design value		8.5	12	15.5	pF
	C <sub>D</sub>			12	17	22	

## ■ SWITCHING CHARACTERISTICS

### 1. N series

$V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$  unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	$T_{r1}$	Load circuit 1, Fig. 2 0.1V <sub>DD</sub> to 0.9V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	2.0	4.0	ns	
				V <sub>DD</sub> =5±1.0V				4.6
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	4.0	8.0			
			V <sub>DD</sub> =5±1.0V			9.5		
Output fall time	$T_{f1}$	Load circuit 1, Fig. 2 0.9V <sub>DD</sub> to 0.1V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	2.0		4.0	ns
				V <sub>DD</sub> =5±1.0V		4.6		
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	4.0	8.0			
			V <sub>DD</sub> =5±1.0V			9.5		
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C <sub>L</sub> =50pF, T <sub>a</sub> =25°C, V <sub>DD</sub> =5.0V			45			55
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, T <sub>a</sub> =25°C, V <sub>DD</sub> =5±1.0V, Load C <sub>L</sub> ≤50pF					100	ns
Output enable delay time	T <sub>PZL</sub>						100	
Maximum operating frequency	f <sub>MAX1</sub>	Load circuit 1, Fig. 2	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±1.0V	50			MHz
	f <sub>MAX2</sub>		C <sub>L</sub> =50pF	V <sub>DD</sub> =5±0.5V	50			
Minimum operating frequency	f <sub>MIN</sub>	Load circuit 1, Fig. 2, C <sub>L</sub> =50pF, V <sub>DD</sub> =5±1.0V					30	MHz

### 2. K series

$V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$  unless otherwise noted.

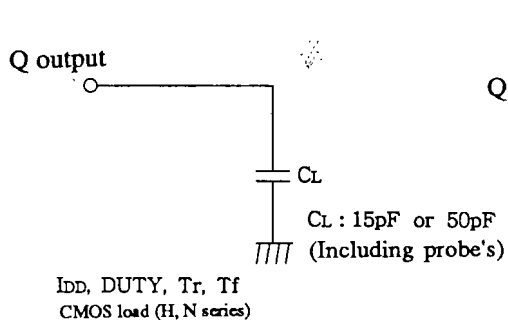
ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	$T_{r1}$	Load circuit 2, Fig. 2 0.4V <sub>DD</sub> to 2.4V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	1.5	3.0	ns	
				V <sub>DD</sub> =5±1.0V				3.5
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	3.0	6.0			
			V <sub>DD</sub> =5±1.0V			7.0		
Output fall time	$T_{f1}$	Load circuit 2, Fig. 2 2.4V <sub>DD</sub> to 0.4V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	1.5		3.0	ns
				V <sub>DD</sub> =5±1.0V		3.5		
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	3.0	6.0			
			V <sub>DD</sub> =5±1.0V			7.0		
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C <sub>L</sub> =15pF, T <sub>a</sub> =25°C, V <sub>DD</sub> =5.0V			45			55
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, T <sub>a</sub> =25°C, V <sub>DD</sub> =5±1.0V, Load C <sub>L</sub> ≤50pF					100	ns
Output enable delay time	T <sub>PZL</sub>						100	
Maximum operating frequency	f <sub>MAX</sub>	Load circuit 2, Fig. 2, V <sub>DD</sub> =5±1.0V			50			MHz
Minimum operating frequency	f <sub>MIN</sub>	Load circuit 2, Fig. 2, V <sub>DD</sub> =5±1.0V					30	MHz

### 3. H series

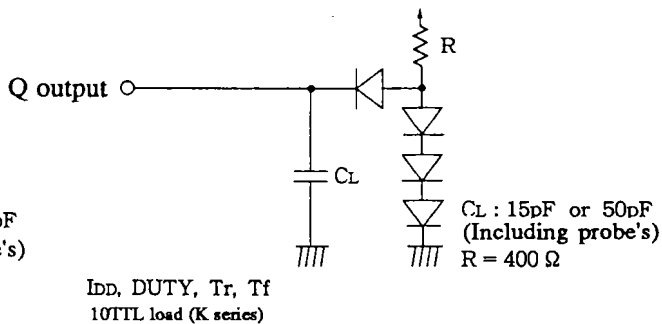
$V_{SS} = 0V$ ,  $T_a = -40$  to  $+85^\circ C$  unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS			UNIT
					MIN	TYP	MAX	
Output rise time	$T_{r1}$	Load circuit 1, Fig. 2 0.1V <sub>DD</sub> to 0.9V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	5.0	10	ns	
				V <sub>DD</sub> =5±1.0V				12
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	13	26			
			V <sub>DD</sub> =5±1.0V			30		
Output fall time	$T_{f1}$	Load circuit 1, Fig. 2 0.9V <sub>DD</sub> to 0.1V <sub>DD</sub>	C <sub>L</sub> =15pF	V <sub>DD</sub> =5±0.5V	5.0		10	ns
				V <sub>DD</sub> =5±1.0V		12		
	C <sub>L</sub> =50pF		V <sub>DD</sub> =5±0.5V	13	26			
			V <sub>DD</sub> =5±1.0V			30		
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C <sub>L</sub> =15pF, T <sub>a</sub> =25°C, V <sub>DD</sub> =5.0V			45			55
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, T <sub>a</sub> =25°C, V <sub>DD</sub> =5±1.0V, Load C <sub>L</sub> ≤50pF					100	ns
Output enable delay time	T <sub>PZL</sub>						100	
Minimum operating frequency	f <sub>MAX</sub>	Load circuit 1, Fig. 2, V <sub>DD</sub> =5±1.0V			50			MHz
Maximum operating frequency	f <sub>MIN</sub>	Load circuit 1, Fig. 2, V <sub>DD</sub> =5±1.0V					30	MHz

■ LOAD CIRCUIT



Load Circuit 1 (H, N versions)



Load Circuit 2 (K versions)

■ TEST CIRCUIT

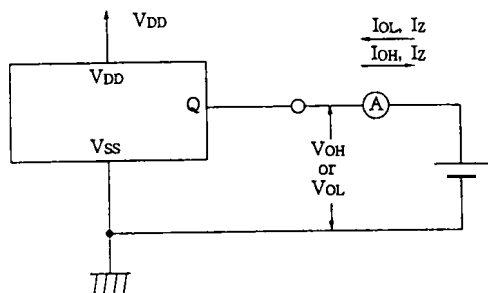


Fig. 1

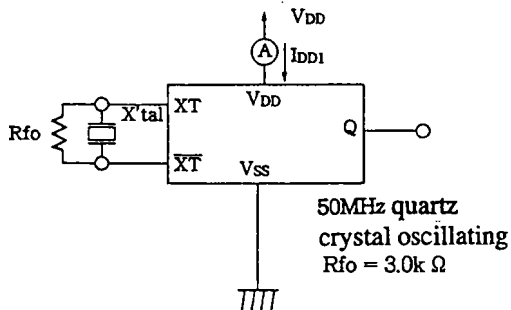


Fig. 2

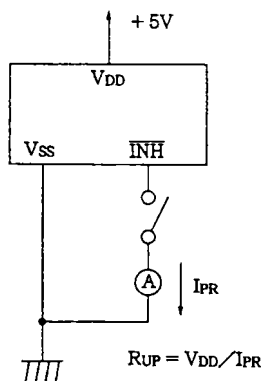


Fig. 3

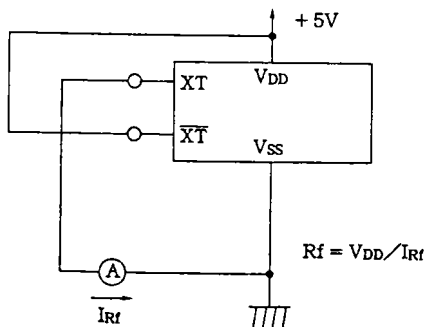
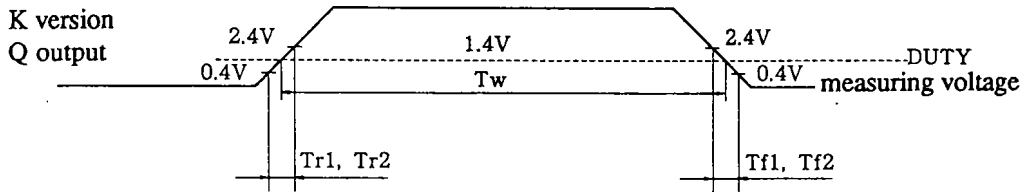
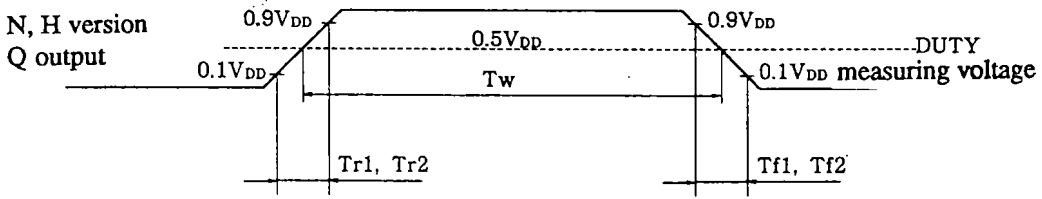
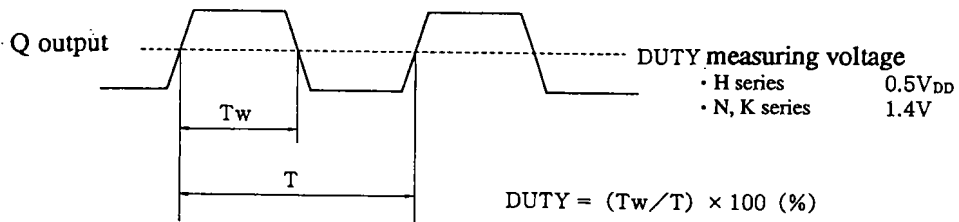


Fig. 4

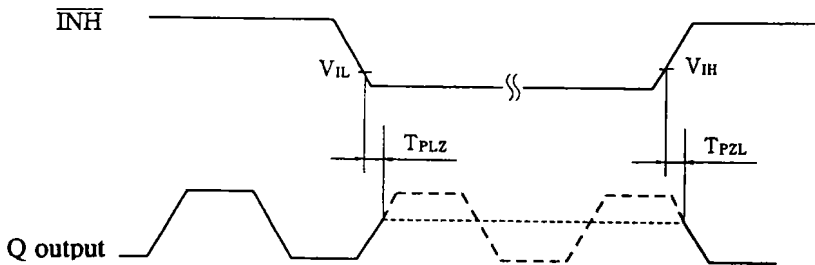
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME



## ■ SERIES TABLE

Versions	Output frequency	Built-in capacity	Output current (mA)	Fan out (TTL)	Input level	Output level	Delivery Form
SM5613N1	$f_o$	○	16	10	TTL	CMOS	Chip
N1S	$f_o$	○	16	10	TTL	CMOS	8Pin SOP
K1	$f_o$	○	16	10	TTL	TTL	Chip
K1S	$f_o$	○	16	10	TTL	TTL	8Pin SOP
H1	$f_o$	○	4	10LS	TTL	CMOS	Chip
H1S	$f_o$	○	4	10LS	TTL	CMOS	8Pin SOP

## ■ FUNCTION

CONTROL	OUTPUT TERMINAL
INH	Q
H (OPEN)	Output ( $f_o$ )
L	High impedance

$f_o$  : Oscillating frequency