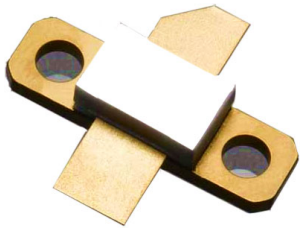
Preliminary

SLD-3091FZ

RoHS Compliant & Green Package

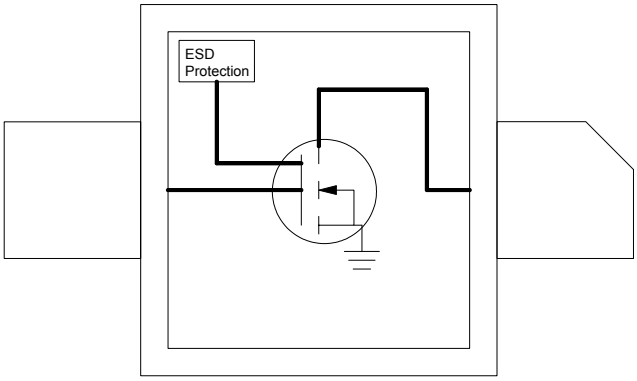
30 Watt Discrete LDMOS FET in Ceramic Flanged Package



Product Description

Sirenza Microdevices' **SLD-3091FZ** is a robust 30 Watt high performance LDMOS transistor designed for operation from 10 to 2200MHz. It is an excellent solution for applications requiring high linearity and efficiency at a low cost. The SLD-3091FZ is typically used in power amplifiers, repeaters, and radio amplifier applications. The power transistor is fabricated using Sirenza's high performance XeMOS II™ process.

Functional Schematic Diagram



Case Flange = Ground

Product Features

- **30 Watt Output P_{1dB}**
- **Single Polarity Supply Voltage**
- **High Gain: 18 dB at 915 MHz**
- **High Efficiency: 45% at 30W CW**
- **XeMOS II LDMOS**
- **Integrated ESD Protection, 1B**

Applications

- **Base Station PA driver**
- **Repeaters**
- **Radio Amplifier**
- **Military Communication**
- **GSM, CDMA, RFID, Point-to-Point**

Key RF Specifications

Symbol	Parameter	Units	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	10	-	2200
Gain	30 Watt CW, 915 MHz	dB		19	
Efficiency	Drain Efficiency at 30 Watt CW, 915 MHz	%		45	
IRL	Input Return Loss, 30 Watt Output Power, 915 MHz	dB		-15	
Linearity	3rd Order IMD at 30 Watt PEP (Two Tone), 915 MHz	dBc		-28	
	1dB Compression (P_{1dB}), 915 MHz	Watt		35	
R_{TH}	Thermal Resistance (Junction-to-Case)	ºC/W		2.4	
Test Conditions	**V_{DS} = 28.0V, I_{DQ} = 300mA, T_{Flange} = 25ºC**				

Key DC Parameters

Symbol	Parameter	Unit	Min	Typ.	Max
g_m	Forward Transconductance @ 425mA I_{DS}	mA / V		1650	
V_{GS}Threshold	I_{DS}=3mA	Volt		3.3	
V_{DS} Breakdown	1mA I_{DS} current	Volt		65	
C_{iss}	Input Capacitance (Gate to Source) V_{GS}=0V, V_{DS}=28V	pF		66	
C_{rss}	Reverse Capacitance (Gate to Drain) V_{GS}=0V, V_{DS}=28V	pF		1.4	
C_{oss}	Output Capacitance (Drain to Source) V_{GS}=0V, V_{DS}=28V	pF		30	
R_{DSon}	Drain to Source Resistance, V_{GS}=10V, V_{DS}=250mV	Ω		0.2	

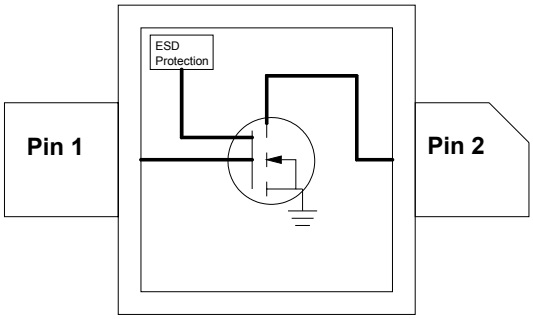
Quality Specifications

Parameter	Description	Rating
ESD Rating	Human Body Model	1B

Pin Description

Pin #	Function	Description
1	Gate	Transistor RF input and gate bias voltage. The gate bias voltage must be temperature compensated to maintain constant bias current over the operating temperature range. Care must be taken to protect against video transients that exceed the recommended maximum input power or voltage.
2	Drain	Transistor RF output and drain bias voltage. Typical voltage is 28V.
Flange	Source, Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

Pin Diagram



Case Flange = Ground

Note 1:
Gate voltage must be applied to the device concurrently or after application of drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to the transistor unless it is properly terminated on both input and output.

Note 2:
The required V_{GS} corresponding to a specific I_{DQ} will vary from device to device due to the normal die-to-die variation in threshold voltage with LDMOS transistors.

Note 3:
The threshold voltage (V_{GSTH}) of LDMOS transistors varies with device temperature. External temperature compensation may be required. See Sirenza application notes AN-067 LDMOS Bias Temperature Compensation.

Absolute Maximum Ratings

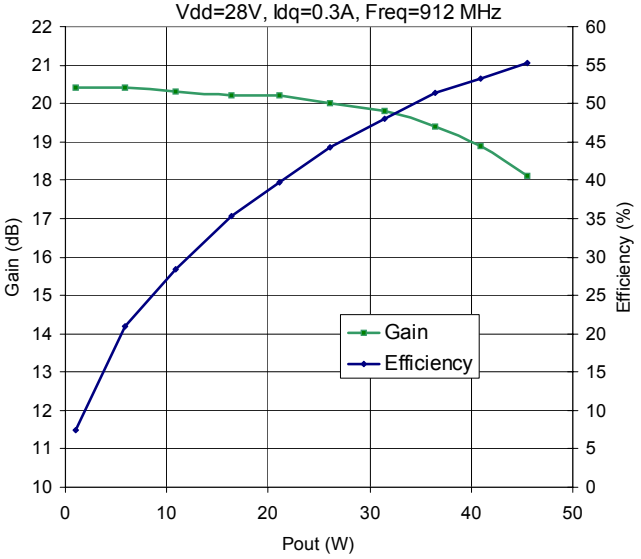
Parameters	Value	Unit
Drain Voltage (V_{DS})	35	V
Gate Voltage (V_{GS})	20	V
RF Input Power	+36	dBm
Load Impedance for Continuous Operation Without Damage	10:1	VSWR
Output Device Channel Temperature	+200	ºC
Lead Temperature During Solder Reflow	+270	ºC
Operating Temperature Range	-20 to +90	ºC
Storage Temperature Range	-40 to +100	ºC

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

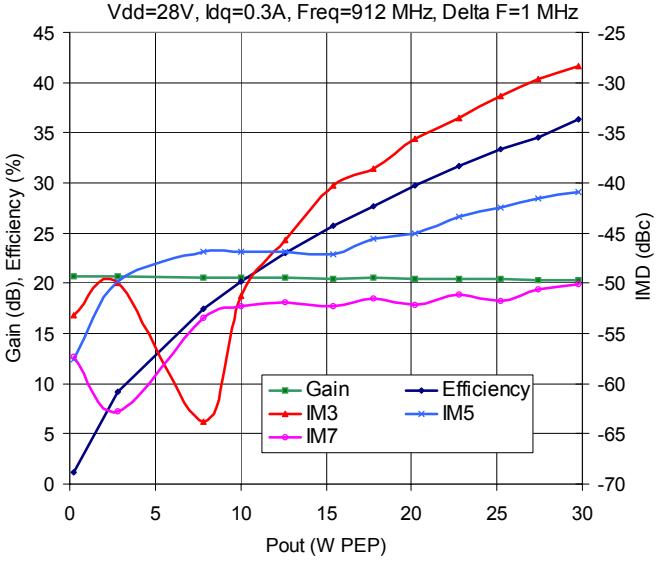
Caution: ESD Sensitive
Appropriate precaution in handling, packaging and testing devices must be observed.

Typical Performance Curves in 900 MHz Application Circuit

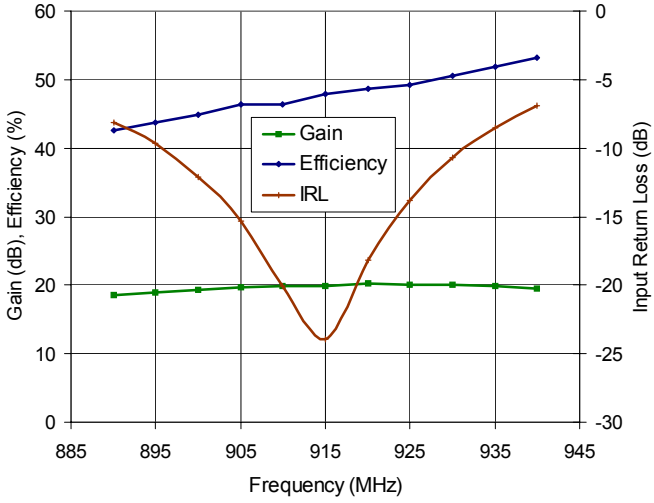
CW Gain, Efficiency vs Pout
Vdd=28V, Idq=0.3A, Freq=912 MHz



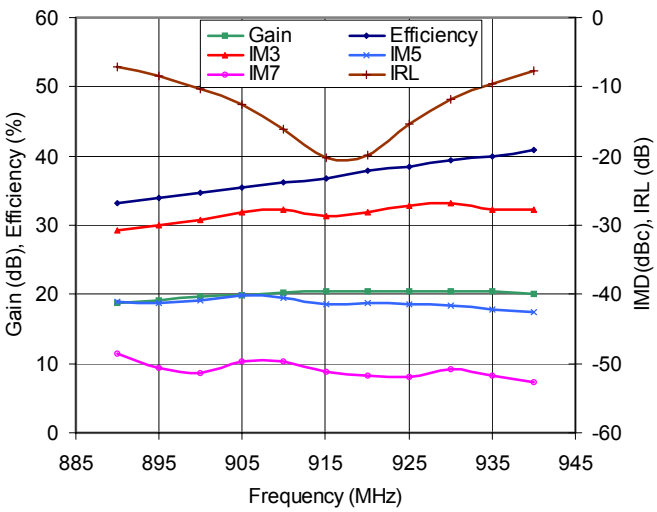
2 Tone Gain, Efficiency, Linearity vs Pout
Vdd=28V, Idq=0.3A, Freq=912 MHz, Delta F=1 MHz



CW Gain, Efficiency, IRL vs Frequency Vdd=28V, Idq=0.3A, Pout=30W

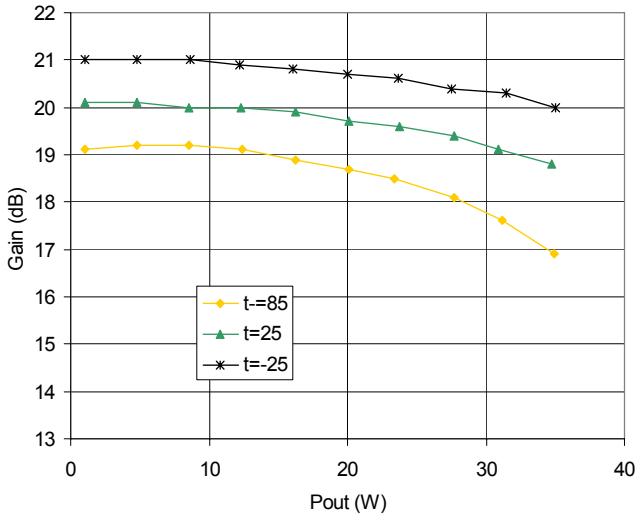


2 Tone Gain, Efficiency, Linearity and IRL vs Frequency
Vdd=28V, Idq=0.3A, Pout=30W PEP, Delta F=1 MHz

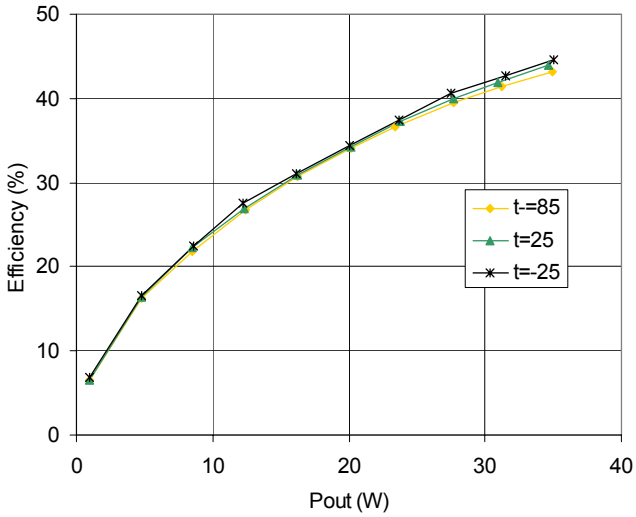


Typical Performance Curves in 900 MHz Application Circuit over Temperature

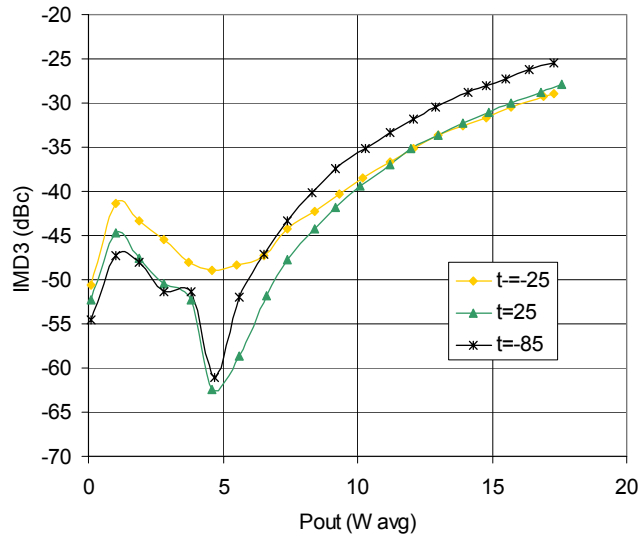
CW Gain vs Pout over Temperature
Vdd=28V, Idq=300mA, Freq=920 MHz



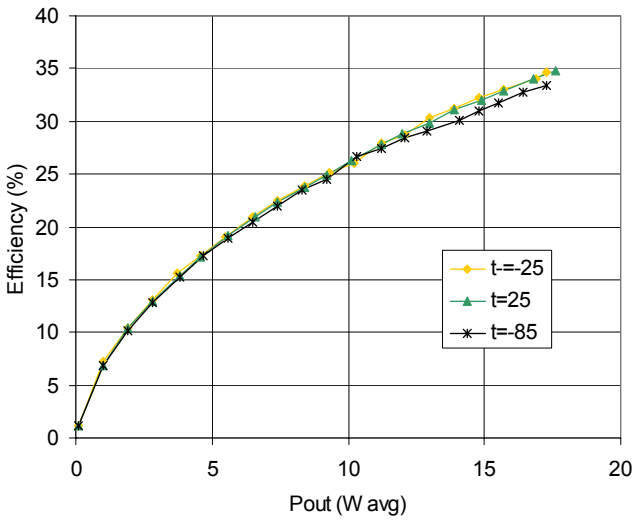
Efficiency vs Pout over Temperature
Vdd=28V, Idq=300mA, Freq=912 MHz



IMD3 vs Pout over Temperature
Vdd=28V, Idq=300mA, Freq=912 MHz



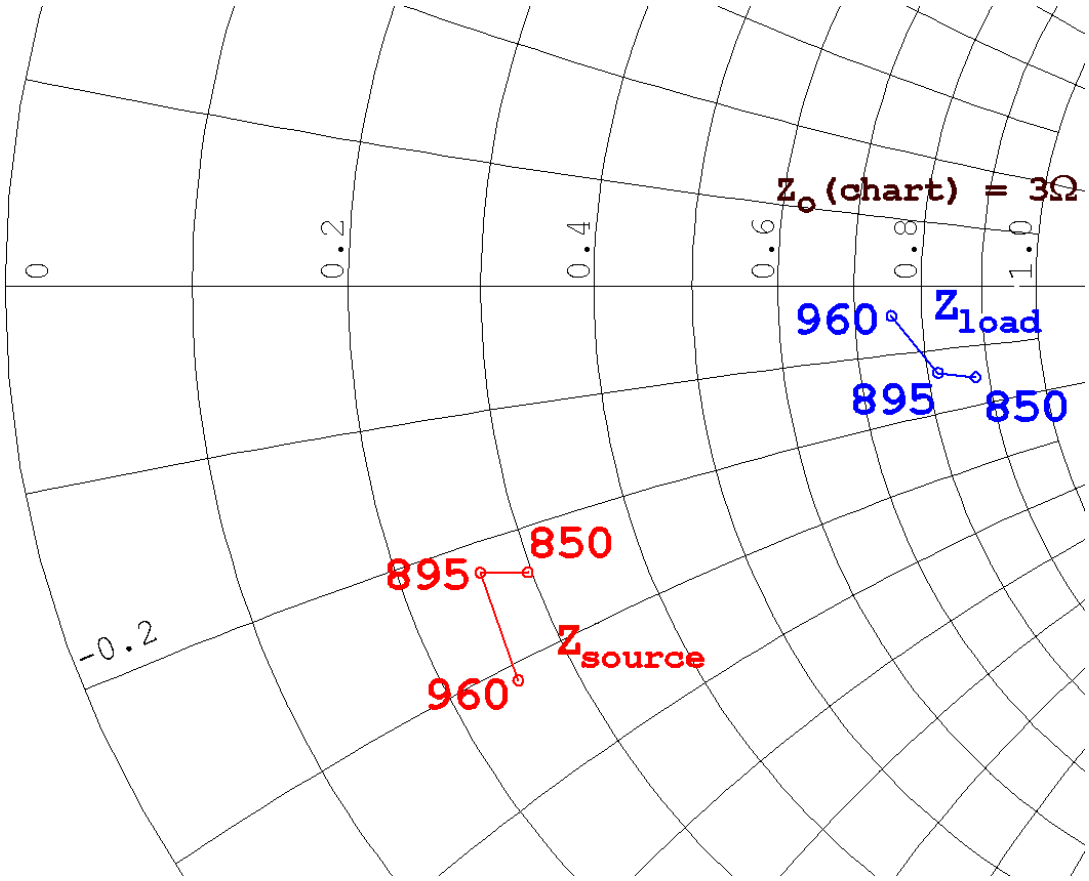
2 tone Efficiency vs Pout over Temperature
Vdd=28V, Idq=300mA, Freq=912 MHz

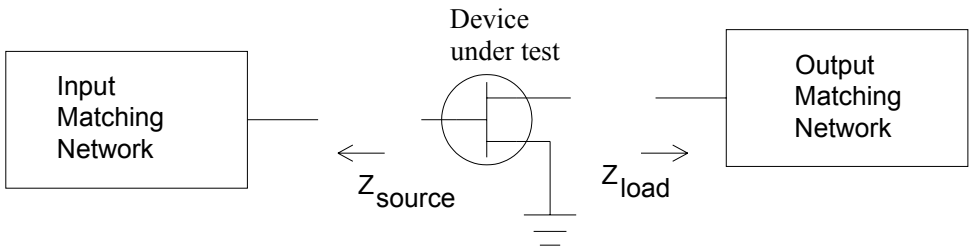


Impedance Data

Frequency (MHz)	Z_{source}	Z_{load}
850	0.9 - j 0.7	2.6 - j 0.5
895	0.8 - j 0.7	2.4 - j 0.4
960	0.7 - j 0.9	2.3 - j 0.1

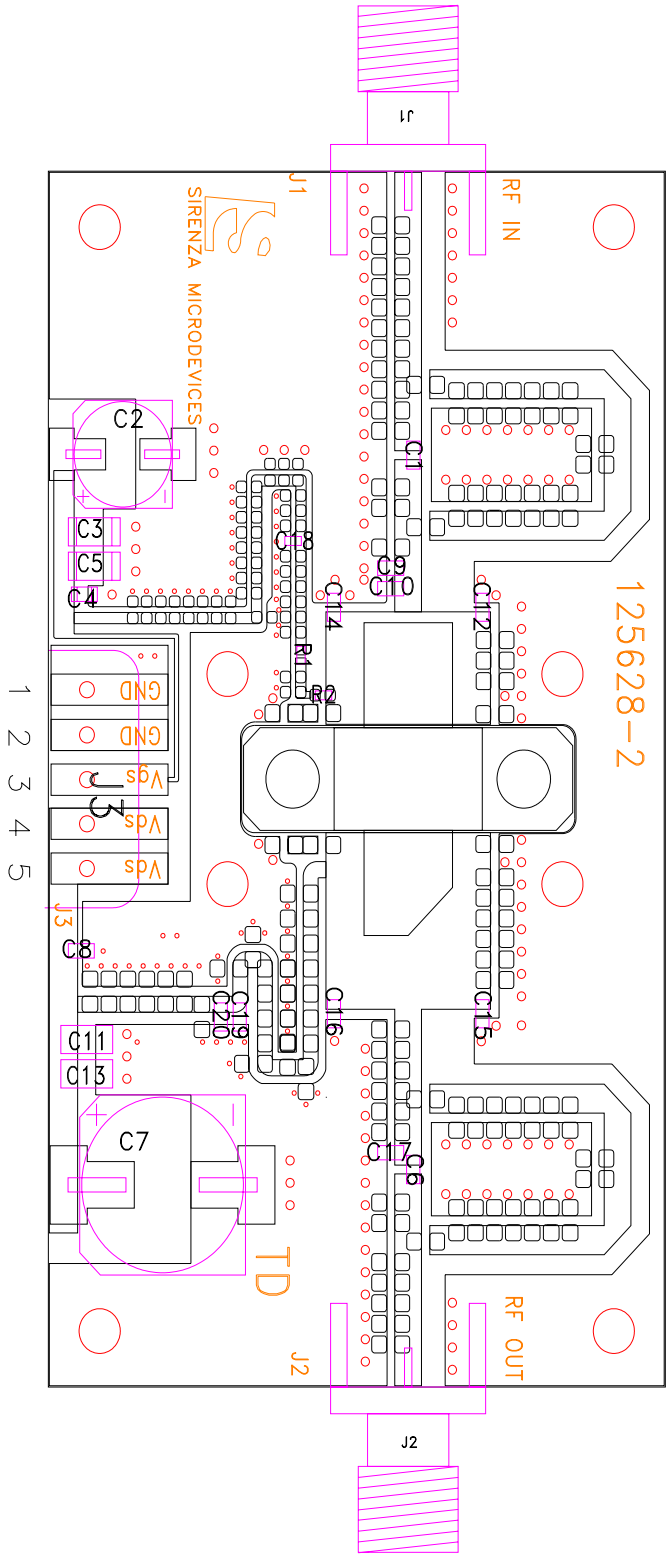
Impedances Referenced to Wirebond/PCB Interface.





Z_{source} and Z_{load} are the optimal impedances presented to the SLD-3091FZ when operating at 28V, Idq=300mA, Pout=30 W PEP

900 MHz Application Circuit



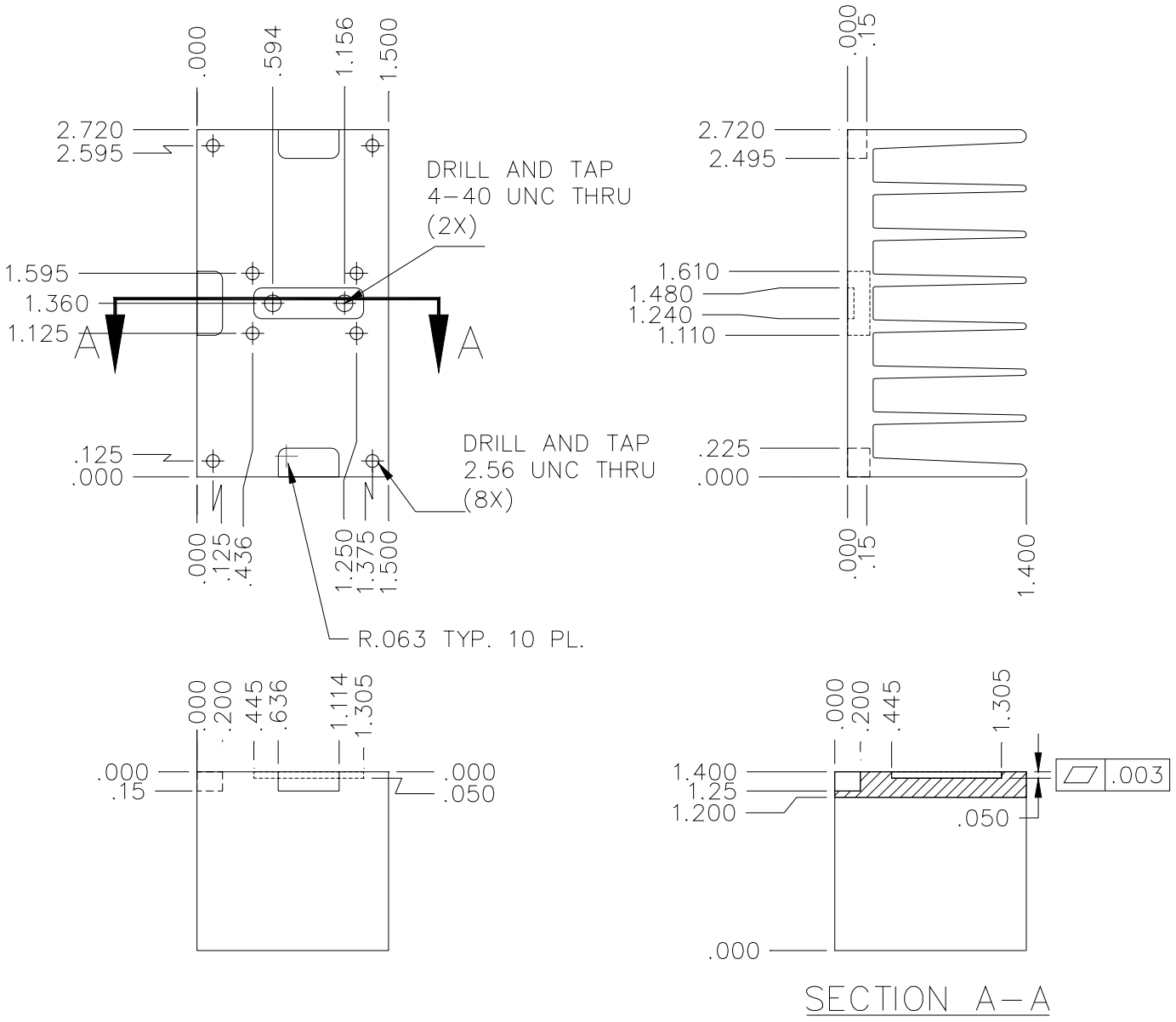
Pin Descriptions - 900 MHz Application Circuit

Connector	Pin #	Function	Description
J1	Coax	RF in	RF input to test fixture (50 Ohm system)
J2	Coax	RF out	RF output to test fixture (50 Ohm system)
J3	1	Gnd	DC ground for D package module. Also connected to RF ground.
J3	2	Gnd	DC ground for D package module. Also connected to RF ground.
J3	3	V_{GS}	Gate voltage for the SLD3091FZ. Nominally +4Vdc.
J3	4	V_{DS}	Drain voltage for the SLD3091FZ. Nominally +28Vdc.
J3	5	V_{DS}	Drain voltage for the SLD3091FZ. Nominally +28Vdc.

Bill of Materials - 900 MHz Application Circuit

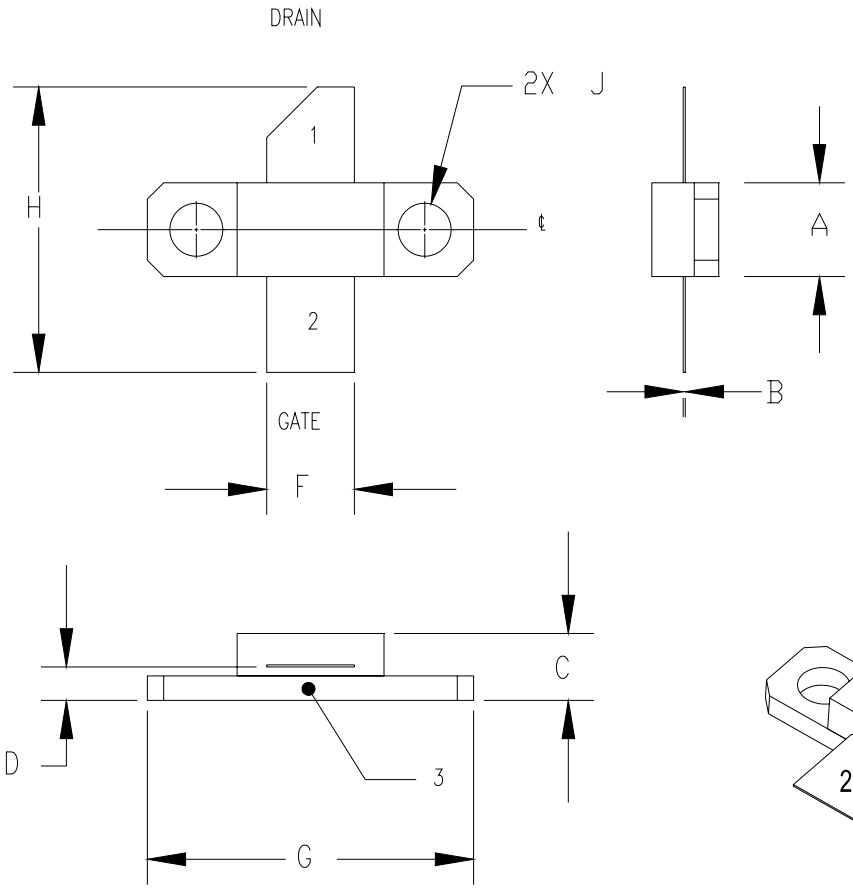
Component	Description	Manufacturer
PCB	Rogers 4350, ε_r=3.5 Thickness=30 mils	Rogers
J1, J2	Connector, SMA END 0.037"	Johnson
J3	MTA Post Header, 5 Pin, Rectangle, Polarized, Surface Mount	AMP
C2	Capacitor, Lytic 22F, 35V	Panasonic
C3, C11	Cap, 0.1μF, 100V, 10%, 1206	Johanson
C5, C13	Cap, 1000pF, 100V, 10%, 1206	Johanson
C7	Capacitor, Lytic 220uF, 50V	Panasonic
C1,C4,C6, C8,C19	CAP, 68PF,250V,5%,0603	ATC
C10,C12, C14	CAP, 12PF,250V,1%,0603	ATC
C15,C16	CAP, 10PF,250V,1%,0603	ATC
C17	CAP, 7.5 PF, 250V,0603	ATC
C18	CAP, 27PF,250V,5%,0603	ATC
C2	CAP, 0.22UF, 50V, CERAMIC, X7R, 1206,	Kemet
C9	CAP, 4.3 PF, 250V, 0603	ATC
R2	RES, 560, 1/16W, 5%, 0402	Panasonic
R1	RES, 0.0, 1/16W, 5%, 0402	Panasonic
Mounting Screws	4-40 X 0.250"	Various

900 MHz Application Circuit Heatsink



To receive Gerber files, DXF drawings, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com.

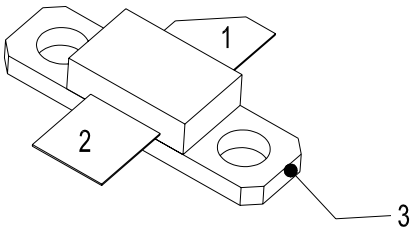
Package Outline



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.225	0.235	5.72	5.97
B	0.004	0.006	0.102	0.152
C	0.149	0.178	3.78	4.52
D	0.077	0.087	1.96	2.21
E	0.355	0.365	9.02	9.27
F	0.210	0.220	5.33	5.59
G	0.795	0.805	20.19	20.45
H	0.697	0.703	17.70	17.86
J	DIA 0.130		DIA 3.30	



PIN 1. DRAIN
PIN 2. GATE
PIN 3. SOURCE