



P-Channel 150-V (D-S) MOSFET

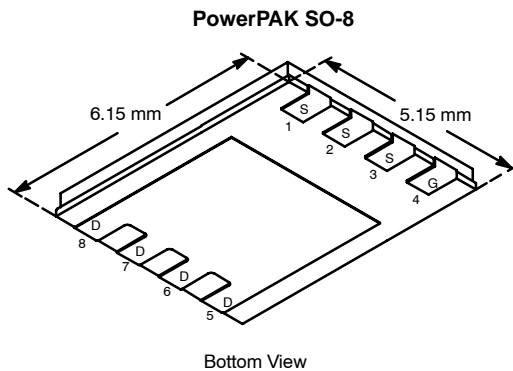
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-150	0.090 @ $V_{GS} = -10$ V	-5.2
	0.095 @ $V_{GS} = -6$ V	-5.0

FEATURES

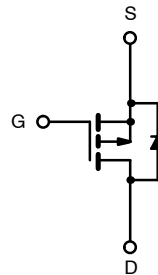
- TrenchFET® Power MOSFETS
- Ultra-Low On-Resistance Critical for Application
- Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_{θ} and Avalanche Tested

APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies



Ordering Information: Si7439DP-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-150		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-5.2	-3.0	A
		$T_A = 70^\circ\text{C}$	-4.1	-2.4	
Pulsed Drain Current	I_{DM}	-50			
Continuous Source Current (Diode Conduction) ^a	I_S	-4.2	-1.6		
Single Pulse Avalanche Current	I_{AS}	L = 0.1 mH	-40		mJ
Single Pulse Avalanche Energy			E_{AS}	80	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	18	23	$^\circ\text{C/W}$
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5		

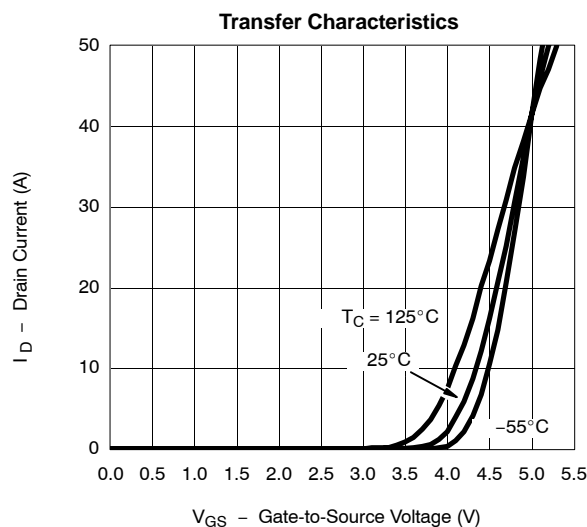
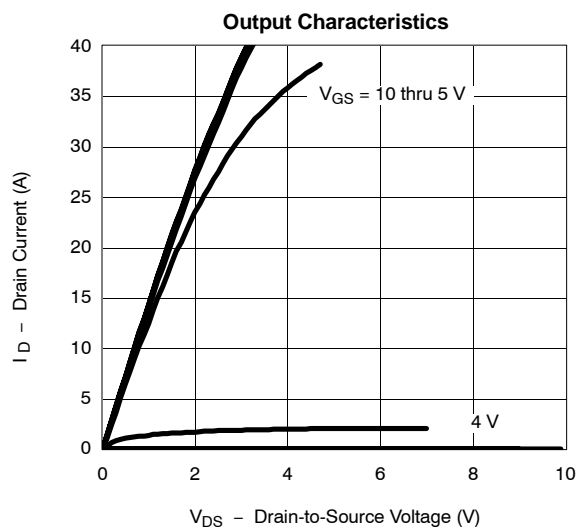
Notes

a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-2.0		-4.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -150 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -150 V, V _{GS} = 0 V, T _J = 70 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -10 V, V _{GS} = -10 V	-30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -5.2 A		0.073	0.090	Ω
		V _{GS} = -6 V, I _D = -5.0 A		0.077	0.095	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -5.2 A		19		S
Diode Forward Voltage ^a	V _{SD}	I _S = -4.2 A, V _{GS} = 0 V		-0.78	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -75 V, V _{GS} = -10 V, I _D = -5.2 A		88	135	nC
Gate-Source Charge	Q _{gs}		17.5			
Gate-Drain Charge	Q _{gd}		26.5			
Gate Resistance	R _g		1.5	3	4.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -75 V, R _L = 15.5 Ω I _D ≅ -4.8 A, V _{GEN} = -10 V, R _g = 6 Ω		25	40	ns
Rise Time	t _r		46	70		
Turn-Off Delay Time	t _{d(off)}		115	180		
Fall Time	t _f		64	100		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2.9 A, di/dt = 100 A/μs		100	150	

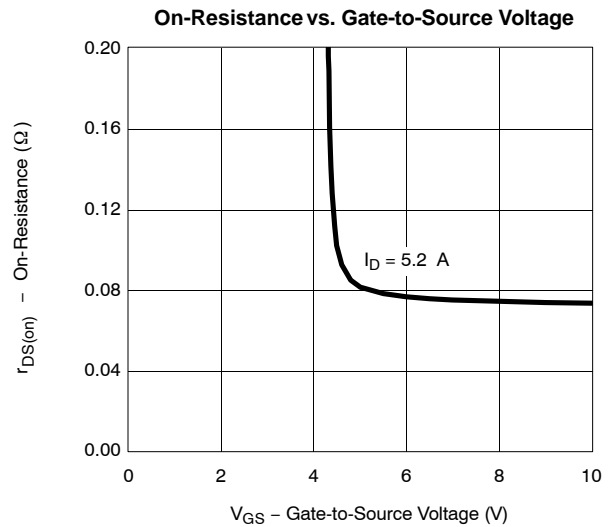
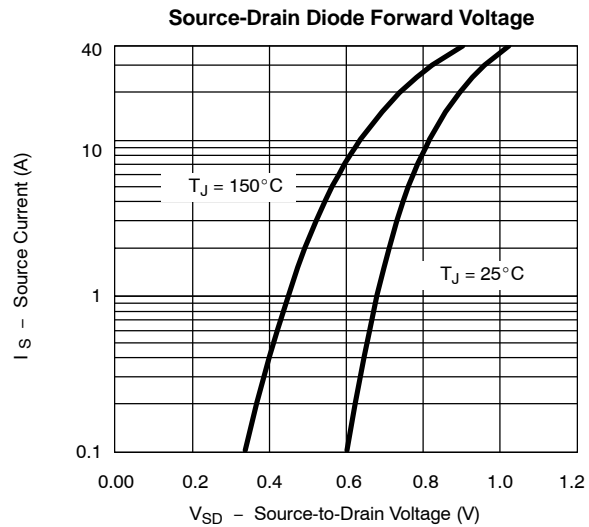
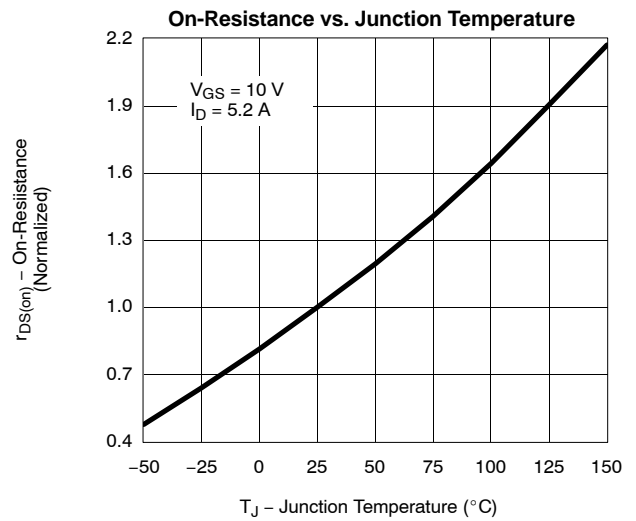
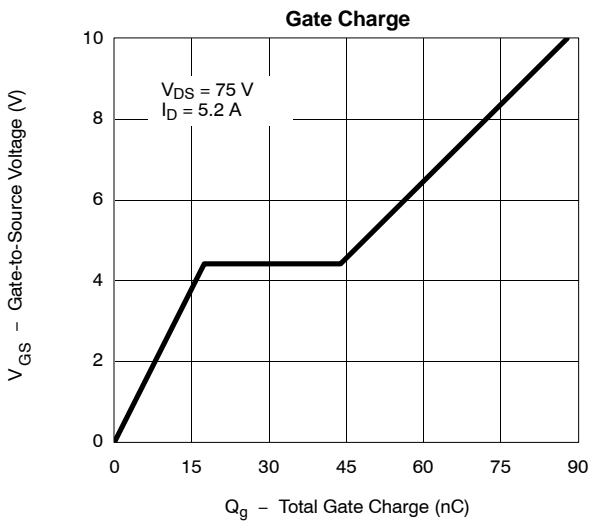
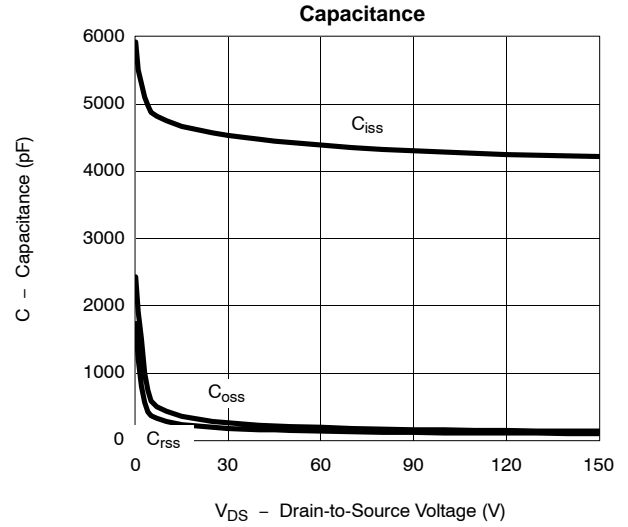
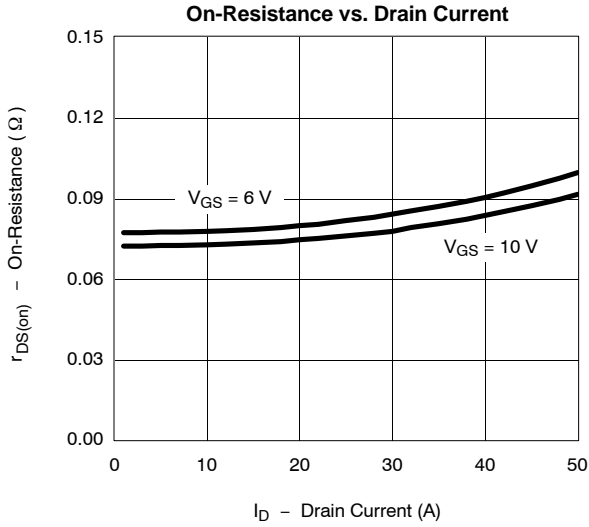
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

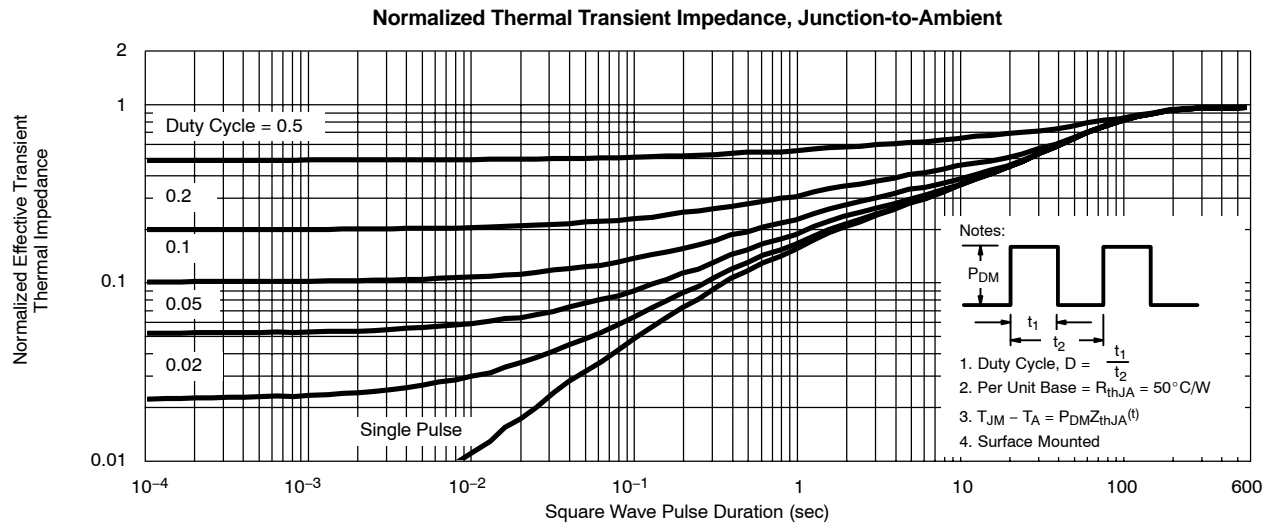
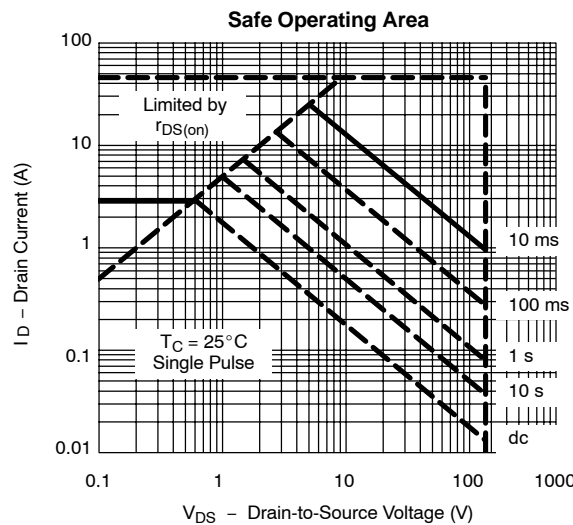
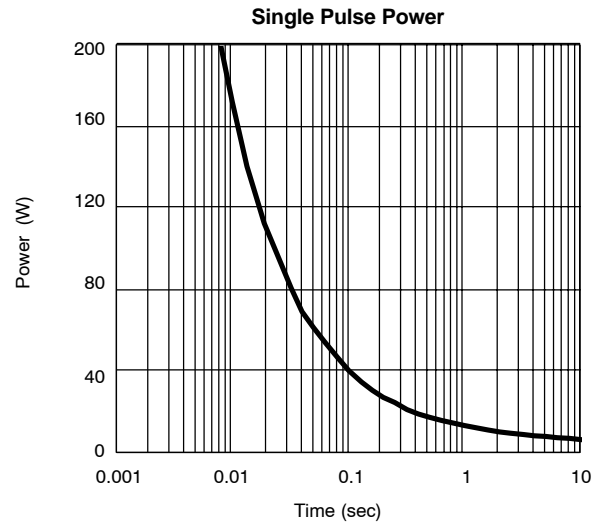
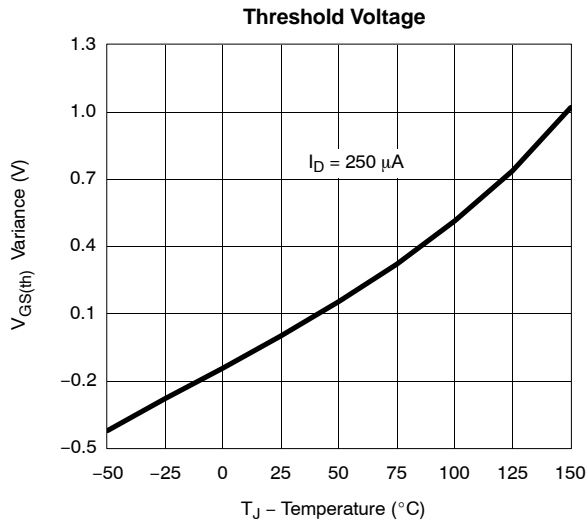
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