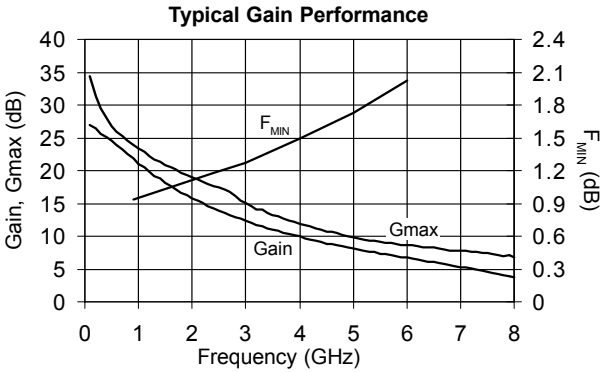
Preliminary

SGA-8343

Low Noise, High Gain SiGe HBT

Product Description

Stanford Microdevices' SGA-8343 is a high performance SiGe HBT amplifier designed for operation from DC to 6 GHz. This RF device uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process. The SGA-8343 is optimized for 3V operation but can be biased at 2V for low-voltage battery operated systems. The device is easily matched as Γ_{OPT} is very close to 50 ohms. This device provides high gain, low NF, and excellent linearity at a low cost.



Product Features

- **6 GHz Useful Bandwidth**
- **Low F_{MIN}: 0.9 dB @ 0.9 GHz, 1.1 dB @ 1.9 GHz**
- **High Gain (Gmax): 24 dB @ 0.9 GHz, 19 dB @ 1.9 GHz**
- **Easily Matched with $|\Gamma_{OPT}|$ = 0.17 @ 1.9 GHz**
- **OIP3 = +28.5 dBm, P1dB = +13 dBm**
- **Low Cost High Performance SiGe HBT**

Applications

- **LNA for Wireless Infrastructure**
- **Fixed Wireless Infrastructure**
- **Wireless Data**
- **Driver Stage for Low Power Applications**
- **Oscillators**

Symbol	Device Characteristics, T = 25ºC V_{CE}=3V, I_{CQ}=10mA (unless otherwise noted)		Units	Min.	Typ.	Max.
G_{MAX}	Maximum Available Gain $Z_S=Z_S^*$, $Z_L=Z_L^*$	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dB		23.9 19.3 17.7	
S_{21}	Insertion Gain $Z_S=Z_L=50\Omega$	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dB		21.8 16.3 14.3	
F_{min}	Minimum Noise Figure $Z_S=\Gamma_{OPT}$, $Z_L=Z_{LOPT}$	f = 0.9 GHz f = 1.9 GHz f = 2.4 GHz	dB		0.9 1.1 1.2	
P1dB	Output 1 dB compression point $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	V_{CE}=2V, I_{CQ}=20 mA V_{CE}=3V, I_{CQ}=20 mA	dBm		10.0 13.3	
OIP_3	Output Third Order Intercept Point $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	V_{CE}=2V, I_{CQ}=20 mA V_{CE}=3V, I_{CQ}=20 mA	dBm		24.0 28.5	
h_{FE}	DC Current Gain			120	180	300
BV_{CEO}	Collector - Emitter Breakdown Voltage		V	5.7	6.0	
Rth	Thermal Resistance (junction to lead)		ºC/W		200	

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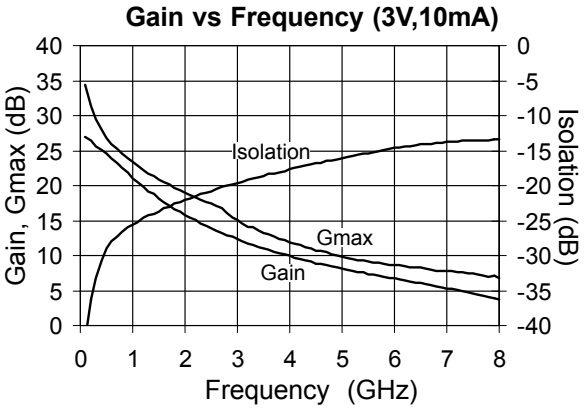
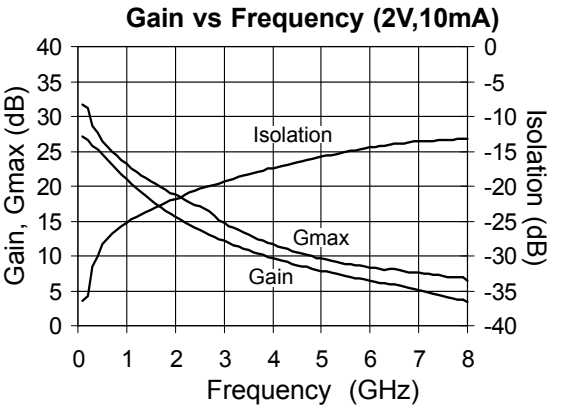
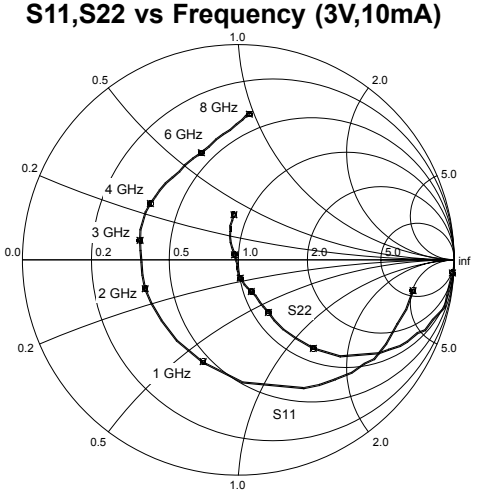
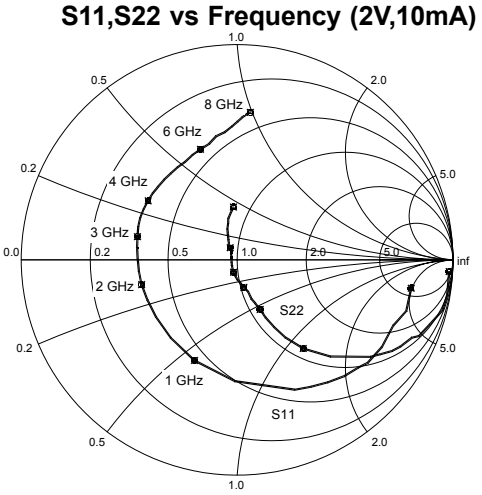
Typical Performance - Deembedded S-Parameters







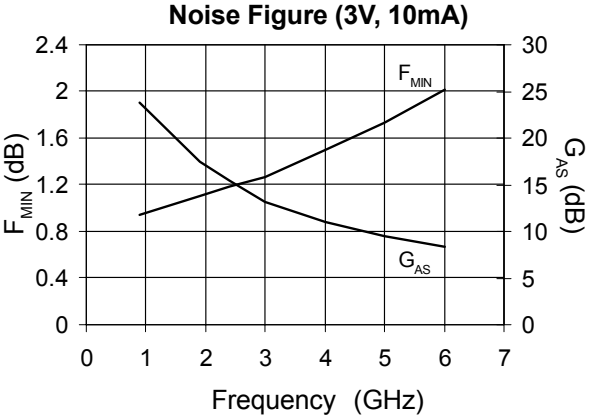


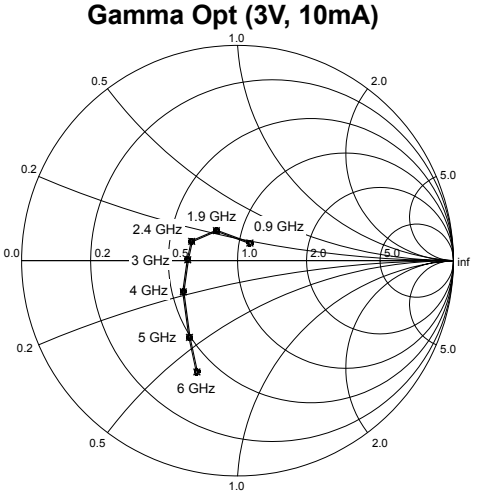
Note: S-parameters are de-embedded to the device leads with $Z_S=Z_L=50\Omega$. The data represents typical performace of the device. De-embedded s-parameters can be downloaded from our website (www.stanfordmicro.com).

Typical Performance - P1dB, OIP3, Gain

Freq (MHz)	V_{CE} (V)	I_{CQ} (mA)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	Z_{LOPT} Mag ∠ Ang
900	2	10	10.0	22.0	25.0	0.50 ∠ 143.3
		20	10.2	24.0	24.0	0.24 ∠ 16.6
	3	10	13.0	24.5	24.4	0.36 ∠ 16.2
		20	13.3	28.0	24.4	0.36 ∠ 16.2
1900	2	10	10.0	23.0	16.7	0.43 ∠ 91.2
		20	10.2	26.0	16.4	0.32 ∠ 24.1
	3	10	13.0	26.0	18.0	0.54 ∠ 15.2
		20	13.3	28.5	18.0	0.38 ∠ 14.0
2400	2	10	10.0	23.0	15.0	0.31 ∠ 45.0
		20	10.2	24.0	15.0	0.29 ∠ 33.3
	3	10	13.0	27.5	15.3	0.44 ∠ 9.2
		20	13.3	29.0	15.3	0.36 ∠ 13.3

Typical Performance - Noise Parameters





Noise Parameters - V_{CE}=3V, I_C=10mA

Freq (MHz)	F_{MIN} (dB)	Gamma Opt Mag ∠ Ang	r_n	G_{AS}(dB)	Gmax (dB)
0.9	0.94	0.10 ∠ 55	0.11	23.8	23.88
1.9	1.1	0.17 ∠ 125	0.10	17.5	19.33
2.4	1.18	0.23 ∠ 157	0.09	15.4	17.66
3	1.27	0.23 ∠ 179	0.09	13.2	15.01
4	1.5	0.29 ∠ -150	0.12	11.0	11.94
5	1.73	0.42 ∠ -122	0.18	9.5	9.84
6	2.02	0.55 ∠ -110	0.24	8.4	8.62

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Collector Current	I_C	72	mA
Base Current	I_B	1	mA
Collector - Emitter Voltage	V_{CEO}	5	V
Collector - Base Voltage	V_{CBO}	12	V
Emitter - Base Voltage	V_{EBO}	4.5	V
Operating Temperature	T_{OP}	-40 to +85	C
Storage Temperature Range	T_{stor}	-40 to +150	C
Power Dissipation	P_{DISS}	325	mW
Operating Junction Temperature	T_J	+150	C

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SGA-8343	7"	3000

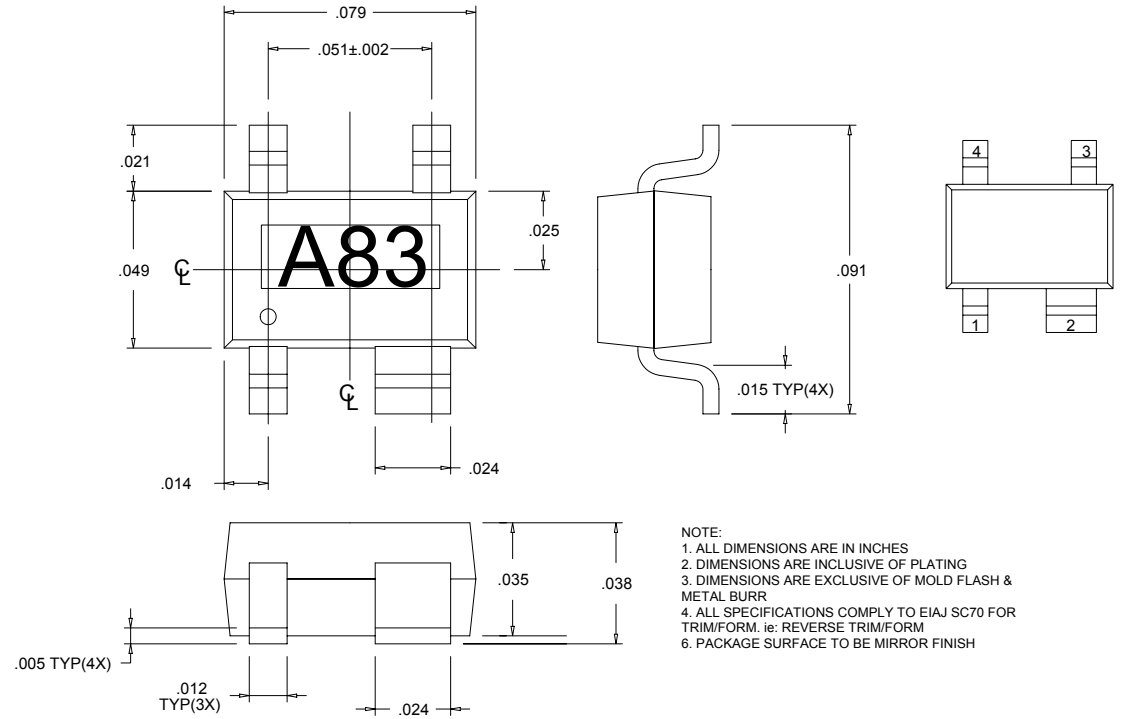
Part Symbolization

The part will be symbolized with an “A83” and a Pin 1 indicator on the top surface of the package.

Pin Description

Pin #	Function	Description
1	Base	RF Input
2	Emitter	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to emitter leads as possible.
3	Collector	RF Output
4	Emitter	Same as Pin 2

Package Dimensions



NOTE:
1. ALL DIMENSIONS ARE IN INCHES
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70 FOR TRIM/FORM. ie: REVERSE TRIM/FORM
6. PACKAGE SURFACE TO BE MIRROR FINISH

A fully dimensioned package outline is available on our website.

Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.