PRELIMINARY

SFF9130-28D

SOLID STATE DEVICES, INC.
14830 Valley View Blvd * La Mirada, Ca 90638
Phone: (562) 404-7855 * Fax: (562) 404-1773

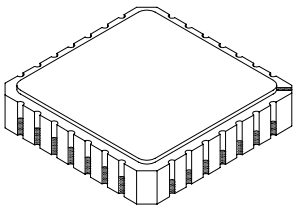
-11 AMP
-100 VOLTS
0.30Ω
DUAL UNCOMMITED
P-CHANNEL POWER MOSFET

DESIGNER'S DATA SHEET

FEATURES:

- **Rugged construction with poly silicon gate**
- **Low RDS (on) and high transconductance**
- **Excellent high temperature stability**
- **Very fast switching speed**
- **Fast recovery and superior dv/dt performance**
- **Increased reverse energy capability**
- **Low input transfer capacitance for easy paralleling**
- **Hermetically sealed surface mount package**
- **TX, TXV and Space Level screening available**
- **Replaces: 2x IRF9130 Types**

28 PIN CLCC



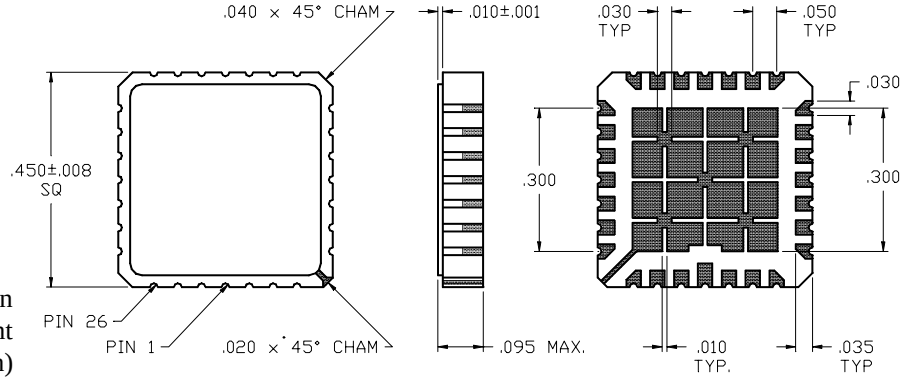
MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Drain to Source Voltage		V_{DS}	-100	Volts
Gate to Source Voltage		V_{GS}	±20	Volts
Continuous Drain Current	T_C = 25°C T_C = 100°C	I_D	-11 -7	Amps
Operating and Storage Temperature		T_{op} & T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case (Both)		$R_{\theta JC}$	3.5	°C/W
Total Device Dissipation	T_C = 25°C T_C = 55°C	P_D	36 37	Watts
Single Pulse Avalange Energy		E_{AS}	84	mJ
Repetitive Avalange Energy		E_{AR}	7.5	mJ

PACKAGE OUTLINE: 28 PIN CLCC

PIN OUT:
SOURCE (1): 16 - 21
DRAIN (1): 24 - 28
GATE (1): 22
SOURCE (2): 9 - 14
DRAIN (2): 2 - 6
GATE (2): 8

NOTE:
All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FP0035D

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ELECTRICAL CHARACTERISTICS @ T_J =25°C (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (VGS =0 V, ID =1mA)		**BV_{DSS}**	-100	-	-	**V**
Temperature Coefficient of Breakdown Voltage		**$\frac{\Delta BV_{DSS}}{\Delta T_J}$**	-	0.87	-	**V**
Drain to Source ON State Resistance 1/ (VGS = -10 V)	**I_D** = 7A **I_D** = 11A	**$R_{DS(on)}$**	- -	- -	0.30 0.35	Ω
Gate Threshold Voltage (VDS =VGS, ID =250µA)		**$V_{GS(th)}$**	-2.0	-	-4.0	**V**
Forward Transconductance (VDS > ID(on) x RDS (on) Max, IDS = 7A)		**gf_s**	3.0	5.0	-	**S(℧)**
Zero Gate Voltage Drain Current (VDS = 80% rated VDS, VGS =0 V, T_A = 25°C) (VDS = 80% rated VDS, VGS =0 V, T_A = 125°C)		**I_{DSS}**	- -	- -	-25 250	**µA**
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	At rated VGS	**I_{GSS}**	- -	- -	-100 100	**nA**
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	VGS = -10 Volts 50% rated VDS ID = -11A	**Qg** **Qgs** **Qgd**	15 1 2	26 3 14	29 7.1 21	**nC**
Turn on Delay Time **Rise Time** **Turn off DELAY Time** **Fall Time**	VDD = 50% of rated VDS ID = 11A RG = 7.5Ω	**$t_{d\ (on)}$** **tr** **$t_{d\ (off)}$** **tf**	- - - -	15 10 30 12	60 140 140 140	**nsec**
Diode Forward Voltage (I_S = rated I_D, V_{GS} = 0V, T_J = 25°C)		**V_{SD}**	-	-	-4.7	**V**
Diode Reverse Recovery Time **Reverse Recovery Charge**	TJ = 25°C IF = 10A di/dt = 100A/µsec	**t_{rr}** **Q_{RR}**	- -	125 -	250 3	**nsec** **µC**
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	VGS = 0 Volts VDS = -25 Volts f = 1 MHz	**Ciss** **Coss** **Crss**	- - -	860 350 125	- - -	**pF**

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES:

1/ All package pins of the same terminations (Drain/Source/Gate) must be connected together to minimize $R_{DS(on)}$ and maximize current carrying capability.