



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

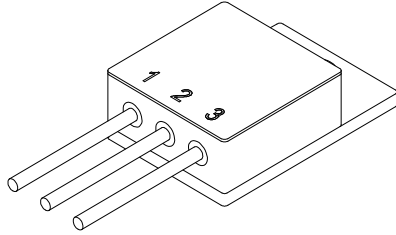
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SFF20P10J

DESIGNER'S DATA SHEET

TO-257



20 AMP /100 Volts
200 mW
P-Channel MOSFET

Features:

- Rugged construction with polysilicon gate
- Low ON-resistance and high transconductance
- Excellent high temperature stability
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- replacement for IRF9140 types
- TX, TXV, S-Level screening available

Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	-100	V
Gate - Source Voltage	V_{GS}	± 20	V
Max. Continuous Drain Current (package limited)	I_{D1}	20	A
	I_{D2}	11	A
Max. Avalanche current	I_{AR}	20	A
Repetitive Avalanche Energy	E_{AR}	12.5	mJ
Single Pulse Avalanche Energy	E_{AS}	500	mJ
Total Power Dissipation	P_D	100	W
Operating & Storage Temperature	$T_{OP} \& T_{STG}$	-55 to +150	$^{\circ}C$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.25	$^{\circ}C/W$

PACKAGE OUTLINE:
TO-257 (J)
PINOUT:
PIN 1: DRAIN
PIN 2: SOURCE
PIN 3: GATE

The technical drawings show the package dimensions in inches. Key dimensions include: 2x $\phi .150$ (top holes), $.420$ (top hole spacing), $.537$ (total height), $.665$ (case height), $.430$ (case width), $.190$ (lead length), $.045$ (lead thickness), $.170$ MIN (lead tip radius), $2 \times .180$ (lead spacing), $3 \times \phi .035$ (lead diameter), $2 \times .105$ (lead length), $.125$ (lead length), and $.170$ MIN (lead tip radius). Suffixes JDB and JUB are shown with their respective lead configurations.

NOTE: All specifications are subject to change without notification. SC'D's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0012A

DOC



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Electrical Characteristics ^{4/}	Symbol	Min	Typ	Max	Units	
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1 \text{ mA}$	BV_{DSS}	-100	—	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 11A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 20A, T_j = 25^\circ C$	R_{DS(on)}	—	140 150	200 230	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	V_{GS(th)}	-2.0	—	-4.0	V
Gate to Source Leakage	$V_{GS} = \pm 20V$	I_{GSS}	—	5	±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -80V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = -80V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	—	0.01 0.75	25 250	μA μA
Forward Transconductance	$V_{DS} = 10V \text{ min}, I_D = 11A, T_j = 25^\circ C$	g_{fs}	6	55	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	55	70	nC
Gate to Source Charge	$V_{DS} = 50V$	Q_{gs}	—	12	15	
Gate to Drain Charge	$I_D = 18A$	Q_{gd}	—	29	45	
Turn on Delay Time	$V_{GS} = 10V$	t_{d(on)}	—	30	35	nsec
Rise Time	$V_{DS} = 50V$	t_r	—	27	85	
Turn off Delay Time	$I_D = 18A$	t_{d(off)}	—	70	85	
Fall Time	$R_G = 9.1\Omega$	t_f	—	45	65	
Diode Forward Voltage	$I_F = 20A, V_{GS} = 0V$	V_{SD}	—	1.90	4.20	V
Diode Reverse Recovery Time	$I_F = 20A, di/dt = 100A/\mu sec$	t_{rr}	—	270	350	nsec
Peak Reverse Recovery Current		Q_{rr}	—	2	3.6	μC
Reverse Recovery Charge						
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	1400	1650	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	600	740	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	180	260	

NOTES:
 * Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.
 4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

