



PRELIMINARY

# SFF120-28Q

## SOLID STATE DEVICES, INC.

14005 Stage Road \* Santa Fe Springs, Ca 90670  
Phone: (562) 404-4474 \* Fax: (562) 404-1773

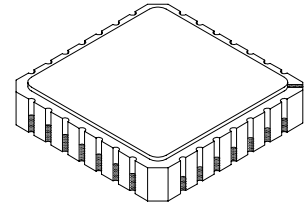
### DESIGNER'S DATA SHEET

#### FEATURES:

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces 4x IRF120 Types in One Package

**9.2 AMPS**  
**100 VOLTS**  
**0.35Ω**  
**QUAD N-CHANNEL**  
**POWER MOSFET**

28 PIN CLCC



### MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	100	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current	I <sub>D</sub>	9.2	Amps
Operating and Storage Temperature	T <sub>op</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance, Junction to Case (All Four)	R <sub>θJC</sub>	10	°C/W
Total Device Dissipation		@ TC = 25°C @ TC = 70°C	Watts
		12.5 9.5	

### PACKAGE OUTLINE: 28

#### PIN OUT:

##### MOSFET 1

DRAIN: 5, 6, 7  
GATE: 1  
SOURCE: 2, 3, 4

##### MOSFET 2

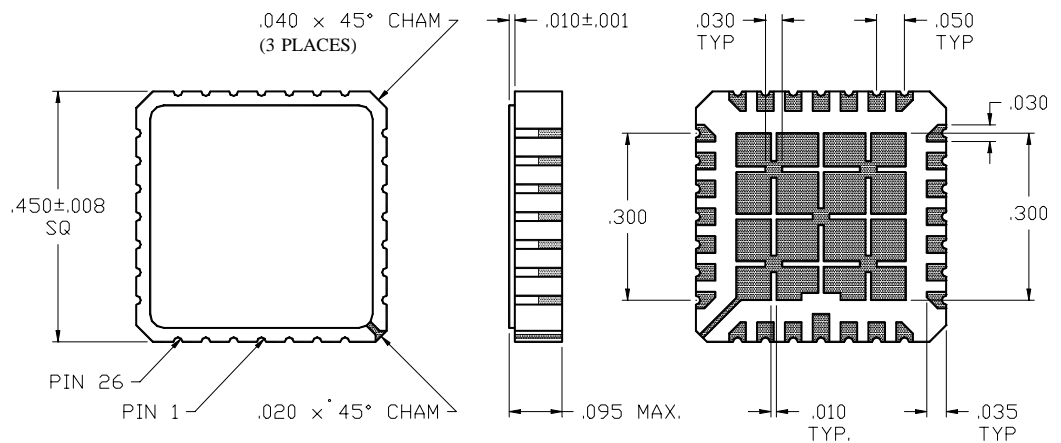
DRAIN: 9, 10, 11  
GATE: 8  
SOURCE: 12, 13, 14

##### MOSFET 3

DRAIN: 19, 20, 21  
GATE: 15  
SOURCE: 16, 17, 18

##### MOSFET 4

DRAIN: 23, 24, 25  
GATE: 22  
SOURCE: 26, 27, 28



**NOTE:** All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)

**NOTE:** All specifications are subject to change without notification. SCDs for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: F00225B**

# SFF120-28Q

PRELIMINARY



**SOLID STATE DEVICES, INC.**

14005 Stage Road \* Santa Fe Springs, Ca 90670

Phone: (562) 404-4474 \* Fax: (562) 404-1773

## ELECTRICAL CHARACTERISTICS @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
<b>Drain to Source Breakdown Voltage</b> ( $V_{GS} = 0\text{ V}$ , $I_D = 250\mu\text{A}$ )		<b><math>BV_{DSS}</math></b>	100	-	-	<b>V</b>
<b>Drain to Source ON State Resistance</b> ( $V_{GS} = 10\text{ V}$ , 60% of Rated ID)		<b><math>R_{DS(on)}</math></b>	-	-	0.35	<b><math>\Omega</math></b>
<b>ON State Drain Current</b> ( $V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $V_{GS} = 10\text{ V}$ )		<b><math>I_D(on)</math></b>	9.2	-	-	<b>A</b>
<b>Gate Threshold Voltage</b> ( $V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$ )		<b><math>V_{GS(th)}</math></b>	2.0	-	4.0	<b>V</b>
<b>Forward Transconductance</b> ( $V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $I_{DS} = 60\%$ rated ID)		<b><math>g_{fs}</math></b>	2.7	4.1	-	<b><math>S(\Omega)</math></b>
<b>Zero Gate Voltage Drain Current</b> ( $V_{DS} = \text{max rated Voltage}$ , $V_{GS} = 0\text{V}$ ) ( $V_{DS} = 80\%$ rated $V_{DS}$ , $V_{GS} = 0\text{V}$ , $T_A = 125^\circ\text{C}$ )		<b><math>I_{DSS}</math></b>	-	-	25 250	<b><math>\mu\text{A}</math></b>
<b>Gate to Source Leakage Forward</b> <b>Gate to Source Leakage Reverse</b>	At rated $V_{GS}$	<b><math>I_{GSS}</math></b>	-	-	+100 -100	<b>nA</b>
<b>Total Gate Charge</b> <b>Gate to Source Charge</b> <b>Gate to Drain Charge</b>	$V_{GS} = 10\text{ V}$ 80% rated $V_{DS}$ 60% rated ID	<b><math>Q_g</math></b> <b><math>Q_{gs}</math></b> <b><math>Q_{gd}</math></b>	-	10.7 2.9 5.1	16 4.4 7.7	<b>nC</b>
<b>Turn on Delay Time</b> <b>Rise Time</b> <b>Turn off DELAY Time</b> <b>Fall Time</b>	$V_{DD} = 50\%$ rated $V_{DS}$ 50% rated ID $R_G = 18\ \Omega$	<b><math>t_d(on)</math></b> <b><math>t_r</math></b> <b><math>t_d(off)</math></b> <b><math>t_f</math></b>	-	13 30 19 20	20 45 29 30	<b>nsec</b>
<b>Diode Forward Voltage</b> ( $I_S = \text{rated } I_D$ , $V_{GS} = 0\text{V}$ , $T_J = 25^\circ\text{C}$ )		<b><math>V_{SD}</math></b>	-	-	2.5	<b>V</b>
<b>Diode Reverse Recovery Time</b> <b>Reverse Recovery Charge</b>	$T_J = 25^\circ\text{C}$ $I_F = \text{rated ID}$ $di/dt = 100\text{A}/\mu\text{sec}$	<b><math>t_{rr}</math></b> <b><math>Q_{RR}</math></b>	55 0.25	140 0.65	260 1.3	<b>nsec</b> <b><math>\mu\text{C}</math></b>
<b>Input Capacitance</b> <b>Output Capacitance</b> <b>Reverse Transfer Capacitance</b>	$V_{GS} = 0\text{ Volts}$ $V_{DS} = 25\text{ Volts}$ $f = 1\text{ MHz}$	<b><math>C_{iss}</math></b> <b><math>C_{oss}</math></b> <b><math>C_{rss}</math></b>	-	350 130 36	- - -	<b>pF</b>

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES: