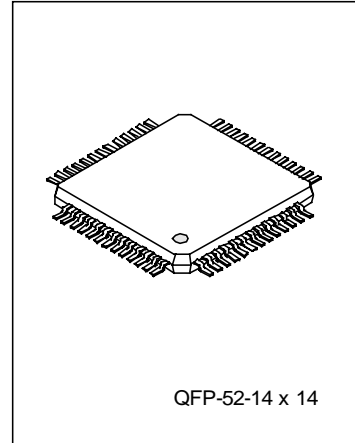


VFD CONTROLLER/DRIVER

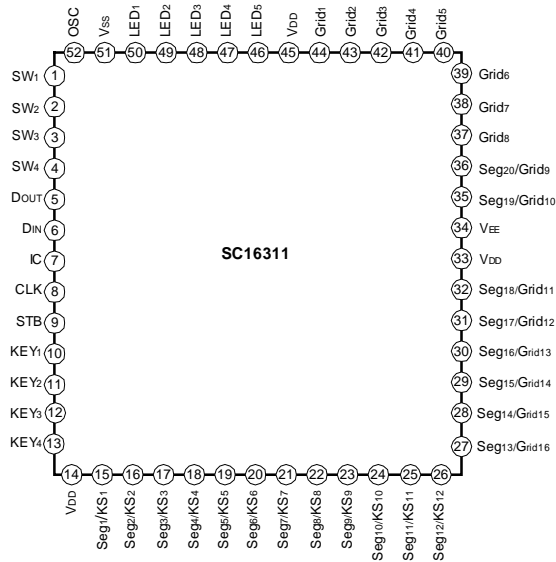
The SC16311 is a FIP (Fluorescent Indicator Panel or Vacuum Fluorescent Display) controller/driver that is driven on a 1/8- to 1/16 duty factor. It consists of 12 segment output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the SC16311 through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device of a single-chip microcomputer.



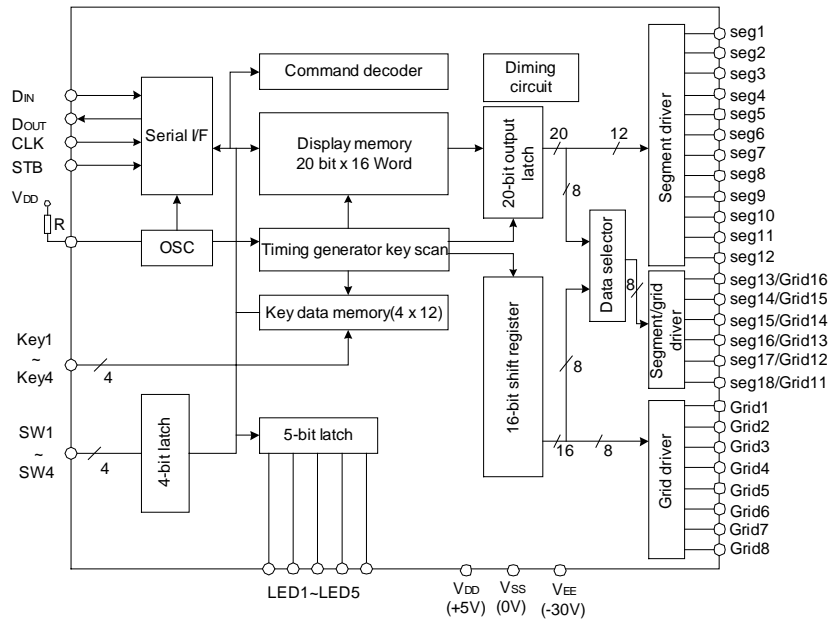
FEATURES

- Many display modes (12-segment & 16-digit to 20-segment & 8-digit)
- Key scanning (12x4 matrices)
- Dimming circuit (eight steps)
- High-voltage output (VDD-35 V max).
- LED ports (5 chs., 20 mA max).
- General-purpose input port (4 bits)
- No external resistor necessary for driver outputs (P-ch open-drain + pull-down resistor output)
- Serial interface (CLK, STB, DIN, DOUT)

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Units
Logic Supply Voltage	V _{DD}	-0.5~ +7.0	V
Driver Supply Voltage	V _{EE}	V _{DD} +0.5 ~V _{DD} -40	V
Logic Input Voltage	V _{I1}	-0.5~V _{DD} +0.5	V
FIP Driver Output Voltage	V _{O2}	V _{EE} -0.5~V _{DD} +0.5	V
LED Driver Output Current	I _{O1}	+25	mA
FIP Driver Output Current	I _{O2}	-40(grid) -15(segment)	mA
Power Dissipation	PD	1200*	mW
Operating Ambient Temperature	TOPT	-40~+85	°C
Storage Temperature	TSTG	-65~+150	°C

*: Dreate at -9.6 Mw/ °C at Ta= 25°C or higher.

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RECOMMENDED OPERATING CONDITIONS (Ta = -20 to +70°C, VSS = 0 V)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	4.5	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD		VDD	V
Low-Level Input Voltage	VIL	0		0.3VDD	V
Driver Supply Voltage	VEE	0		VDD-35	V

ELECTRICAL CHARACTERISTICS (TA=-20~+70°C, VDD=4.5~5.5V, VSS=0V, VEE=VDD-35V)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
High-Level Output Voltage	VOH1	LED, IOH1=-1mA	0.9VDD			V
Low-Level Output Voltage	VOL1	LED, IOL1=20mA			1	V
Low-Level Output Voltage	VOL2	DOUT, IOL2=4mA			0.4	V
High-Level Output Current	IOH21	VO=VDD-2V, Seg1~Seg12	-3			mA
High-Level Output Current	IOH22	VO=VDD-2V, Grid1~Grid8, Seg13/Grid16 ~Seg18/Grid11	-15			mA
Driver Leakage Current	IOLEAK	VO=VDD-35V, driver off			-10	μA
Output Pull-Down Resistor	RL	driver output	50	100	150	KΩ
Input Current	II	VI=VDD or VSS			±1	μA
High-Level Input Voltage	VIH		0.7VDD			V
Low-Level Input Voltage	VIL				0.3VDD	V
Hysteresis Voltage	VH	CLK, DIN, STB		0.35		V
Dynamic Current Consumption	IDDdyn	Under no load, display off			5	mA

SWITCHING CHARACTERISTICS (Ta = -20 to +70°C, VDD = 4.5 to 5.5 V, VEE = -30 V)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Oscillation Frequency	tOSC	R=56kΩ		350	500	650	kHz
Propagation Delay Time	tPLZ	CLK→DOUT, CL=15pF,				300	ns
	tPZL	RL=10KΩ				100	ns
Rise Time	tTZH1	CL=300pF	Seg1~Seg12			2	μs
	tTZH2		Grid1~Grid8, Seg13/Grid16~ Seg20/Grid9			0.5	μs
Fall time	tTZH	CL=300pF, Segn, Gridn				120	μs
Maximum Clock Frequency	fmax	Duty = 50%		1			MHz
Input Capacitance	CI					15	pF

TIMING CONDITIONS (TA=-20~+70°C, VDD=4.5~5.5V)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max	Unit
Clock Pulse Width	PWCLK		400			ns
Strobe Pulse Width	PWSTB		1			μs
Data Setup Time	tSETUP		100			ns
Data Hold Time	tHOLD		100			ns
Clock-Strobe Time	tCLK-STB	CLK↑→STB↑	1			μs
Wait Time	tWAIT	CLK↑→CLK↓	1			μs

PIN DESCRIPTION

Pin NO	Symbol	Pin name	Description
1~4	SW1~SW4	Switch input	These pins constitute 4-bit general-purpose input port
5	DOUT	Data output	Output serial data at falling edge of shift clock, starting from lower bit. This is N-ch open-drain output pin.
6	DIN	Data input	Inputs serial data at rising edge of shift clock, starting from lower bit.
7	IC	Internally connected	Be sure to leave this pin open (this pin is at VDD level)

(To be continued)

(Continued)

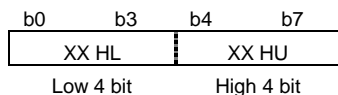
Pin NO	Symbol	Pin name	Description
8	CLK	Clock input	Reads serial data at rising edge, and outputs data at falling edge.
9	STB	Strobe	Initializes serial interface at rising or falling edge to make SC16311 waiting for reception of command. Data input after STB has fallen is processed as command. While command data is processed, current processing is stopped, and serial interface is initialized. While STB is high, CLK is ignored.
10~13	Key1~Key4	Key data input	Data input to these pins is latched at end of display cycle.
14,33,45	VDD	Logic power	5V±10%
15~26	Seg1/KS1~ Seg12/KS12	High-voltage output (segment)	Segment output pins.
27~32, 35, 36	Seg13/Grid16~S eg20/Grid9	High-voltage output (grid/segment)	These pins are selectable for segment or grid output.
34	VEE	Pull-down level	VDD-35V
37~44	Grid8 ~ Grid1	High-voltage output (grid)	Grid output pins
46-50	LED1~LED5	LED output	CMOS output. +20mV .max.
51	VSS	Logic ground	Connect this pin to GND of system.
52	OSC	Oscillator pin	Connect resistor for determining oscillation frequency to this pin.

FUNCTION DESCRIPTION

Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the SC16311 through the serial interface, and is assigned addresses as follows, in units of 8 bits:

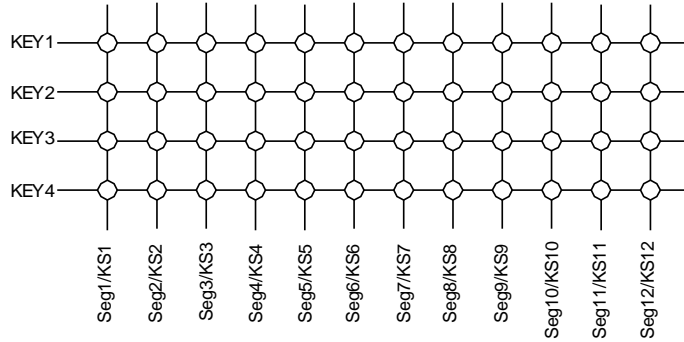
Seg1	Seg4	Seg8	Seg12	Seg16	Seg20	
00HL		00HU	01HL	01HU	02HL	DIG1
03HL		03HU	04HL	04HU	05HL	DIG2
06HL		06HU	07HL	07HU	08HL	DIG3
09HL		09HU	0AHL	0AHU	0BHL	DIG4
0CHL		0CHU	0DHL	0DHU	0EHL	DIG5
0FHL		0FHU	10HL	10HU	11HL	DIG6
12HL		12HU	13HL	13HU	14HL	DIG7
15HL		15HU	16HL	16HU	17HL	DIG8
18HL		18HU	19HL	19HU	1AHL	DIG9
1BHL		1BHU	1CHL	1CHU	1DHL	DIG10
1EHL		1EHU	1FHL	1FHU	20HL	DIG11
21HL		21HU	22HL	22HU	23HL	DIG12
24HL		24HU	25HL	25HU	26HL	DIG13
27HL		27HU	28HL	28HU	29HL	DIG14
2AHL		2AHU	2BHL	2BHU	2CHL	DIG15
2DHL		2DHU	2EHL	2EHU	2FHL	DIG16



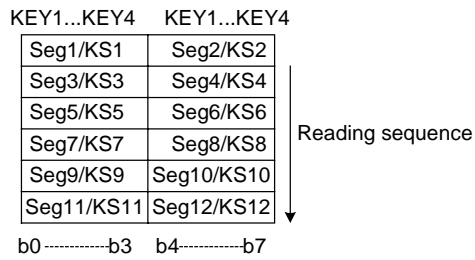
Only the lower 4 bits of the addresses assigned to Seg17 through Seg20 are valid, and the higher 4 bits are ignored.

Key Matrix and Key-Input Data Storage RAM

The key matrix is of 12 x 4 configuration, as shown below.



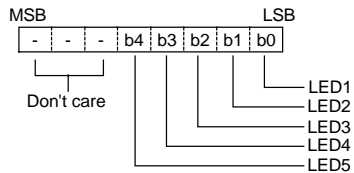
The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.



When the most significant bit of data (Seg12 b7) has been read, the least significant bit of the next data (Seg1 b0) is read.

LED Port

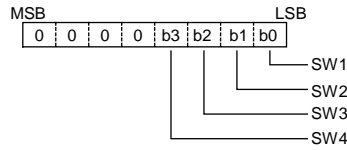
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.



On power application, all the LEDs remain dark.

SW data

The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



Command

A command sets the display mode and status of the FIP driver.

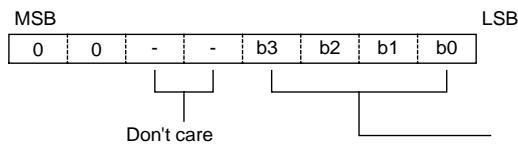
The first 1 byte input to the SC16311 through the DIN pin after the STB pin has fallen is regarded as a command.

If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

(1) Display mode setting command

This command initializes the SC16311 and selects the number of segments and number of grids (1/8 to 1/16 duty, 12 segments to 20 segments).

When this command is executed, display is forcibly turned off, and key scanning is also stopped. To resume display, a display ON command must be executed. If the same mode is selected, however, nothing is performed.

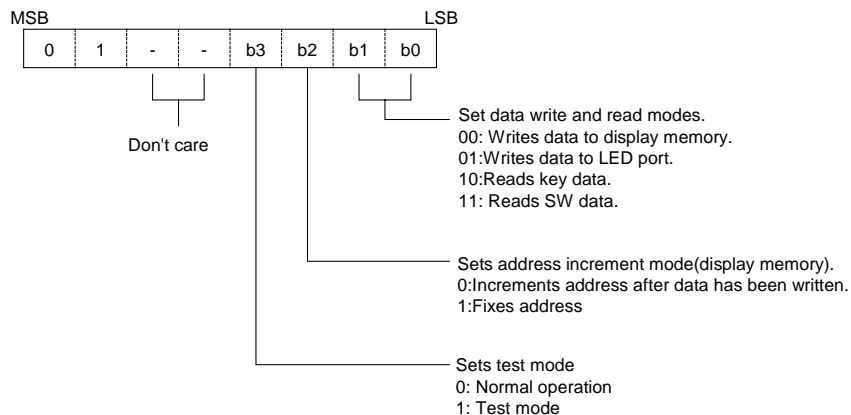


- Selects display mode
- 0XXX: 8 digits, 20 segments
 - 1000: 9 digits, 19 segments
 - 1001: 10 digits, 18 segments
 - 1010: 11 digits, 17 segments
 - 1011: 12 digits, 16 segments
 - 1100: 13 digits, 15 segments
 - 1101: 14 digits, 14 segments
 - 1110: 15 digits, 13 segments
 - 1111: 16 digits, 12 segments

On power application, the 16-digit, 12-segment mode is selected.

(2) Data setting command

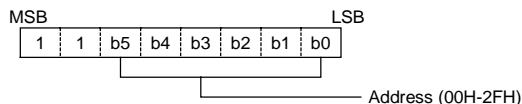
This command sets data write and data read modes.



On power application, the normal operation mode and address increment mode are set.

(3) Address setting command

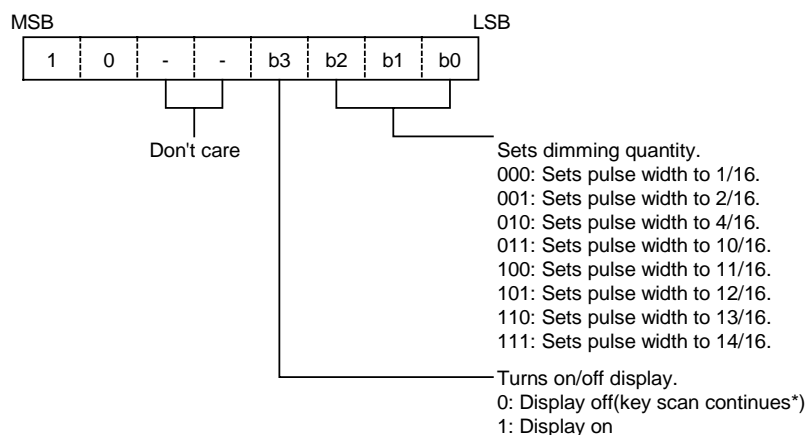
This command sets an address of the display memory.



If address 30H or higher is set, the data is ignored, until a correct address is set.

On power application, the address is set to 00H.

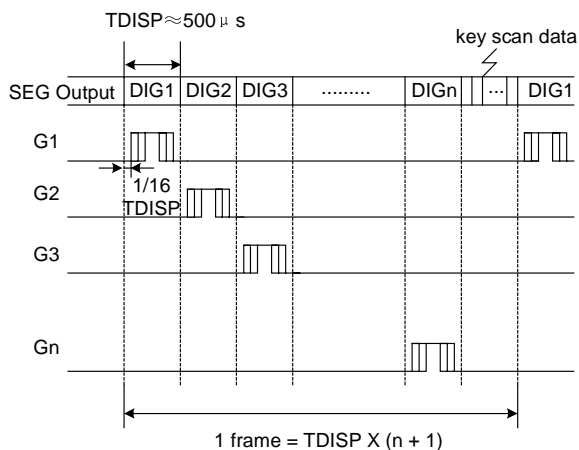
(4) Display control command



On power application, the 1/16-pulse width is set and the display is turned off.

*: On power application, key scanning is stopped.

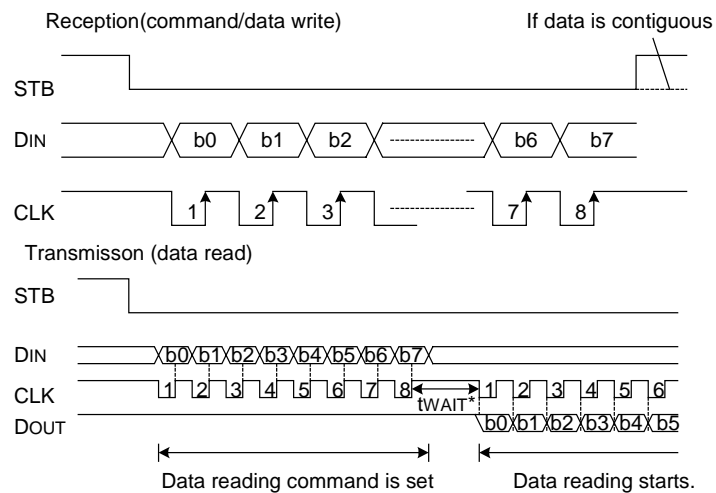
Key Scanning and Display Timing



One cycle of key scanning consists of two frames, and data of 12 x 4 matrices is stored in RAM.

Serial Communication Format

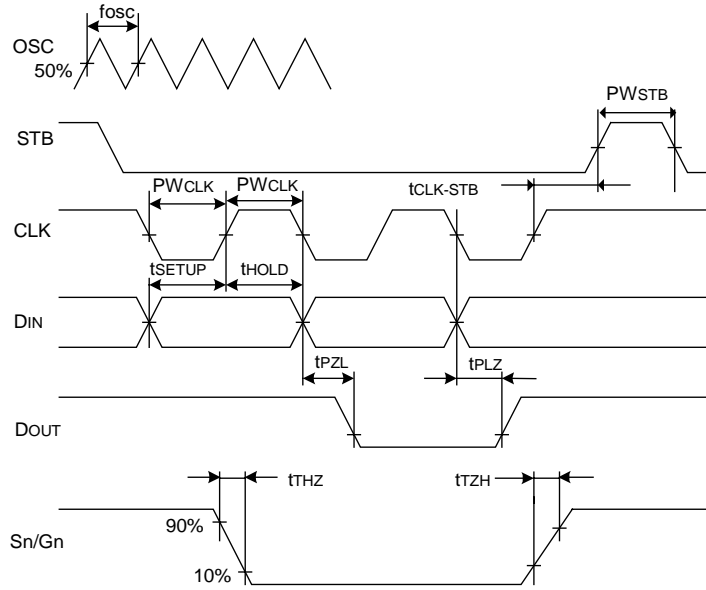
Reception (command/data write)



Because the DOUT pin is an N-ch , open-drain output pin, be sure to connect an external pull-up resistor to this pin (1 k Ω to 10 k Ω).

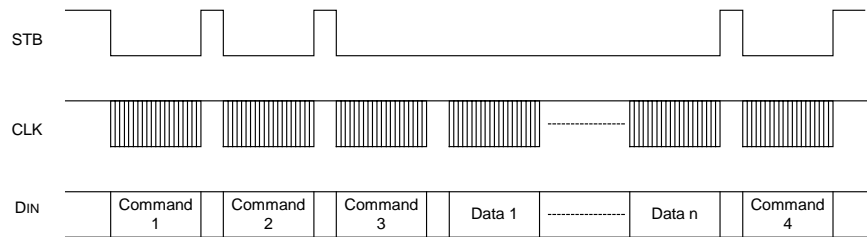
*: When data is read, a wait time t_{WAIT} of 1 μ s is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

Switching Characteristic Waveform



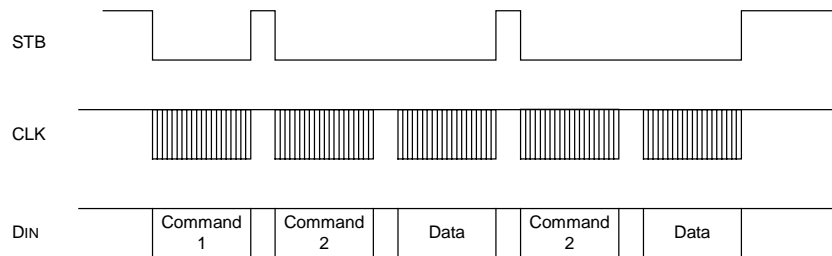
Applications

Updating display memory by incrementing address



- Command 1: sets display mode
- Command 2: sets data
- Command 3: sets address
- Data 1 to n: transfers display data (48 bytes max.)
- Command 4: controls display

Updating specific address

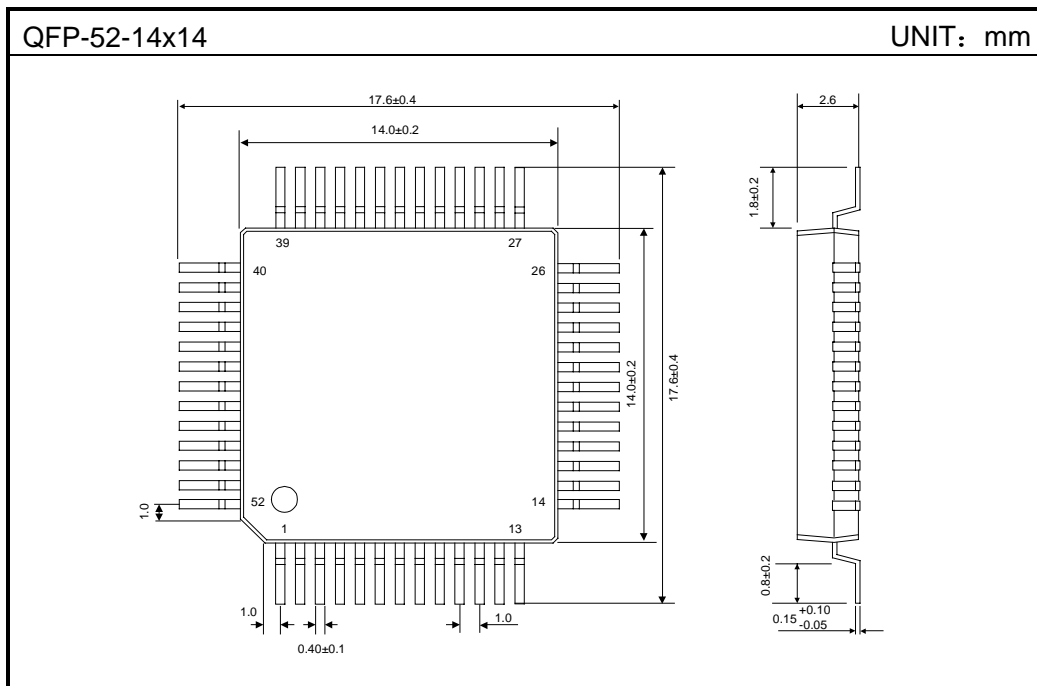


Command 1: sets data

Command 2: sets address

Data: display data

PACKAGE OUTLINE



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