## BLOCK MODE TIME SLOT ALLOCATION CIRCUIT

## DESCRIPTION

The SA8702 (BMTSAC) is a Block Mode Time Slot Allocation Circuit. The device is used to generate 8 consecutive timeslots in one of 4 blocks in a 32 time-slot PCM system. Each timeslot pulse is 8 BLCK cycles long. BCLK is the 2,048 station clock provided by the system. An active MRST will disable all outputs until a valid XSYNC input is recognised. The output TSX is delayed by half a cycle and indicates that one of 8 timeslots is currently active. There are 4 possible modes of operation, selectable by means of the BL0 and BL1 pins (See Table 1).

## PIN CONNECTIONS

All inputs and outputs are C-MOS compatible. All outputs are push-pull with the exception of TSX which is open drain. The inputs MRST and BCLK are Schmitt Trigger. Inputs BL0 and BL1 have pull-ups. (See figure 1).

## APPLICATIONS

- PCM Switching Systems
- PCM Transmission Systems
- Subscriber Multiplex Equipment
- PBX Systems


Figure 1.

## Operating Modes

| BL1 | BLO | Mode of Operation |
| :--- | :--- | :--- |
| 0 | 0 | Outputs active in timeslots 0 to 7 |
| 0 | 1 | Outputs active in timeslots 8 to 15 |
| 1 | 0 | Outputs active in timeslots 16 to 23 |
| 1 | 1 | Outputs active in timeslots 24 to 31 |

Table 1.

Input pulse XSYNC occurs periodically in every frame and is used to generate the first of the eight timeslots and also defines the beginning of Block 0. If XSYNC fails high then the outputs will be generated as they were before the failure occured. Should XSYNC fail low then the outputs will be deactivated after completion of the frame.

## Maximum Ratings

All voltages measured with respect to $\mathrm{V}_{\mathrm{ss}}$.

| Parameter | Symbol | Value | Units |
| :--- | :---: | :---: | :---: |
| Supply voltage | $\mathrm{V}_{\mathrm{DD}}$ | $+7,5$ | V |
| Positive voltage on any pin | $\mathrm{V}_{\mathrm{HM}}$ | $\mathrm{V}_{\mathrm{DD}}+0,3$ | V |
| Negative voltage on any pin | $\mathrm{V}_{\mathrm{LM}}$ | $\mathrm{V}_{\mathrm{SS}}-0,3$ | V |
| Maximum current through any pin | $\mathrm{I}_{\mathrm{HM}}$ | $\pm 10$ | mA |
| Storage temperature | $\mathrm{T}_{\mathrm{ST}}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating temperature | $\mathrm{T}_{\mathrm{O}}$ | -10 to +70 | ${ }^{\circ} \mathrm{C}$ |

Stresses beyond these values may cause permanent damage to the device. Exposure to maximum rated conditions for extended periods may affect device reliability.

## Operating Conditions:

All voltages measured with respect to $\mathrm{V}_{\mathrm{ss}}$. Inputs must never be left open.

| DC Parameters | Symbol | Min. | Nom. | Max. | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- |
| Supply Voltage | $\mathrm{V}_{\mathrm{DD}}$ | 4,75 | 5,00 | 5,25 | V | - |
| * Input Low Voltage | $\mathrm{V}_{\mathrm{IL}}$ | - | - | 1,0 | V | $\mathrm{~V}_{\mathrm{DD}}=5 \mathrm{~V}$ |
| ${ }^{*}$ Input High Voltage | $\mathrm{V}_{\mathrm{H}}$ | 4,0 | - | - | V | $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}$ |
| ${ }^{* *}$ Output Low Voltage | $\mathrm{V}_{\mathrm{OL}}$ | - | - | 0,5 | V | $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}$ <br> $\mathrm{I}_{\mathrm{ol}}$ <br> $=0,5 \mathrm{~mA}$ |
| ** Output High Voltage | $\mathrm{V}_{\mathrm{OH}}$ | 4,5 | - | - | V | $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}$ <br> $\mathrm{I}_{\mathrm{oh}}$ <br> $=0,5 \mathrm{~mA}$ |
| Operating Frequency |  | - | 2,048 | 2,273 | MHz | $4,75 \leq \mathrm{V}_{\mathrm{DD}}$ <br> $\leq 5,25$ |
| Operating Temp. range |  | -10 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ | - |

* All inputs are C-MOS level compatible. Pins 6 and 7 have internal pull-up devices.
** All outputs are push-pull except pin 1 which is open drain.

| AC Parameters | Symbol | Min. | Nom. | Max. | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| XSYNC setup before <br> BCLK goes low | $\mathrm{T}_{\mathrm{s}}$ | 60 | - | - | ns | $4,75 \leq \mathrm{V}_{\mathrm{DD}}$ <br> $\leq 5,25$ |
| Output propagation <br> delay from active clock <br> edge | $\mathrm{T}_{\mathrm{pd}}$ | - | - | 150 | ns | $4,75 \leq \mathrm{Vdd}$ <br> $\leq 5,25$ |
| XSYNC hold time from <br> BCLK | $\mathrm{T}_{\mathrm{h}}$ | 50 | - | - | ns | $4,75 \leq \mathrm{V}_{\mathrm{DD}}$ <br> $\leq 5,25$ |

PIN DESCRIPTION

| Pin No. | I/O | Name | Description |
| :---: | :---: | :---: | :---: |
| 1 | 0 | TSX | An open drain N -channel high impedance, but pulls low during any active timeslot. |
| 2 | 1 | $\overline{\text { MRST }}$ | A Schmitt trigger input that asynchronously disables all outputs. |
| 3 | 0 | FSO | A timeslot output which is normally low, and goes active-high for 8 cycles of BCLK when a valid XSYNC is made. |
| 4 | 0 | FS1 | Similar to pin 3. |
| 5 | O | FS2 | Similar to pin 3. |
| 6 | I | BLO | The input for the LSB of the 2 bit word which defines the active block. |
| 7 | 1 | BL1 | The input for the MSB of the 2 bit word which defines the active block. |
| 8 | 1 | VSS | The OV ground connection to the device. |
| 9 | 1 | BCLK | The $2,048 \mathrm{MHz}$ station clock input. |
| 10 | 1 | XSYNC | The input pulse XSYNC used to generate the first of the eight timeslots and also defines the beginning of block 0 . |
| 11 | 0 | FS7 | Similar to pin 3. |
| 12 | 0 | FS6 | Similar to pin 3. |
| 13 | 0 | FS5 | Similar to pin 3. |
| 14 | 0 | FS4 | Similar to pin 3. |
| 15 | O | FS3 | Similar to pin 3. |
| 16 | 1 | VDD | The positive supply to the device. |

## TIMING DIAGRAM



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