S5D4100X

Data Sheet

Revision 0.1

SAMSUNG ELECTRONICS

RECORD OF REVISIONS

Rev. No	Date	Page	Description of Change
0.0	2004/12		First Release
0.1	2005/3	12 ~ 14	Output drive current and Pull Up/Down Pad descriptions
		12	Revision Point: PCKO output drive Current change (20mA $\rightarrow$ 4mA)

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1. OVERVIEW

S5D4100X is a digital interface including Scaler, Image Enhancement, ITU-R VT656 Decoder, OSD, GAMMA and DITHER. S5D4100X supports two ITU-R BT656 Video inputs or one ITU-R BT601 input, and provides R/G/B Serial and ITU-R 656 Outputs or R/G/B Parallel Output

1.1 FEATURES

- **Input Format**
  - ITU-R BT601 / ITU-R BT656 Video Format
  - Support Dual ITU-R BT656 Channel Port
- **ITU Decoder**
  - ITU-R BT656 Decoding
  - Support NTSC / PAL System
- **Image Enhancement**
  - Image Boost-Up (Adaptive Contrast Control)
  - Sharpness Control
  - Color Hue & Saturation Control
- **High-Quality Advanced Scaling**
  - Fully Programmable Image Scaling (Up to XGA)
  - Independent Horizontal / Vertical Image Scale-Up and / or Scale-Down
- **Built-in On-Screen Display**
  - Programmable Character RAM Fonts (256 Fonts)
  - User Friendly Font Size (12x18) and Display Font Number of Window Frame (Up to 450)
  - Various Font Attribute (Raster Enable, Blink, Character Border/Shadow Enable, Half-Tone, Intensity)
- **Economic Clock Source**
  - External X-tal Application (Optional)
  - Programmable Frequency Synthesize in Built-in PLL Core
- **Supports I^2C Bus & 3-Wired / 6-Wired Serial Host Interface**
- **R/G/B Gamma look-up table**
- **8 to 6 bit Dithering**
- **Built-in RGB Black Level / Bright / Contrast Control**
- **Application based Output Data Interface**
  - R/G/B Serial Output for RGB-Dot-Pixel LCD Panel
  - R/G/B Parallel Output for RGB-Pixel Panel
  - ITU-R656, 8-Bit 4:2:2 Data with Embedded
  - Sync Output for External Application
- **Fab. & PKG Information**
  - Fab. Process: L18 (0.18 μm)
  - PKG: 88-FBGA-0707 / 80-TQFP-1212
- **Operating Conditions**
  - 1.8 Volts Internal Core Logic, 3.3 Volts I/O Driver Power

2. PIN CONFIGURATIONS

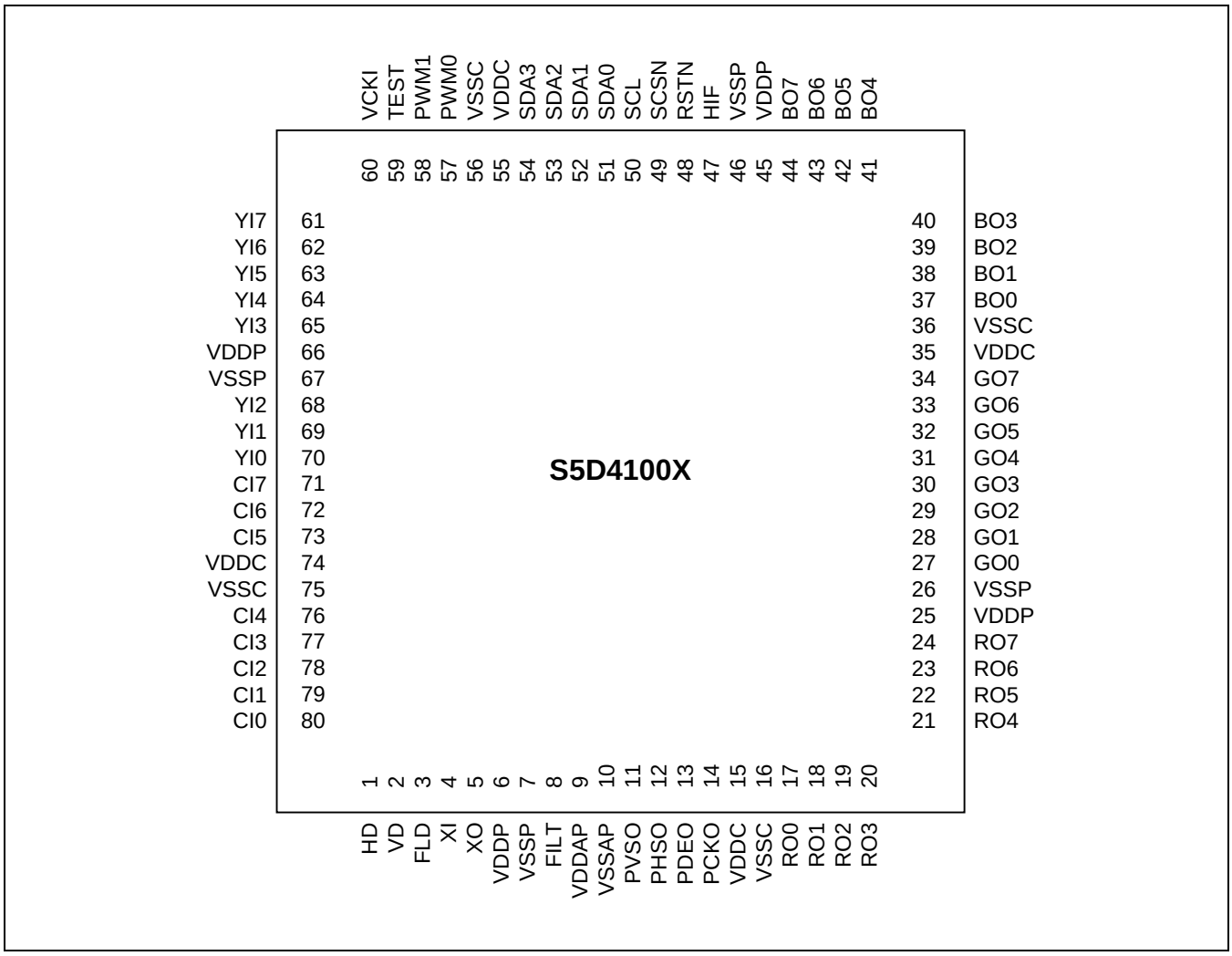


Figure 1. 80-TQFP-1212

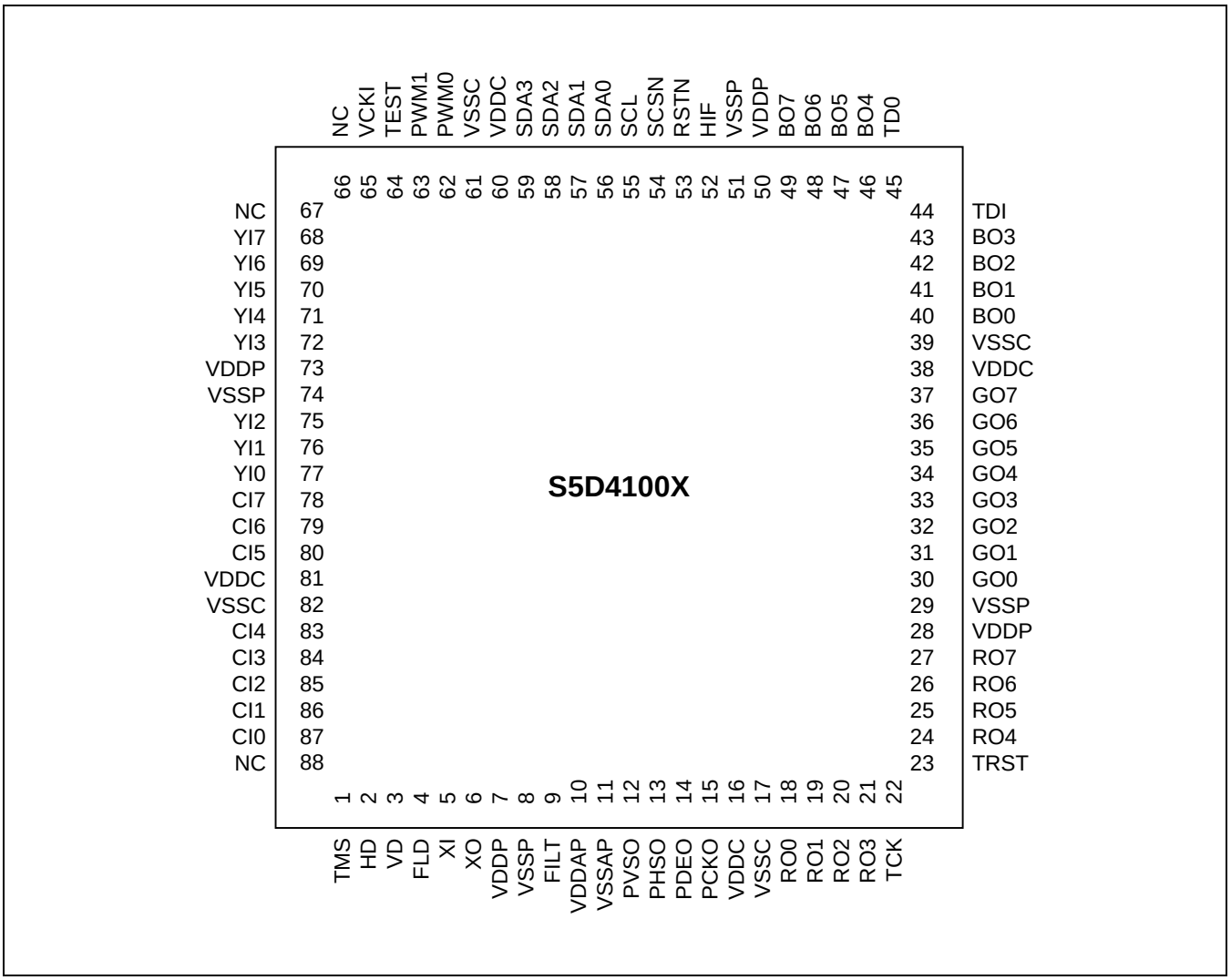


Figure 2. 88-FBGA-0707 (PAD Domain)

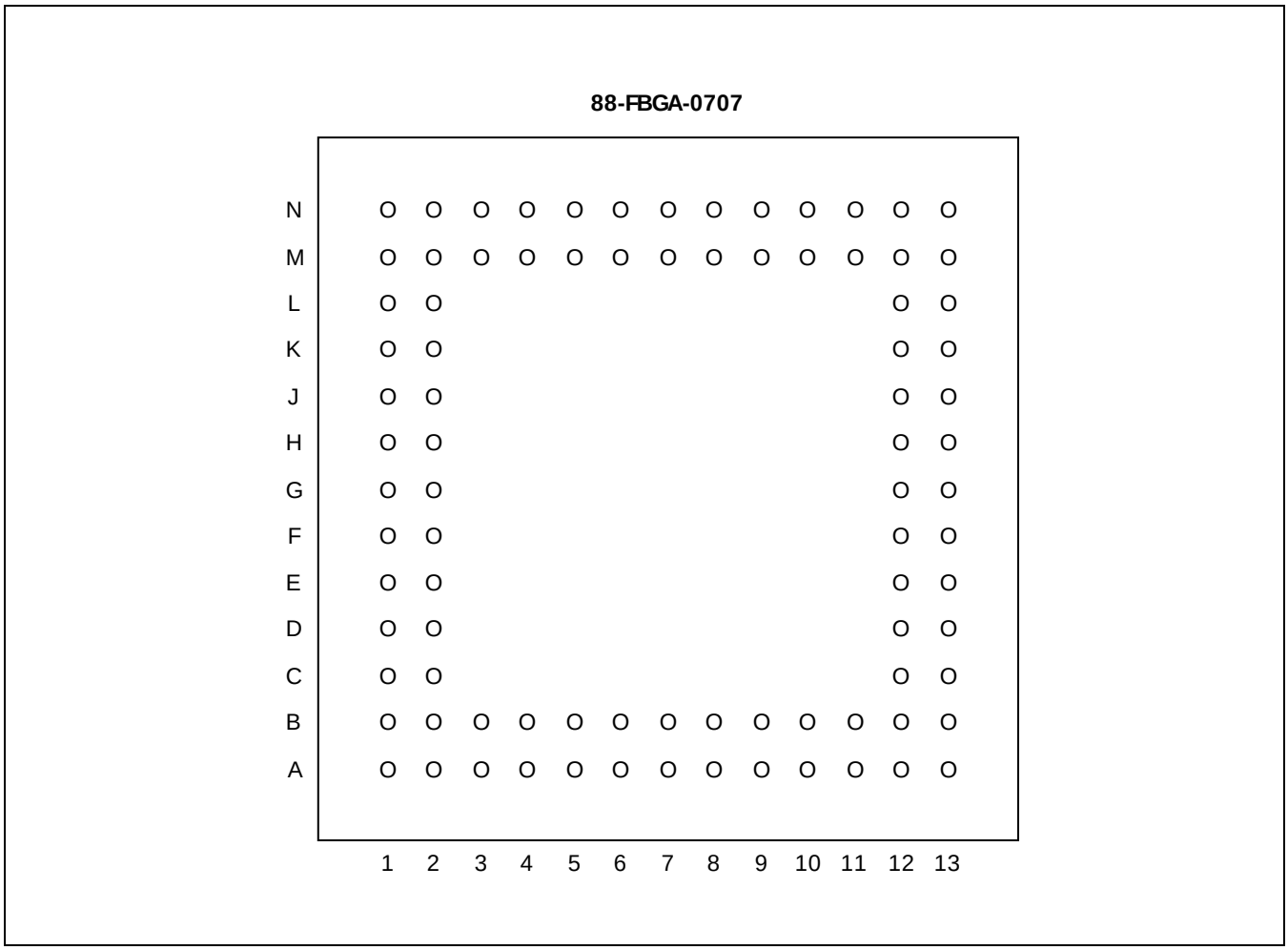


Figure 3. 88-FBGA-0707

2.1 PIN DESCRIPTIONS

Terminal				I/O	Output drive current	Pull up down	Description
Name	Number						
	TQFP	FBGA					
TMS	-	1	B1	I	-	up	JTAC mode (Boundary Scan Design)
HD	1	2	B2	I	-	-	Horizontal Driving Pulse in ITU-R. BT601 /VCKI_B in ITU-R. BT656
VD	2	3	C1	I	-	-	Vertical Driving Pulse in ITU-R. BT601 / VSYNC_A in ITU-R. BT656
FLD	3	4	C2	I	-	-	Field Identification in ITU-R. BT601 /VSYNC_B in ITU-R. BT656
XI	4	5	D1	I	-	-	X-tal Input for External Clock Reference (Free-Run Clock)
XO	5	6	D2	O	12.1mA	-	X-tal Output for External Clock Reference
VDDP	6	7	E1	P	-	-	I/O Pad Drive VDD (3.3V)
VSSP	7	8	E2	G	-	-	I/O Pad Drive VSS
FILT	8	9	F1	O	0.0mA	-	External Loop Filter Terminal for Built-In PLL
VDDAP	9	10	F2	P	-	-	Analog VDD for Built-in PLL (1.8V)
VSSAP	10	11	G1	G	-	-	Analog VSS for Built-in PLL
PVSO	11	12	G2	O	4.0mA	-	Vertical Sync Output for LCD Panel
PHSO	12	13	H1	O	4.0mA	-	Horizontal Sync Output for LCD Panel
PDEO	13	14	H2	O	4.0mA	-	Data Enable Output for LCD Panel
PCKO	14	15	J1	O	4.0mA	-	System Clock Output for LCD Panel
VDDC	15	16	J2	P	-	-	Internal Core Drive VDD (1.8V)
VSSC	16	17	K1	G	-	-	Internal Core Drive VSS
RO0	17	18	K2	O	4.0mA	-	R-CH Output 0 / Serial Output 0 [LSB]
RO1	18	19	L1	O	4.0mA	-	R-CH Output 1 / Serial Output 1
RO2	19	20	L2	O	4.0mA	-	R-CH Output 2 / Serial Output 2
RO3	20	21	M1	O	4.0mA	-	R-CH Output 3 / Serial Output 3
TCK	-	22	M2	I	-	down	JTAC mode (Boundary Scan Design)
TRST	-	23	N1	I	-	up	JTAC mode (Boundary Scan Design)
RO4	21	24	N2	O	4.0mA	-	R-CH Output 4 / Serial Output 4
RO5	22	25	M3	O	4.0mA	-	R-CH Output 5 / Serial Output 5
RO6	23	26	N3	O	4.0mA	-	R-CH Output 6 / Serial Output 6
RO7	24	27	M4	O	4.0mA	-	R-CH Output 7 / Serial Output 7 [MSB]
VDDP	25	28	N4	P	-	-	I/O Pad Drive VDD (3.3V)
VSSP	26	29	M5	G	-	-	I/O Pad Drive VSS
GO0	27	30	N5	O	4.0mA	-	G-CH Output 0 / General Purpose Output 0

Terminal				I/O	Output drive current	Pull up down	Description
Name	Number						
	TQFP	FBGA					
GO1	28	31	M6	O	4.0mA	-	G-CH Output 1 / General Purpose Output 1
GO2	29	32	N6	O	4.0mA	-	G-CH Output 2 / General Purpose Output 2
GO3	30	33	M7	O	4.0mA	-	G-CH Output 3 / General Purpose Output 3
GO4	31	34	N7	O	4.0mA	-	G-CH Output 4 / General Purpose Output 4
GO5	32	35	M8	O	4.0mA	-	G-CH Output 5 / General Purpose Output 5
GO6	33	36	N8	O	4.0mA	-	G-CH Output 6 / ITU-R656 VSYNC Output for Non-Standard Sync Mode
GO7	34	37	M9	O	4.0mA	-	G-CH Output 7 / ITU-R656 VCK Output
VDDC	35	38	N9	P	-	-	Internal Core Drive VDD (1.8V)
VSSC	36	39	M10	G	-	-	Internal Core Drive VSS
BO0	37	40	N10	O	4.0mA	-	B-CH Output 0 / ITU-R656 Output 0 [LSB]
BO1	38	41	M11	O	4.0mA	-	B-CH Output 1 / ITU-R656 Output 1
BO2	39	42	N11	O	4.0mA	-	B-CH Output 2 / ITU-R656 Output 2
BO3	40	43	N13	O	4.0mA	-	B-CH Output 3 / ITU-R656 Output 3
TDI	-	44	N12	I	-	up	JTAC mode (Boundary Scan Design)
TDO	-	45	M13	O	4.0mA	-	JTAC mode (Boundary Scan Design)
BO4	41	46	M12	O	4.0mA	-	B-CH Output 4 / ITU-R656 Output 4
BO5	42	47	L13	O	4.0mA	-	B-CH Output 5 / ITU-R656 Output 5
BO6	43	48	L12	O	4.0mA	-	B-CH Output 6 / ITU-R656 Output 6
BO7	44	49	K13	O	4.0mA	-	B-CH Output 7 / ITU-R656 Output 7 [MSB]
VDDP	45	50	K12	P	-	-	I/O Pad Drive VDD (3.3V)
VSSP	46	51	J13	G	-	-	I/O Pad Drive VSS
HIF	47	52	J12	I	-	down	Host Interface Select ("0":3-Wired or 6-Wired, "1": IIC)
RSTN	48	53	H13	I	-	-	System Reset
SCSN	49	54	H12	I	-	-	Chip Select of the Host Interface
SCL	50	55	G13	I	4.0mA	-	Clock of the Host Interface
SDA0	51	56	G12	I/O	4.0mA	-	Data/Address 0 of the Host I/F [LSB] / SDA in case of IIC
SDA1	52	57	F13	I/O	4.0mA	-	Data/Address 1 of the Host I/F
SDA2	53	58	F12	I/O	4.0mA	-	Data/Address 2 of the Host I/F
SDA3	54	59	E13	I/O	4.0mA	-	Data/Address 3 of the Host I/F [MSB]
VDDC	55	60	E12	P	-	-	Internal Core Drive VDD (1.8V)

Terminal				I/O	Output drive current	Pull up down	Description
Name	Number						
	TQFP	FBGA					
VSSC	56	61	D13	G	-	-	Internal Core Drive VSS
PWM0	57	62	D12	O	4.0mA	-	Pulse Width Modulation 0
PWM1	58	63	C13	O	4.0mA	-	Pulse Width Modulation 1
TEST	59	64	C12	I	-	down	Test Input (Pull-Down)
VCKI	60	65	B13	I	-	-	Video Clock Input in ITU-R. BT601 / VCKI_A in ITU-R. BT656
NC	-	66	A13		-	down	No Connect
NC	-	67	B12		-	down	No Connect
YI7	61	68	A12	I	-	-	Luminance Data Input 7 / ITU-R656 Data A Input 7 [MSB]
YI6	62	69	B11	I	-	-	Luminance Data Input 6 / ITU-R656 Data A Input 6
YI5	63	70	A11	I	-	-	Luminance Data Input 5 / ITU-R656 Data A Input 5
YI4	64	71	B10	I	-	-	Luminance Data Input 4 / ITU-R656 Data A Input 4
YI3	65	72	A10	I	-	-	Luminance Data Input 3 / ITU-R656 Data A Input 3
VDDP	66	73	B9	P	-	-	I/O Pad Drive VDD (3.3V)
VSSP	67	74	A9	G	-	-	I/O Pad Drive VSS
YI2	68	75	B8	I	-	-	Luminance Data Input 3 / ITU-R656 Data A Input 2
YI1	69	76	A8	I	-	-	Luminance Data Input 3 / ITU-R656 Data A Input 1
YI0	70	77	B7	I	-	-	Luminance Data Input 3 / ITU-R656 Data A Input 0 [LSB]
CI7	71	78	A7	I	-	-	Chrominance Data Input 7 / ITU-R656 Data B Input 7 [MSB]
CI6	72	79	B6	I	-	-	Chrominance Data Input 6 / ITU-R656 Data B Input 6
CI5	73	80	A6	I	-	-	Chrominance Data Input 5 / ITU-R656 Data B Input 5
VDDC	74	81	B5	P	-	-	Internal Core Drive VDD (1.8V)
VSSC	75	82	A5	G	-	-	Internal Core Drive VSS
CI4	76	83	B4	I	-	-	Chrominance Data Input 4 / ITU-R656 Data B Input 4
CI3	77	84	A4	I	-	-	Chrominance Data Input 3 / ITU-R656 Data B Input 3
CI2	78	85	B3	I	-	-	Chrominance Data Input 2 / ITU-R656 Data B Input 2
CI1	79	86	A3	I	-	-	Chrominance Data Input 1 / ITU-R656 Data B Input 1
CI0	80	87	A1	I	-	-	Chrominance Data Input 0 / ITU-R656 Data B Input 0 [LSB]
NC	-	88	A2		-	down	No Connect

3. FUNCTIONAL BLOCK DIAGRAM

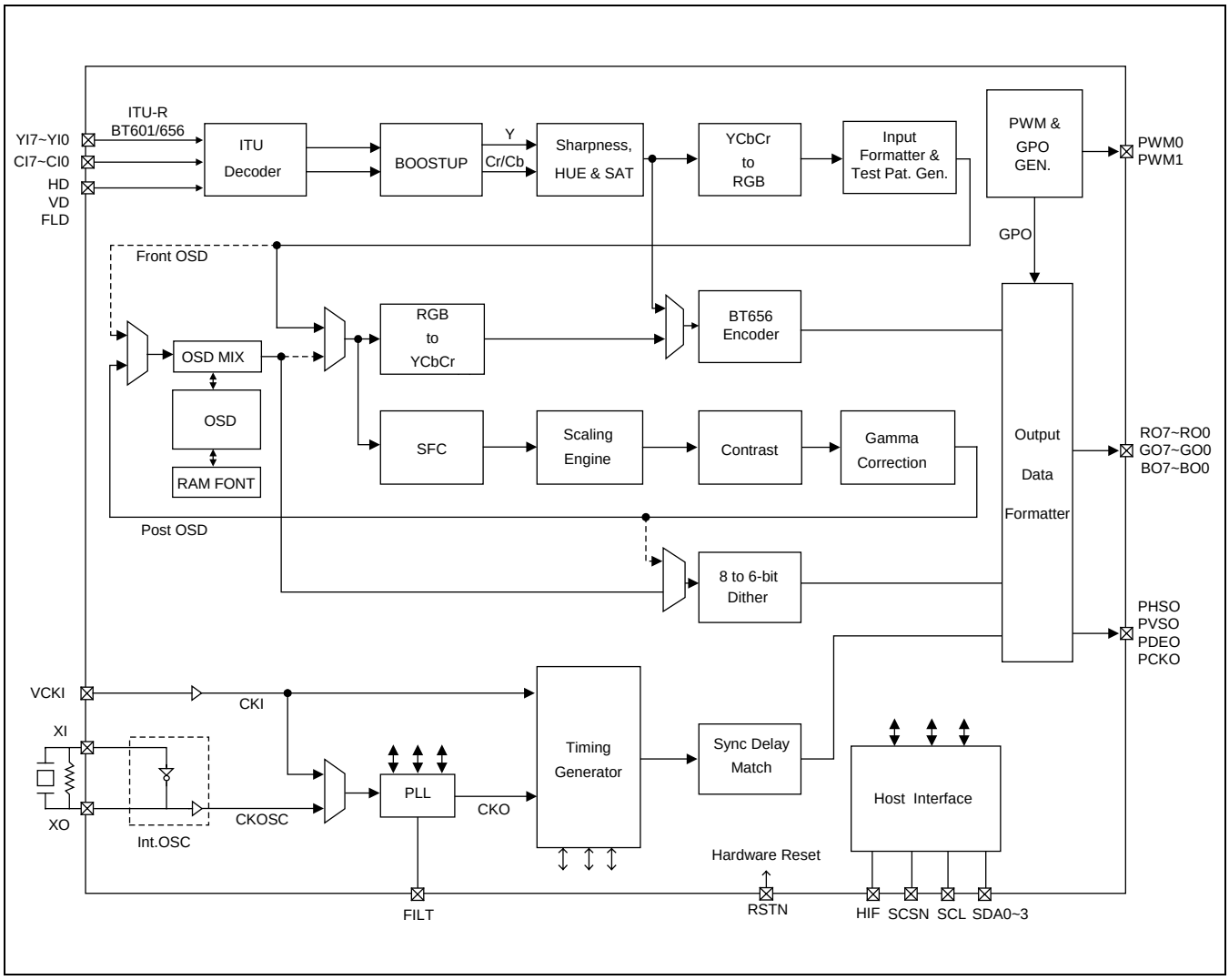


Figure 4. Functional Block Diagram

4. SOLUTION CIRCUIT FOR APPLICATION

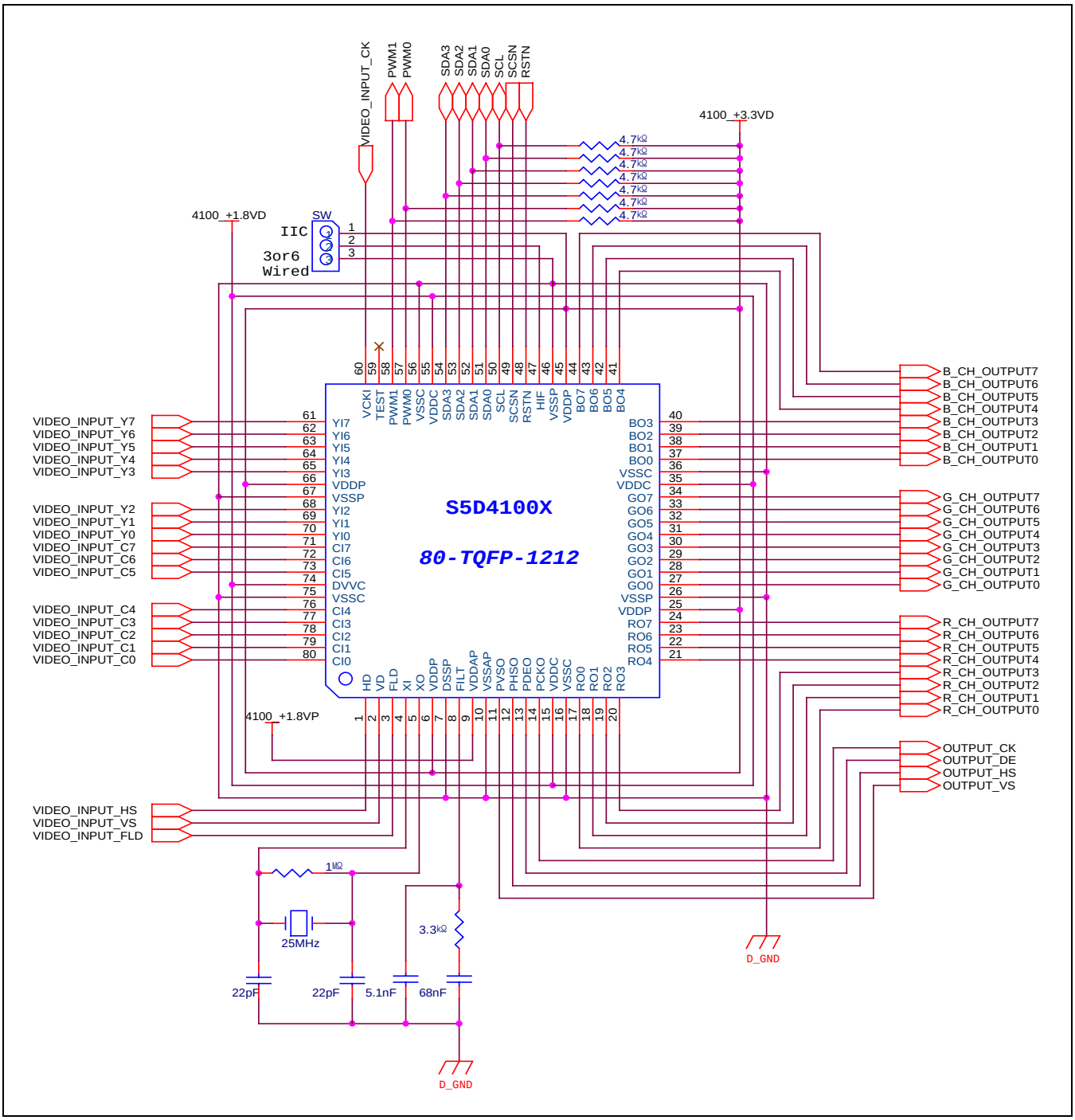


Figure 5. Solution Circuit for Application (TQFP)

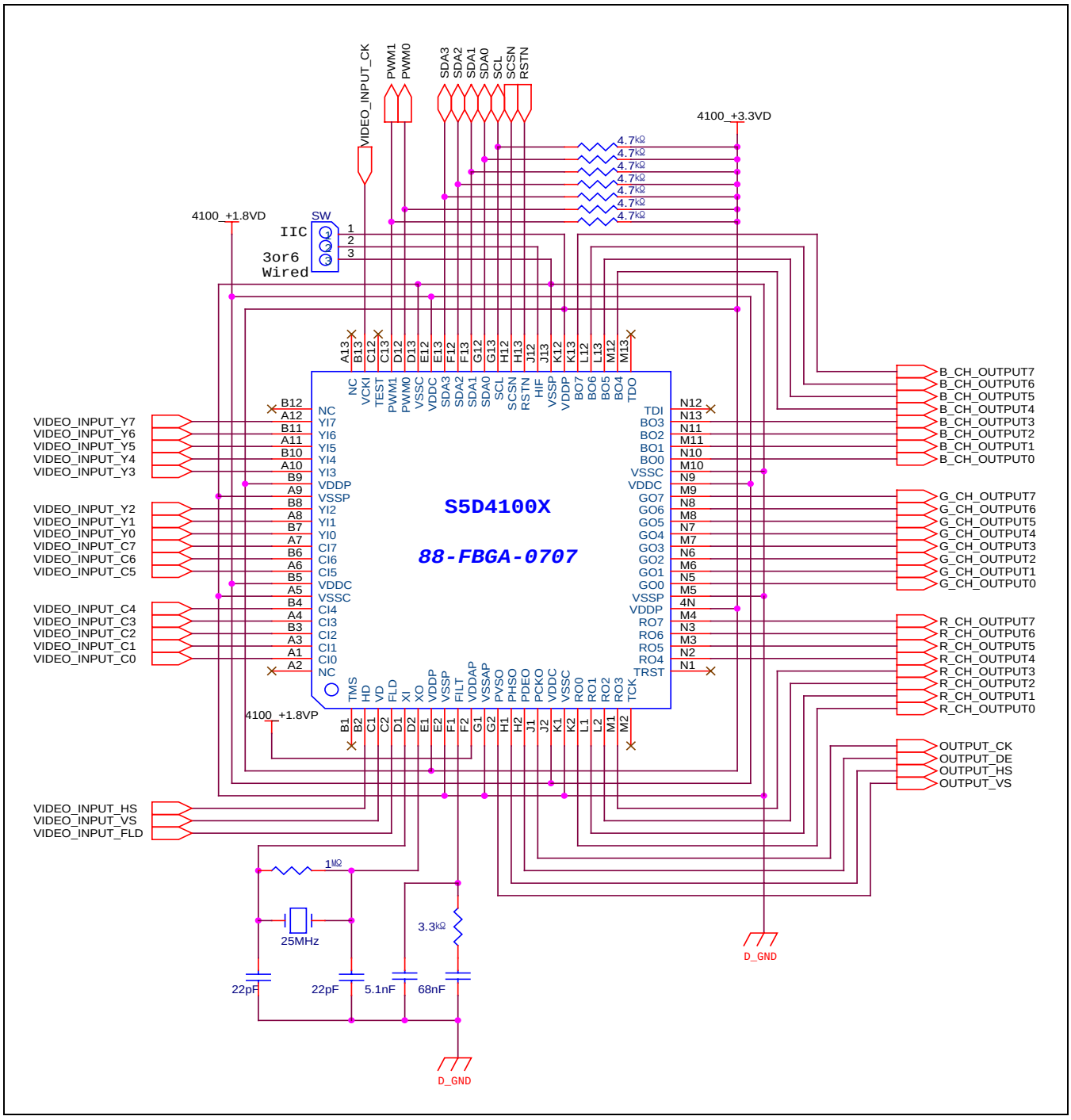


Figure 6. Solution Circuit for Application (FBGA)

5. FUNCTIONAL DESCRIPTION

5.1 CLOCK SYSTEMS

Figure 7 shows the names of the clocks used in each block of S5D4100X and the registers that affect them. As illustrated in the following system diagram, each block is designed to enable the user to switch on/off clocks at his/her need. For example, in order to activate the scaler, the clock is supplied only when Register GBI_ON, SC_ON, and GBO_ON are HIGH. Register ENC_ON, Register BU_ON and Register OSD_ON should be HIGH to enable ITU-R656 format output, BOOST-UP function and OSD menu function, respectively. In this manner, the system is configured to minimize power consumption in the portable devices which are the main applications.

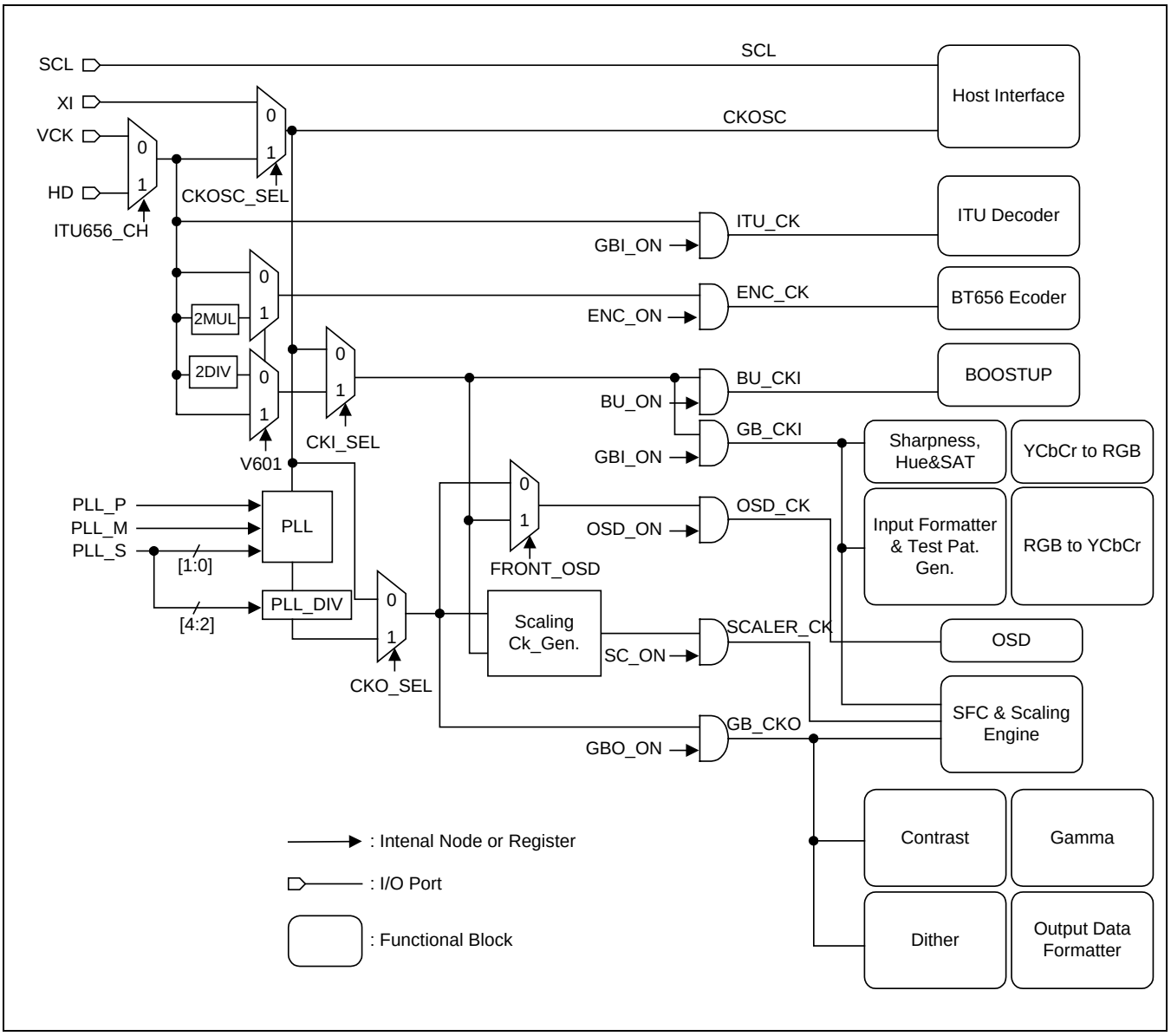


Figure 7. Clock Systems

5.2 ITU DECODER

The ITU decoder block divides Y, C and sync signal from the BT656 data via decoding of the input data in accordance with the protocol.

For BT656 input image, the ITU decoder block selects two channels alternatively. If the value of Register ITU656_CH is LOW, pins YI7 ~ YI0 are used for BT656 data, VCKI for input clock, and VD for input vertical sync signal. On the contrary, if the value of Register ITU656_CH is HIGH, pins CI7 ~ CI0 are used for BT656 data, HD for input clock, and FLD for input vertical sync signal. In other words, for ITU-R BT656, two input sources are used selectively for image by alternating channels.

For ITU-R BT601 input, the ITU decoder block simply multiplexes the data and the sync signal.

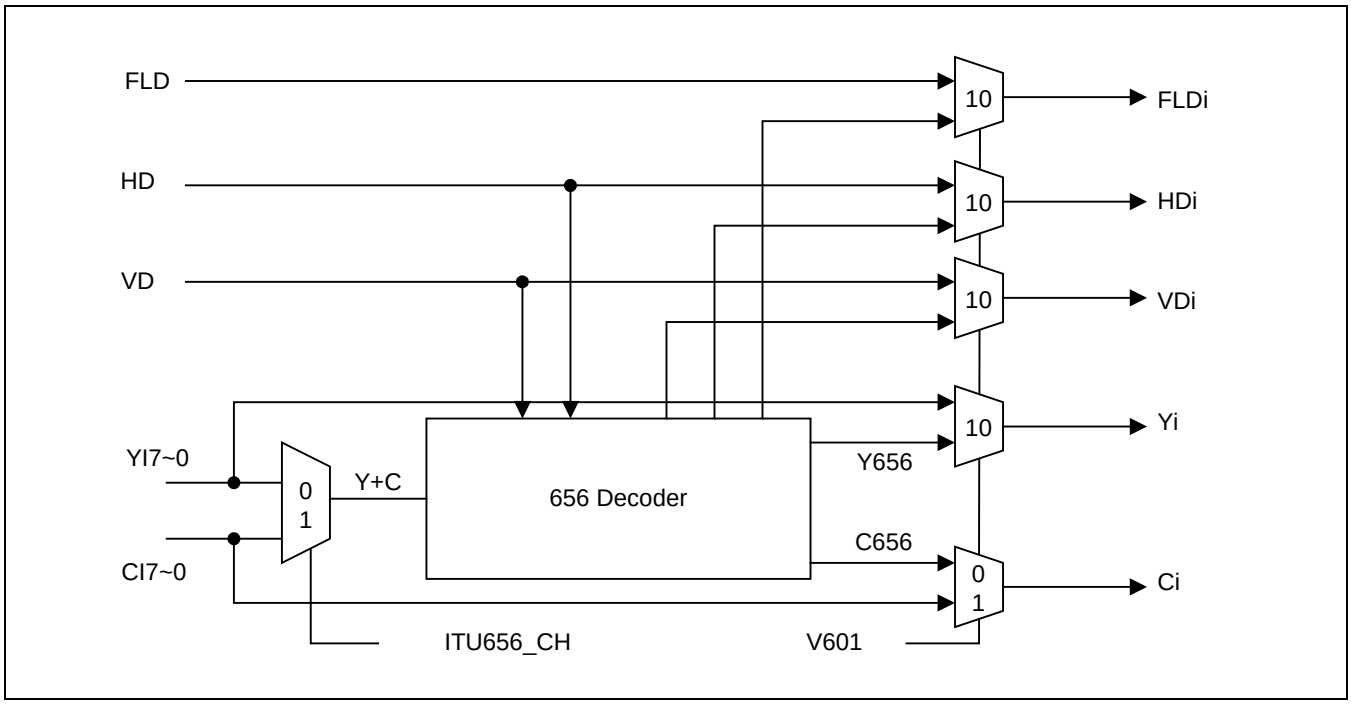


Figure 8. ITU Decoder

5.3 BOOST-UP

The BOOST-UP block performs image enhancement so that the image can be seen more clearly. Main functions of image boost-up are as follows.

5.3.1 Adaptive Contrast Control

This function makes a certain area or the entire area of the screen clearer. This is achieved as the block sorts out the colors being displayed on the screen, finds the maximum and the minimum value, and displays the image with the colors calculated adaptively through the contrast control processing.

5.3.2 Adaptive Brightness Control

This function makes the screen brighter in accordance with the LUT value. As shown in Figure 9, LUT is a value between 0 ~ 255, and maps input/output in 1:1 ratio. The size of the curve A configured in accordance with input/output mapping varies adaptively in accordance with the brightness of the screen. Point B is the inflection point of the curve which should be set by the turning point Register (TURN_POINT). All the values of LUT should be set to the size of the absolute value. The values in the area lower than Register TURN_POINT (Area C) are automatically calculated as the negative values.

5.3.3 Boost Up Calculation Area

The Boost-Up block reflects the previous screen status in the current screen. The area in which the screen status is judged becomes the calculation area. The screen is divided into the calculation area and the reflected area in order to prevent the screen from being affected by other data such as caption dialog than the actual video image.

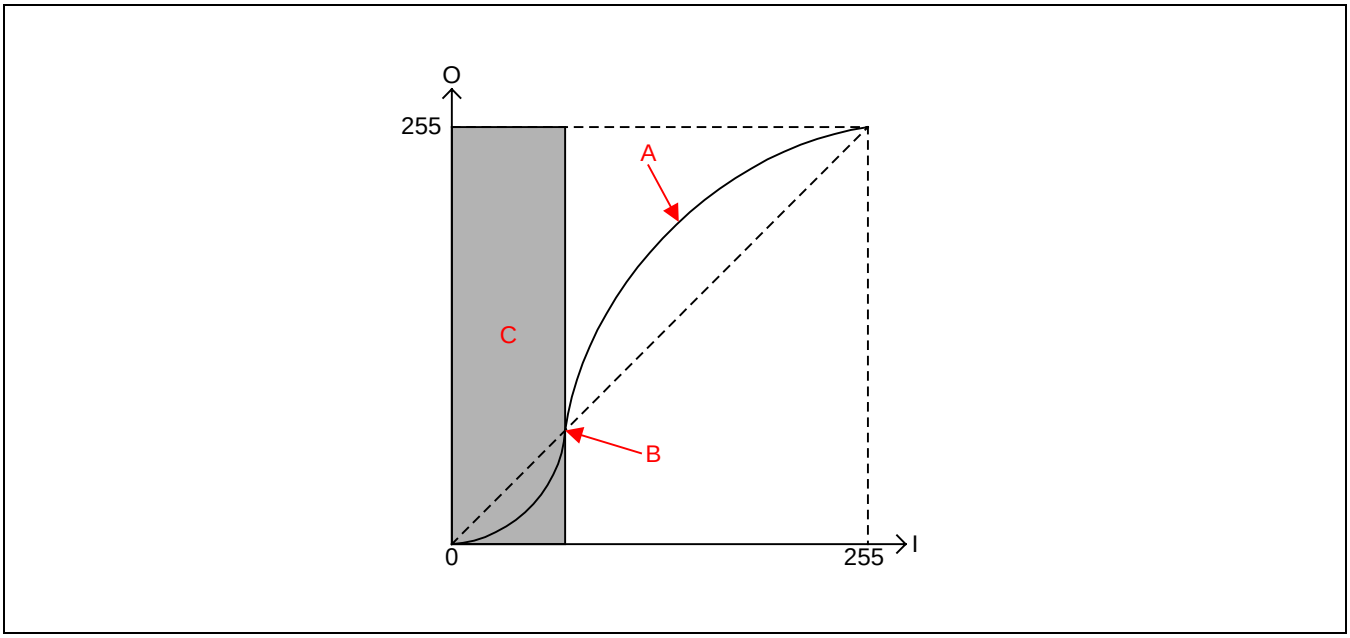


Figure 9. Adaptive Brightness Control LUT

5.4 SHARPNESS, HUE & SAT

5.4.1 Sharpness

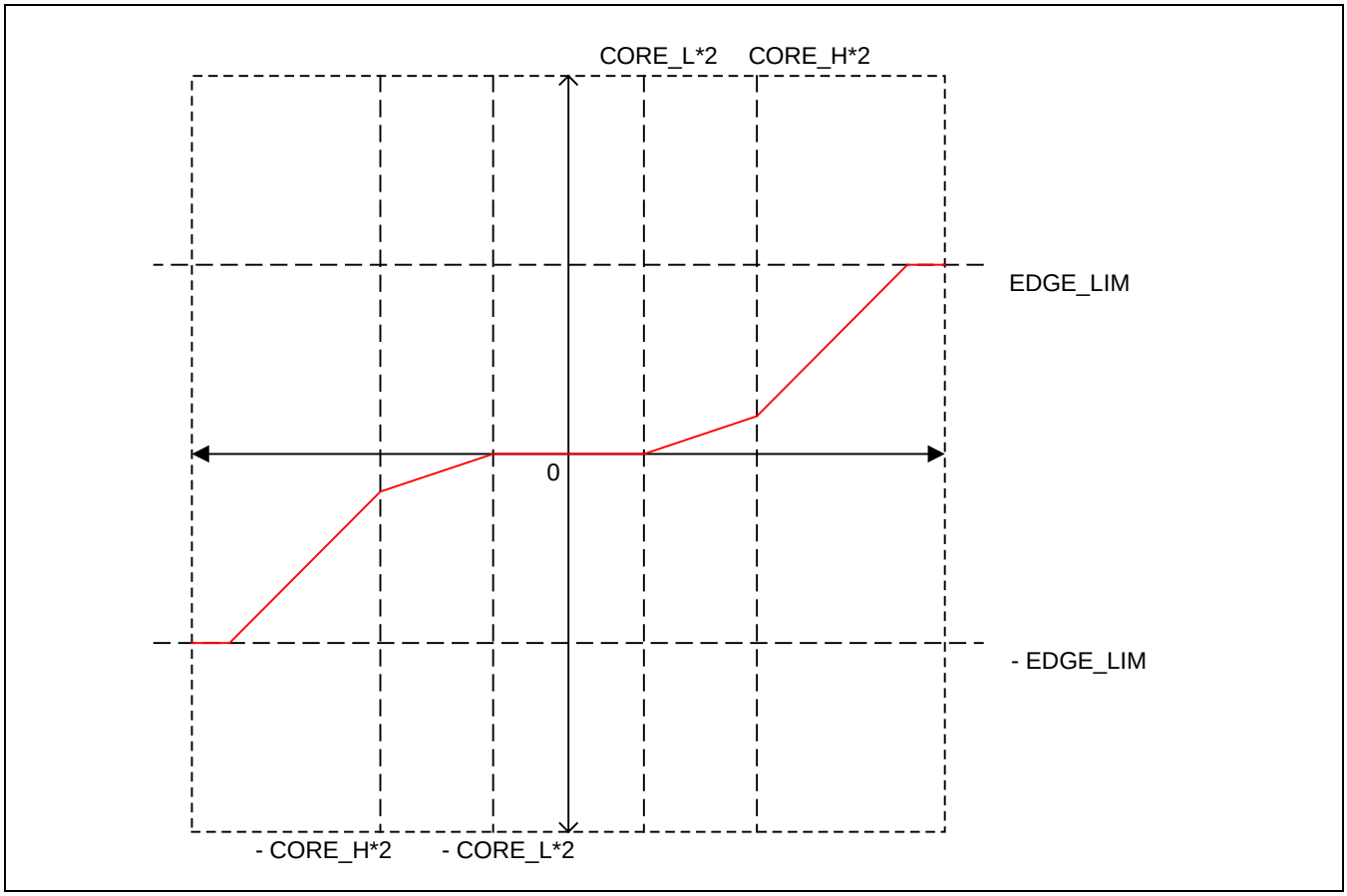


Figure 10. Sharpness I/O Characteristic Curve

The Sharpness block applies "0" for any value smaller than two times of Register CORE_L shown in Figure 10, applies a certain gradient for the value smaller than two times of Register CORE_H, and bypasses edge value for the area bigger than two times of Register Core_H. Any value which is bigger than Register EDGE_LIM is limited to Register EDGE_LIM. The gradient between Register CORE_L and Register CORE_H is determined by Register CORE_RATE; 1/2, 1/4, 1/8 and 1/16 for 00, 01, 10 and 11, respectively.

BLACK/BRIGHTNESS/CONTRAST can be adjusted as following, after EDGE is reflected.

YOUT = (YIN – YCP_BLACK) * YCP_CONTRAST + YCP_BRIGHTNESS

Where, Register YCP_BRIGHTNESS is a 2's complement, and can be a negative number.

5.4.2 HUE & SAT

Register HUE can be adjusted between -180 degree and +180 degree. The value can be a 2's complement between -512 and +511. Register SATURATION is applied after adjustment of Register HUE.

5.5 INPUT FORMATTER & TEST PAT. GEN.

5.5.1 Input Formatter

The Input Formatter block transforms the input data into the format appropriate for SFC. The block generates input sync, and adjusts Vsync delay of the odd/even field.

5.5.2 Test Pat. Gen.

The Test Pat. Gen. block generates a pattern for sync and test without input sync and data, and uses it as the input for SFC. In order to use the test data of the Test Pat. Gen. block, Register TEST_PAT_ON should be HIGH. In order to use the test sync, Register TP_SYNC_ON should be HIGH.

Figure 11 shows the internally generated sync.

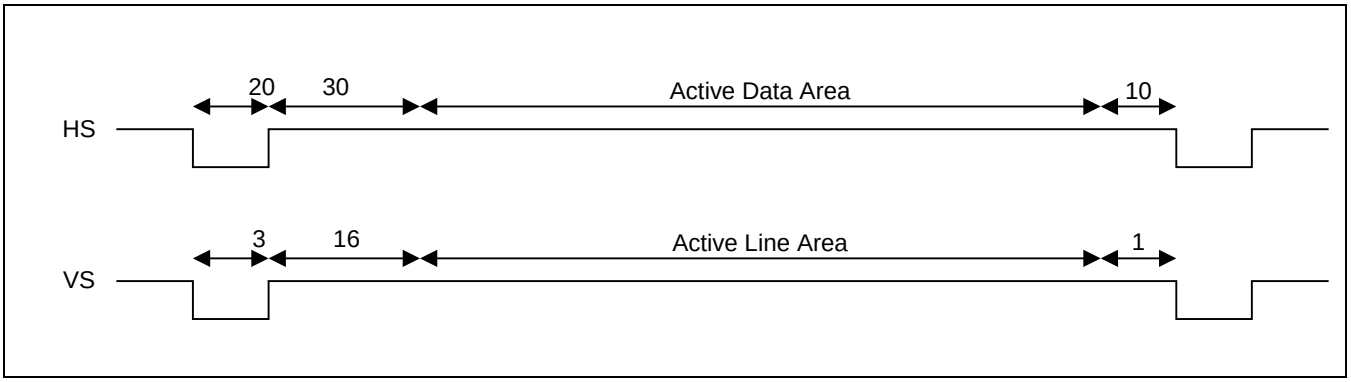


Figure 11. Test Sync

The active data area and the active line area are as specified in Registers HIAS and VIAS.

The pattern to be used as the input data for SFC is selected by Register TP_SEL. The image is passed if Bit [7] is 0, and inverted if it is 1. Bit [5] is used to select direction (H/V) of the pattern. Bits [4] ~ [0] are used to select type of the pattern. The following figure summarizes the above description.

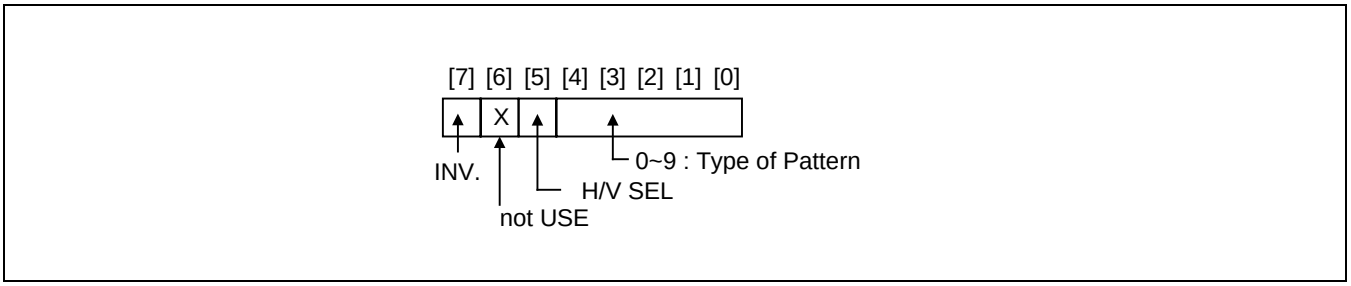


Figure 12. TP_SEL Register

Types of pattern selected by Bits [4] ~ [0] are as follows.

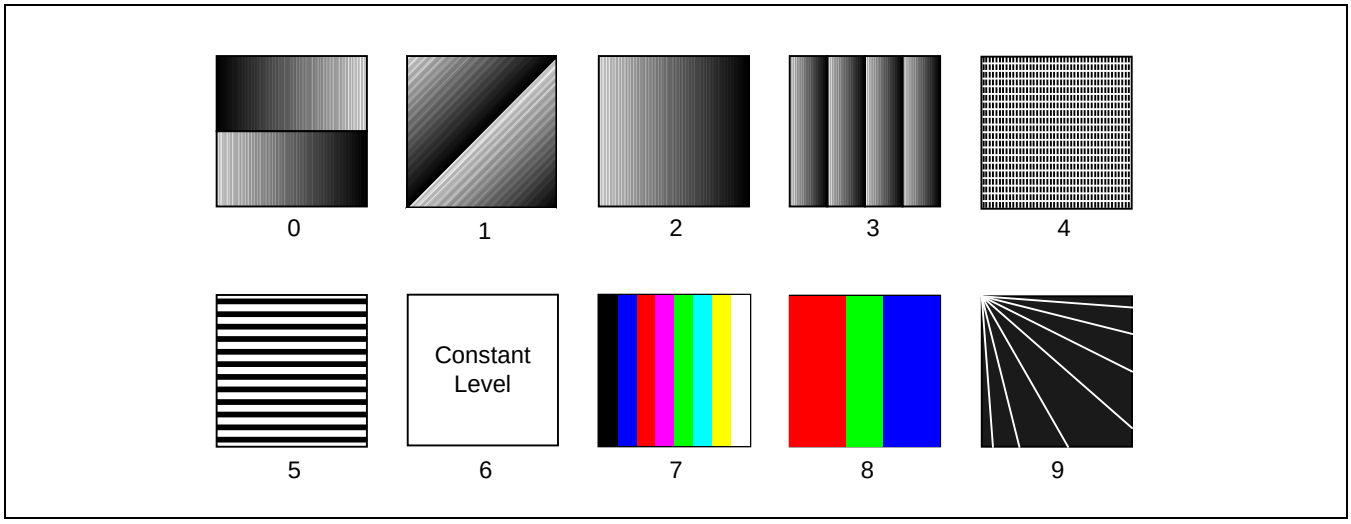


Figure 13. Types of Pattern

Pattern No 6, Constant level in the above figure is decided depending on the Register TP_CONST_LEVEL and TP_CONST_WIDTH. If Register TP_CONST_WIDTH is 0, the value set in Register TP_CONST_LEVEL is displayed. If Register TP_CONST_WIDTH is other than 0, starting at the value set in Register TP_CONST_LEVEL, the number of pixels in Register TP_CONST_WIDTH is counted from left to right in the screen, and then, at the TP_CONST_LEVEL +1, the pixels set in Register TP_CONST_WIDTH is displayed. In other words, the screen is displayed as shown in the following figure.

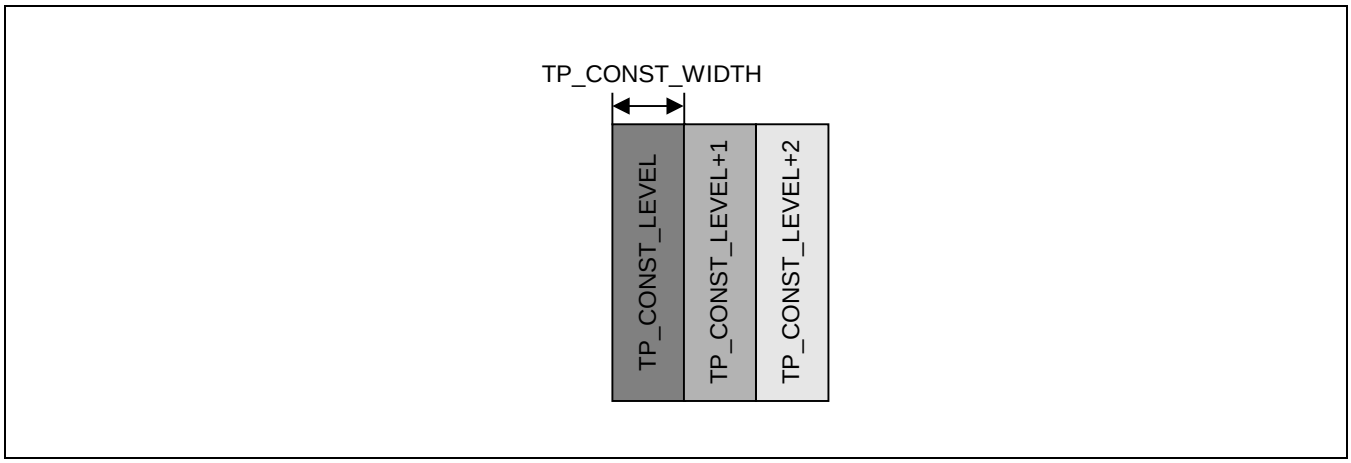


Figure 14. Pattern 6 (Constant Level)

In case of other registers related to the Test Pat. Gen. block, if Register TP_YUV_ON is HIGH, the display of the Test Pat. Gen. block is sent to the BOOST-UP block. This is the flow to test the BOOST-UP block, and is not used in general screen test. Register TP_RGB_ON consists of R, G and B by 2 bits from front (Y, Cb and Cr if Register TP_YUV_ON is HIGH). The following table shows the display ratio.

Table 1. Test Pattern Display Ratio

R/G/B	00	01	10	11
Display ratio	0%	25%	50%	100%

5.6 BT656 ENCODER

The BT656 encoder outputs the ITU-R656 data via the pins BO0 ~ BO7 when Register SERIAL_ON and Register ENC_ON are HIGH. The encoder also outputs VCKO and VSO via GO7 and GO6.

The outputs of the BT656 encoder are determined in accordance with the Register EN_656OUTSEL values as shown in the following table.

Table 2. Encoder Output

EN_6565OUTSEL	Output
00	Input 656 data (The channel selected in accordance with Register ITU656_CH value)
01	ITU decoder output data (If Register VS_SEL is HIGH, the 656 data contains VS instead of VACT)
10	Sharpness, HUE & SAT output data
11	OSD output data if FRONT_OSD is HIGH, and input formatter output data if it is LOW.

5.7 TIMING GENERATOR

The timing generator generates the timing used in S5D4100X, and delivers the value required for PCKO (output clock). Using input HS and VS, the timing generator generates PHSO, PVSO and PDEO for output sync. The generated timing signals are sent to the internal blocks. TG also delivers the value for generation of PCKO from MCU to internal PLL.

5.7.1 Output Timing Generation

Using input HS and VS, TG generates the output sync (PHSO, PVSO and PDEN). To set the active data area in input HS and VS, values for Register HTOTAL, H_STR, HIAS, VTOTAL, V_STR and VIAS are set as shown in Figure 15. The output signals are defined with the values of Register HOFP, HOSW, HOBP, VOFP, VOSW, HOAS and VOAS.

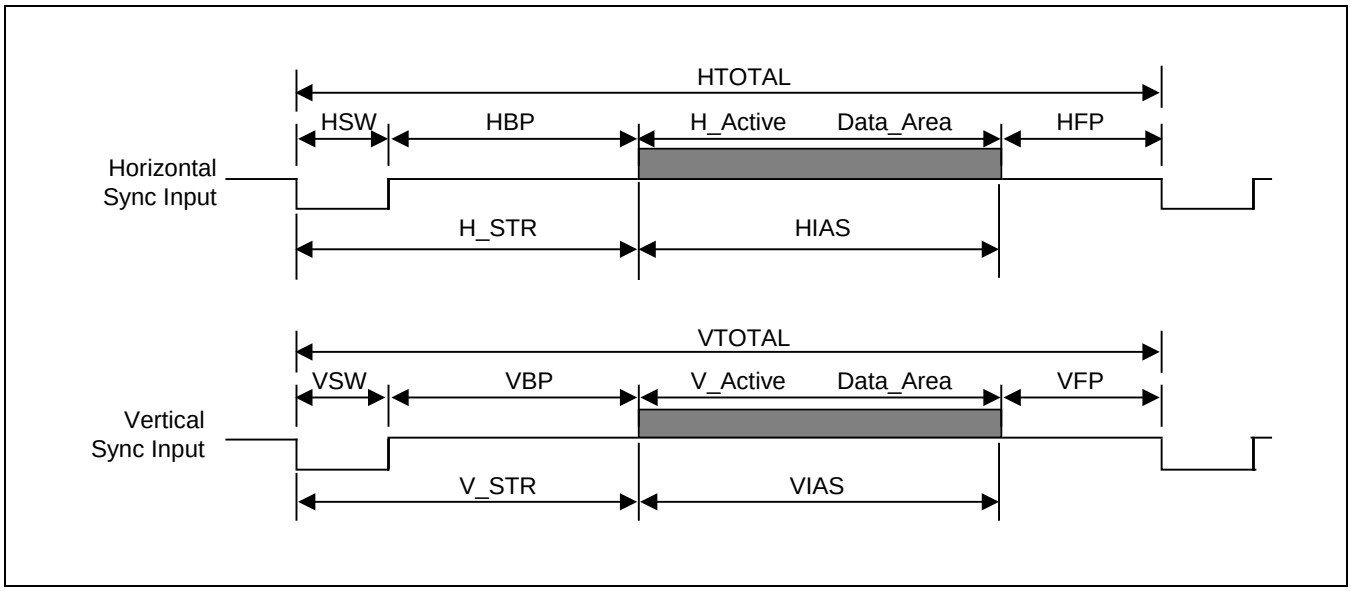


Figure 15. Input Timing

5.7.2 Output Clock Generation

S5D4100X generates output clock with PLL. Figure 16 shows the structure of PLL.

Receiving the input clock Fin from VCK or X1 pin, the Pre-Divider divides the clock, using the Register PLL_P value, and send them to PFD. PFD uses the signal received from the Pre-Divider as the reference frequency, compares the signal with the output of the main divider which is determined by the Register PLL_M value, and controls the charge pump voltage. VCO generates the output clock, and supplies the final output clock (FOUT) via Post Scaler1 and Post Scaler2. The signal is divided for lower 2 bits of Register PLL_S for Post Scaler1, and upper 3 bits of Register PLL_S for Post Scaler2.

The frequency of FOUT is calculated as:

$$FOUT = Fin * (Pll\_M+1) / (PLL\_P * 2^{S})$$

Where,

$$S = PLL\_S[4:2] + PLL\_S[1:0].$$

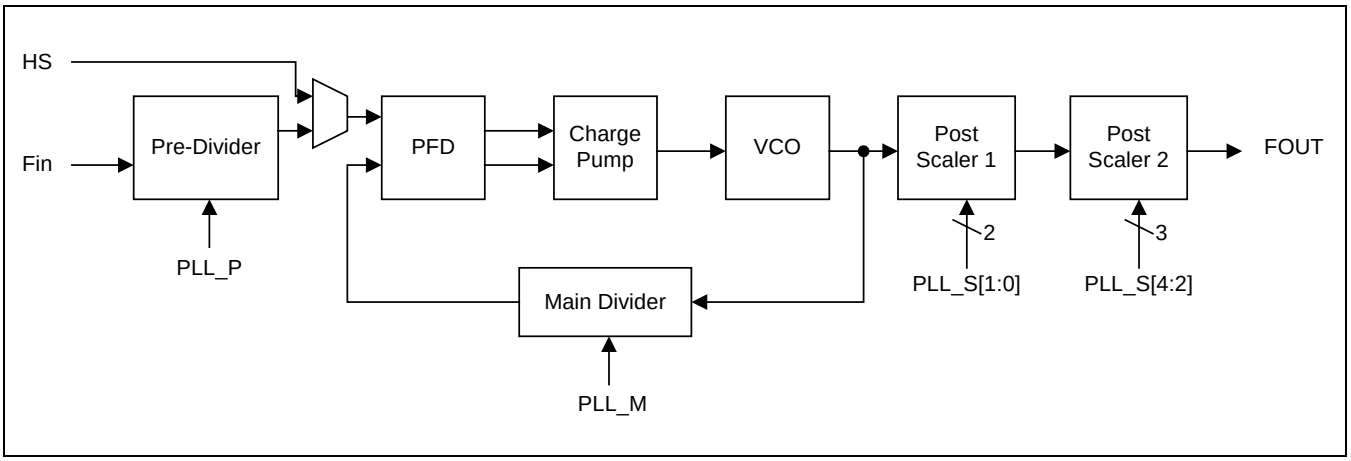


Figure 16. Structure of Frequency Synthesized PLL

5.8 SCALER

The scaler of S5D4100X runs in the following 4 image scaling modes. (1:1 mode is Scale Up.)

5.8.1 HUPVUP (Horizontal-Scale-Up, Vertical-Scale-Up)

For ITU-R.656/601 input, the scaler guarantees clock speed of 80MHz to XGA output. The scaler supports scale-up of up to 1024 pixels in horizontal direction, and up to 768 lines in vertical direction. The scaler supports scale-up at different ratio in H/V direction respectively.

5.8.2 HDNVDN (Horizontal-Scale-Down, Vertical-Scale-Down)

For ITU-R.656/601 input, the scaler supports scale-down to 1/2 size. For NT input, the scaler supports scale-down of up to 360 pixels in the horizontal direction, and up to 120 lines in the vertical direction. The scaler supports scale-up at different ratio in H/V direction respectively.

5.8.3 HUPVDN (Horizontal-Scale-Up, Vertical-Scale-Down)

For ITU-R.656/601 input, the scaler supports scale-up of up to 1024 pixels in the horizontal direction, and scale-down of up to 1/2 in the vertical direction. For NT input, the scaler supports scale-up of up to 1024 pixels in the horizontal direction and scale-down of up to 120 lines in the vertical direction.

5.8.4 HDNVUP (Horizontal-Scale-Down, Vertical-Scale-Up)

For ITU-R.656/601 input, the scaler supports scale-down of up to 1/2 in the horizontal direction, and scale-up of up to 768 lines in the vertical direction. For NT input, the scaler supports scale-down of up to 360 pixels in the horizontal direction, and scale-up of up to 768 lines in the vertical direction.

5.9 OSD (ON-SCREEN DISPLAY)

OSD stores the Font RAM address and the font features in the Display RAM, displays the font and its features in the designated location, and displays the features designated in OSD register on the screen.

5.9.1 FONT

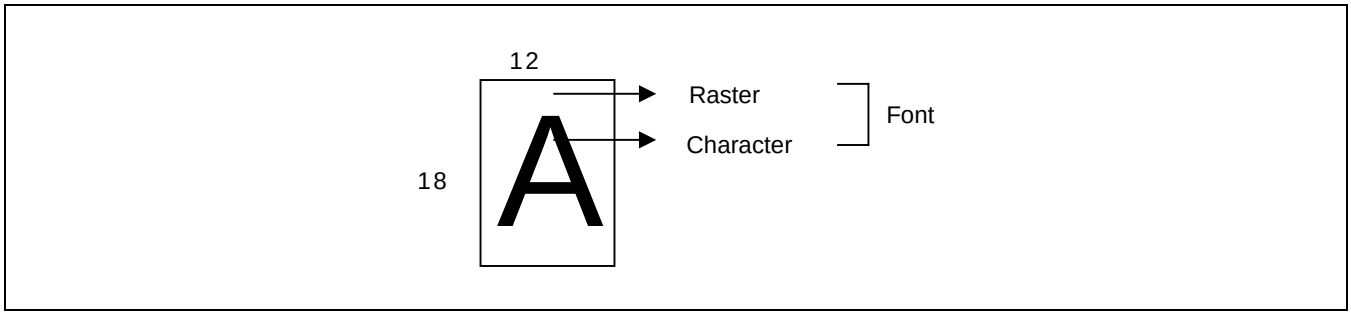


Figure 17. OSD Font Structure

OSD font is configured with 12*18 (W*L) pixels, and is divided into character and raster when displayed on the screen. Font color can be controlled with FC of Display RAM, and a font has 16 kinds of character color and 16 kinds of raster colors. FC value is used as the reference of LUT for controlling of character and raster.

5.9.2 LUT (Look Up Table) Control

The user can assign a bit to Register LUT0 ~ LUT15, and the color is displays in reference to the color elements of the values.

For font color (Register FC), if Register FC == 3, LUT3 is assigned to the font, and hence, the character color has R= LUT3[7] , G= LUT3[6:5] and B= LUT3[4], and the raster color has R= LUT3[3], G= LUT3[2:1], B= LUT3[0].

For Character Border/Shadow Color (Register CH_BSC), R= LUTn[7] , G= LUTn[6:5] and B= LUTn[4] are assigned (n = 0 ~ 15).

For MCF Color, R= LUTn[7], G= LUTn[6:5] and B= LUTn[4] are assigned (n = 0 ~ 7), and in this case, Register CH_BSC is available for LUT0 ~LUT7 only.

5.9.3 User Definable OSD Region

OSD region is defined by the number of OSD horizontal fonts and the number of OSD vertical fonts to be displayed on the screen by Register OSD_HFONT[6:0] and Register OSD_VFONT[5:0].
Since 7 bits and 6 bits are assigned for Register OSD_HFONT and Register OSD_VFONT, respectively, the maximum fonts displayed are 127 in horizontal direction and 63 in vertical direction.
Since the number of horizontal/vertical pixels of the minimum font is 12/18, the maximum pixels displayed in horizontal/vertical direction are 1524/1134 pixels.

Because the maximum size of the display RAM is 450 * 2 (Display Ram attribute is 2 byte size), OSD_HFONT * OSD_VFONT <= 450 must be fulfilled.
If Register OSD_HFONT is 30 and Register OSD_VFONT is 10, the OSD region is as in the following figure. In this case, the Display RAM uses addresses from 0x2000 to 0x2257 for display.

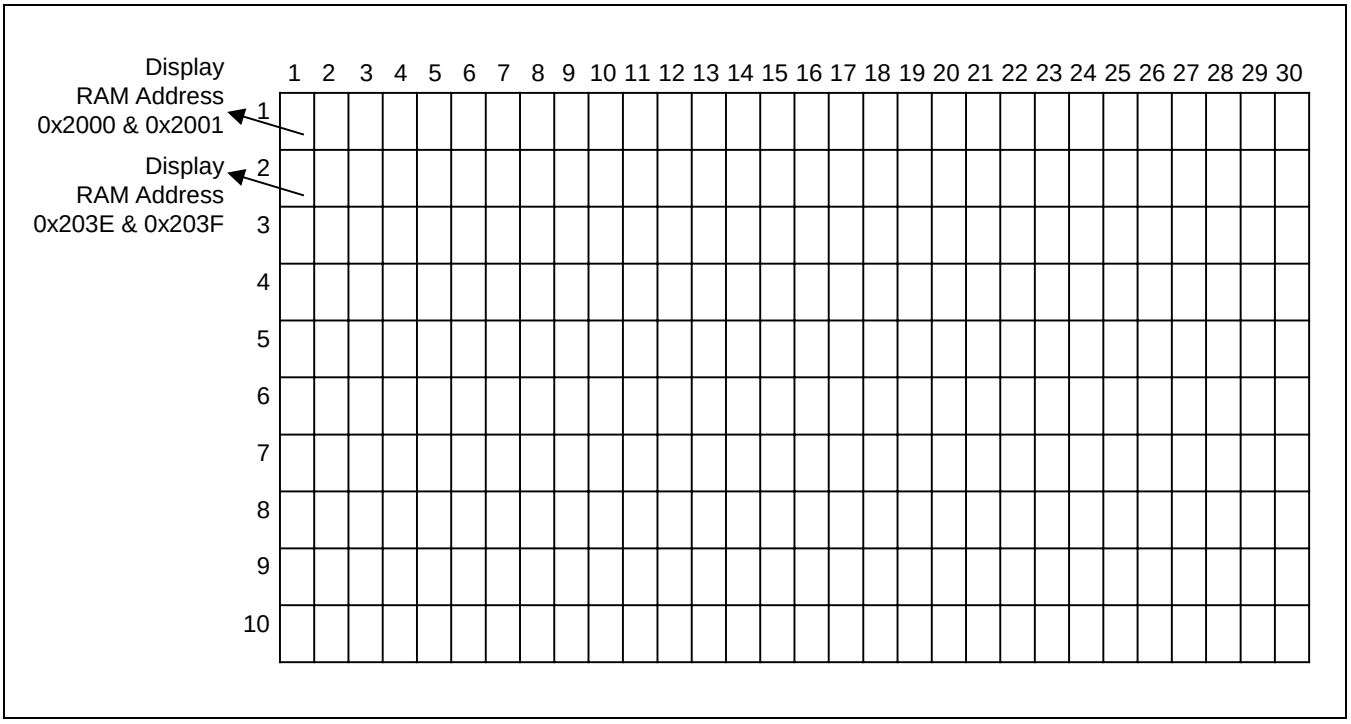


Figure 18. OSD DISPLAY RAM Structure

5.9.4 OSD Position

Start point of OSD can be changed via controlling of Register OSD_HSP and Register OSD_VSP.

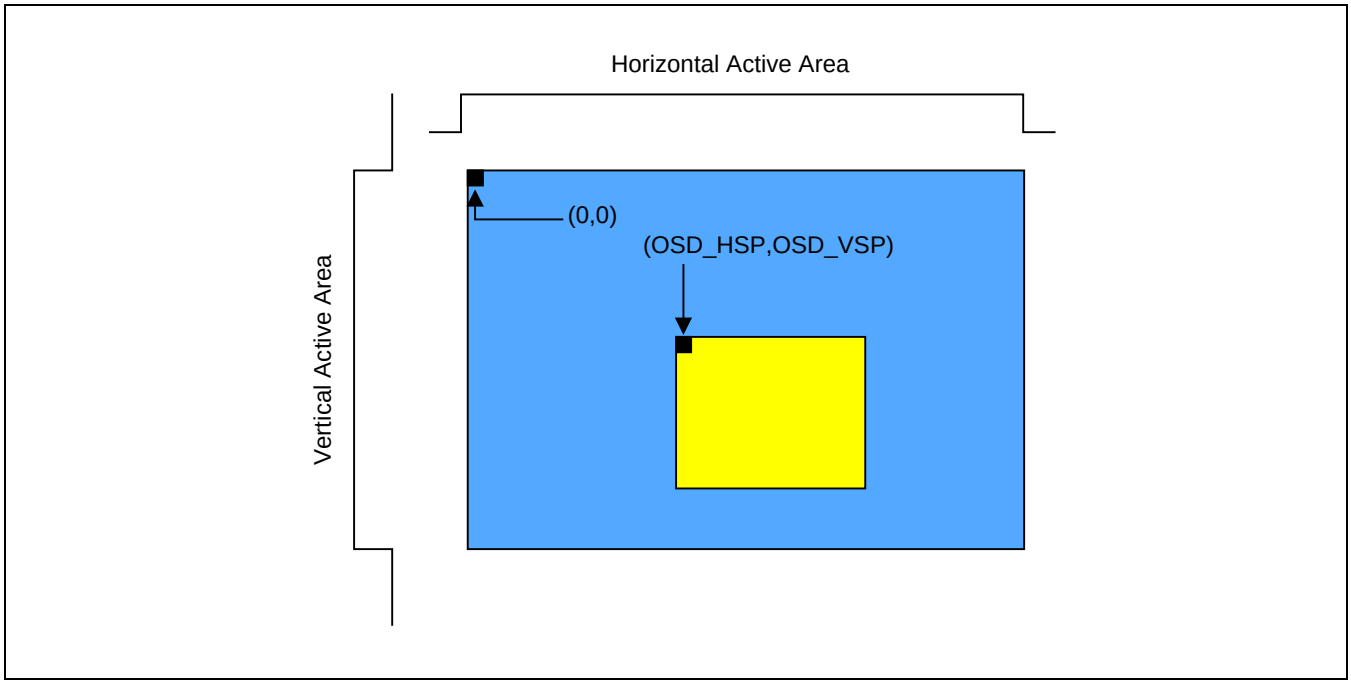


Figure 19. OSD Position

5.9.5 Adjustment of Font Size

OSD font is stored on the Font RAM with 12 bits in a line, and is displayed in a 12*18 font via 18 accesses and displays in total.

Horizontal/vertical size of a font can be enlarged to 1, 2, 3 and 4 times via adjustment of Register CH_HSZ and Register CH_VSZ. For example, 4 x Register CH_HSZ and 2 x OSD_VSZ will make the OSD font size 48*36.

In this case, for 1 pixel of font data, the same data are displayed 4 times in horizontal direction and 2 times in vertical direction.

Therefore, if Register CH_HSZ and Register CH_VSZ are changed, the OSD window size displayed on the screen is also changed.

5.9.6 Character Border/Shadow

The character border/shadow of a font is implemented as G_BDSH_EN of OSD Register is HIGH, Register CH_BDSH_EN of each character of Display RAM is HIGH, and Register BDSH_SEL is 1 or 0 (1: Border, 0: Shadow).

If Register BDSH_TYPE_SEL (0x0108[7]) = 0, the size of border/shadow is decided in connection with the font size (Register CH_HSZ, Register CH_VSZ). For example, if Register CH_HSZ is 0, the character border/shadow is displayed by 1 pixel, and if Register CH_HSZ is 2, the character border/shadow is displayed in the thickness of 3 pixels.

If Register BDSH_TYPE_SEL (0x0108[7]) = 1, regardless of the font size, the border/shadow is displayed in 1 pixel thickness.

The border/shadow color of the character is decided by Register CH_BSC, and the value given in Register CH_BSC becomes the reference of LUT.

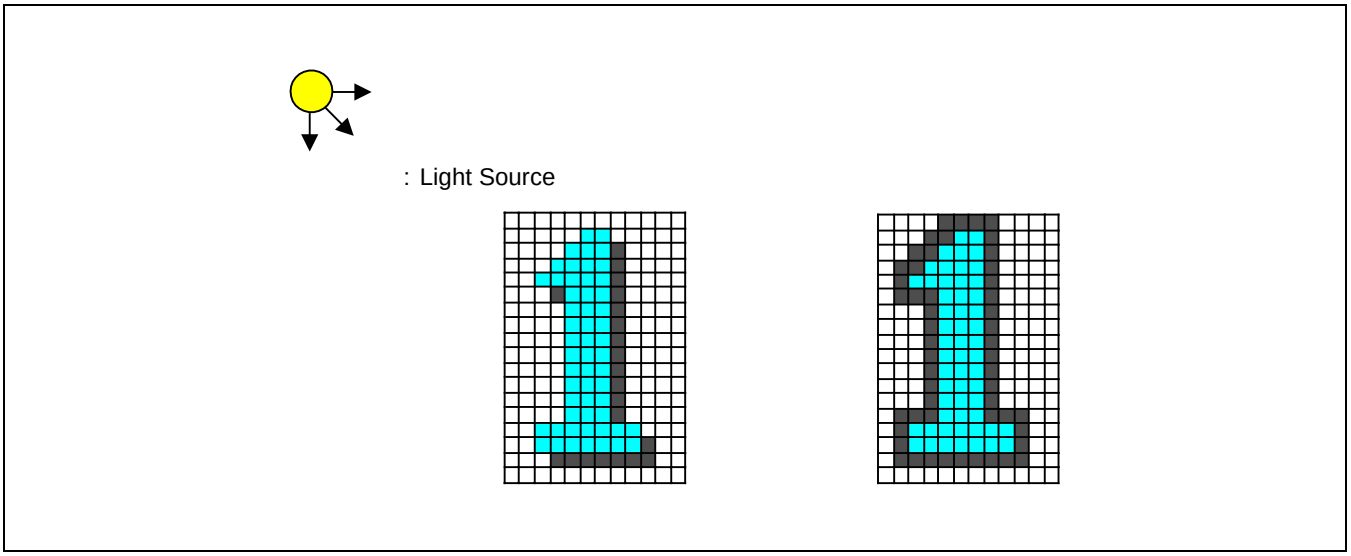


Figure 20. Board/Shadow

5.9.6.1 If there is no space on the right

The border is created on the outside of the font area along the right side of the font.
(This, however, is applied when Register BDSH_PASS (0x0108[6]) = 1.
If Register BDSH_PASS = 0, the character border/shadow is created inside the font area.)

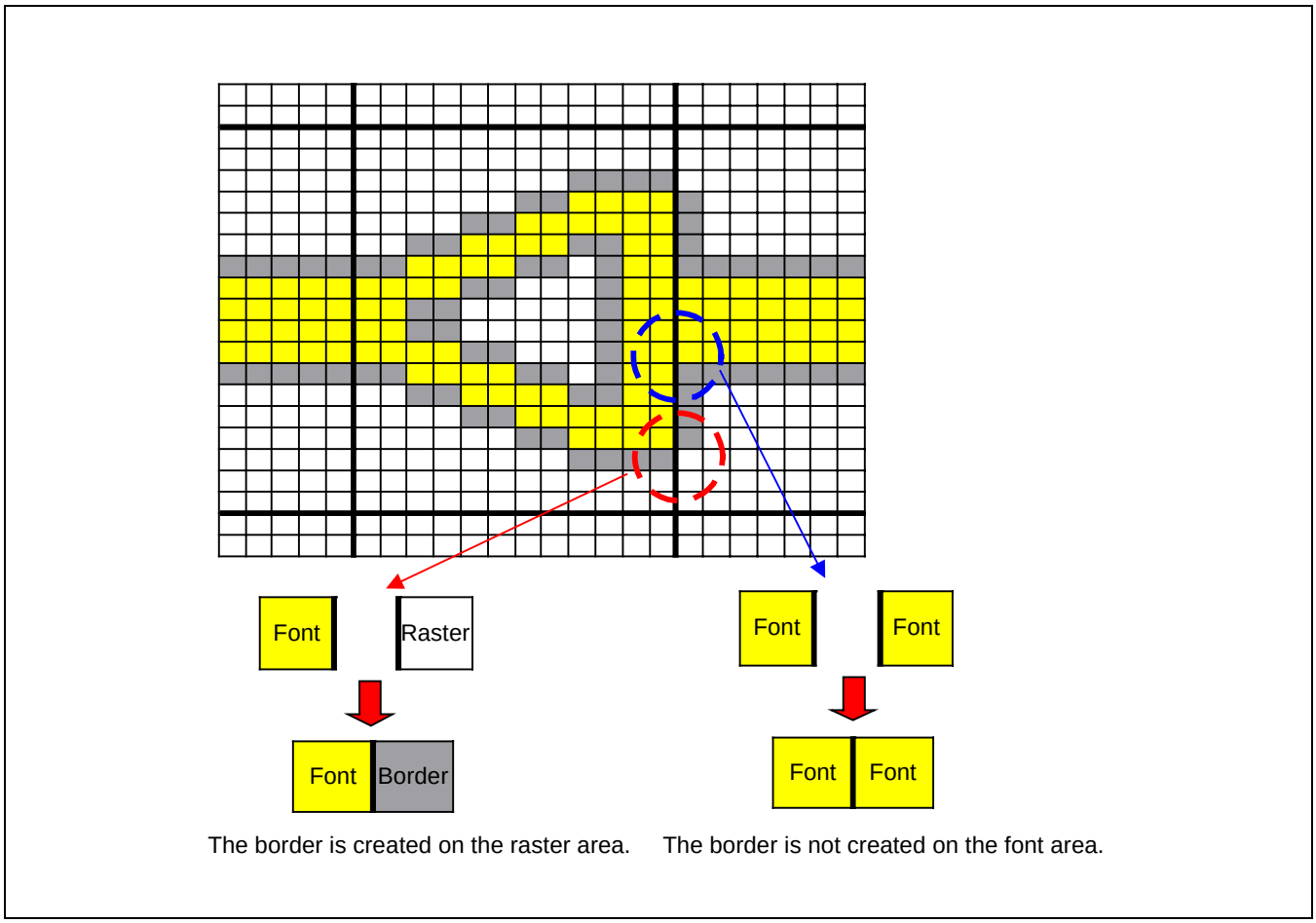


Figure 21. Creating Border When There is No Space on the Right

5.9.6.2 If there is no space on the left

No border shall be created on the left if there is no space on the left of the font.

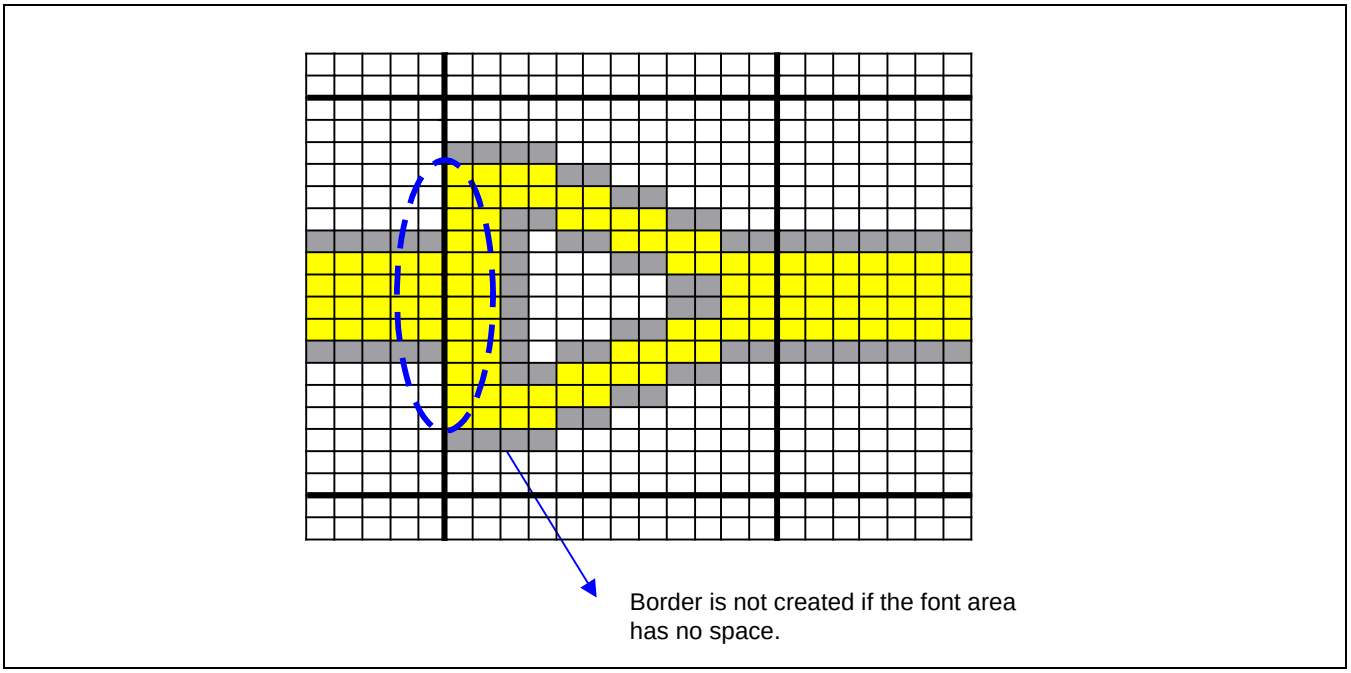


Figure 22. When there is no Space on the Left

In this case, the border can be created through modification of the font. (Shifting the entire font to the right by 1 pixel to create a space of 1 pixel on the left of the font)

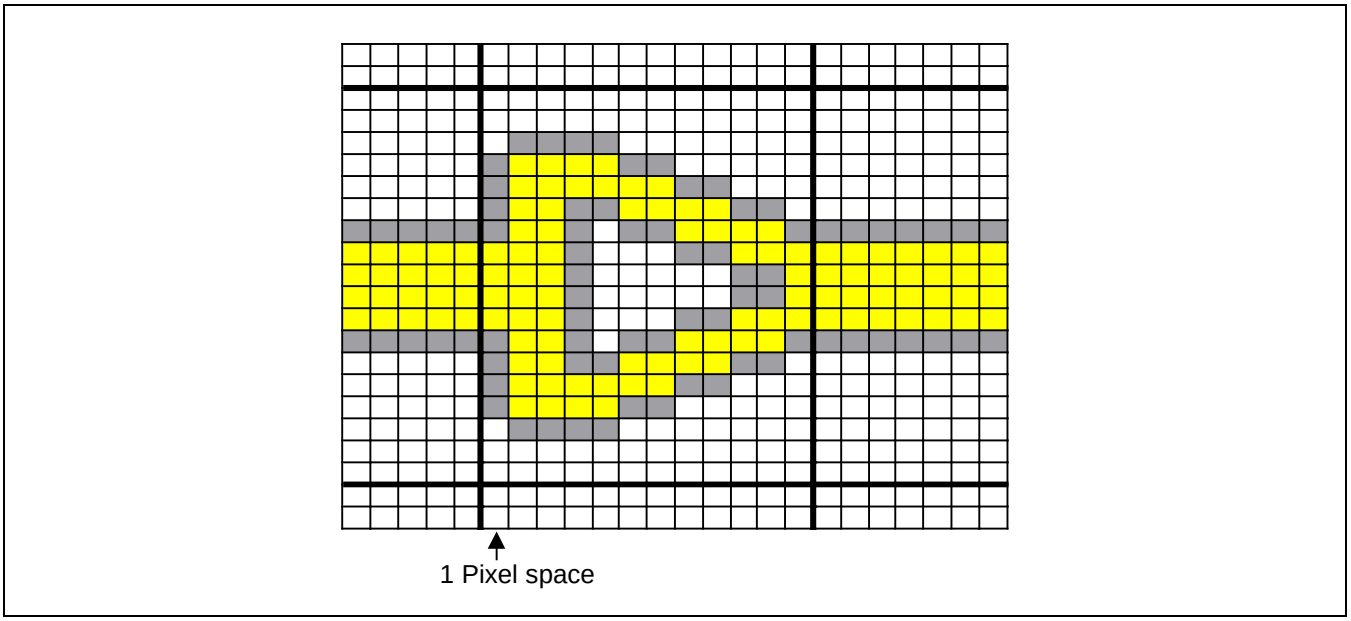


Figure 23. Creating Border on the Left Space

5.9.7 Blink Control

OSD blink function can be controlled by font.

The font blink function is enabled when Register BL_NTRA (Blink or NoTone Raster) is 1 and the Display RAM BLNK is 1 Register BLNK_SEL is used for adjustment of blink duty while the blink function is enabled.

Table 3. Blink Control

BLNK_SEL	Blink Off	Blink On
0	0.5 sec	0.5 sec
1	1 sec	0.5 sec
2	0.5 sec	1 sec
3	1 sec	1 sec
4	1.5 sec	1.5 sec
5	2 sec	1 sec
6	1 sec	2 sec
7	2 sec	2 sec

Register BLNK_C supports color inversion of the character to be blinked.

Once Register BLNK_C is set, the complementary color of the raster color of the current font is displayed on the character area during the blink off period, and if reset, the raster color is displayed.

5.9.8 Multi-Colored Font (MCF) control

OSD displays icons in multi-color. 8 (3-bit) or 4 (2-bit) multi-color fonts are available. Each multi-colored font consists of 3 colors attribute RAM fonts as shown in the following figure. The three fonts make a multi-colored font with the OR operation. Accessing a multi-colored font is performed via addressing of the first font.

MCF starts from the point of font number 1 to the point in which Register N_MCF (0x0109[6:0]) becomes tripled (MCF_SEL = 0) or doubled (MCF_SEL = 1).

If Register N_MCF is 4, font numbers 1 ~ 4 are R, 5 ~ 8 are G, and 9 ~ 12 are B-color fonts. The multi-colored font can be accessed via addressing of 1~4.

For example, if Register N_MCF is 3, and the display RAM addresses 1, MCF uses 1 for the first font, 4 for the second font, and 7 for the third font.

A pixel from each of the three fonts make a CHAR part via the OR operation. The three pixels are used as the selection [2:0] for Registers LUT1~LUT7.

If the pixels are "000", the color of Register LUT0 is recognized as the raster, rather than the color of Register LUT0, and the attribute of the first font raster color is used. In other words, one of the 16 LUTs can be selected.

If the G/B-color font is accessed instead of MCF R-color font, it is not recognized as MCF, but the Standard Font (SF) is used.

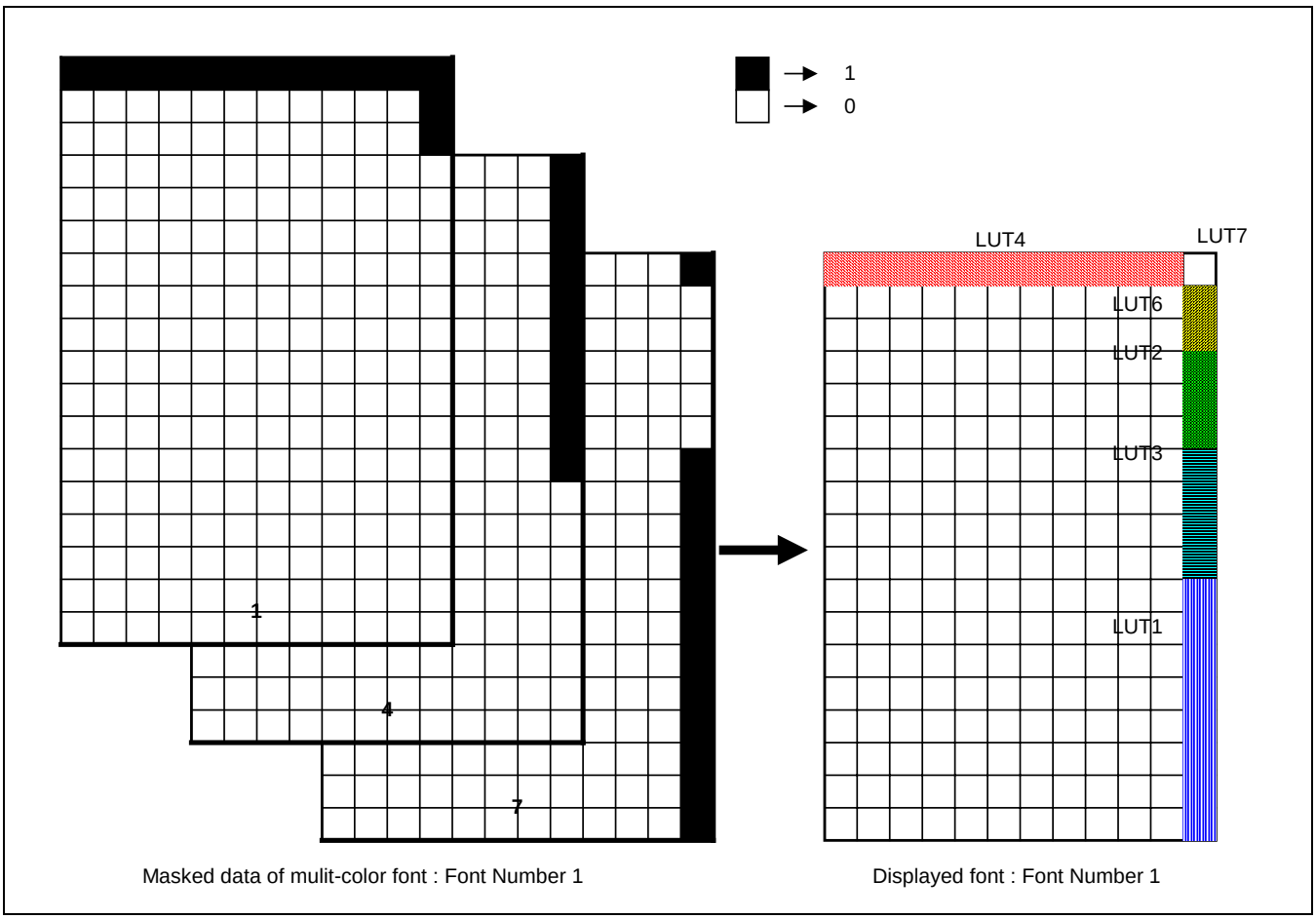


Figure 24. OSD Multicolor Font Structure

5.9.9 Blank Font Control

If DSRAM font address attribute is 8'h00, 0x4000h of FTRAM is accessed and displayed, and only the input image is displayed in the OSD region.

FTRAM 0x2000h is called as a blank font, and provides some useful function. For example, as the actual ODS window size is 30x10, the user can display this OSD window size as 20x5 by using blank fonts in the other area except 20x5.

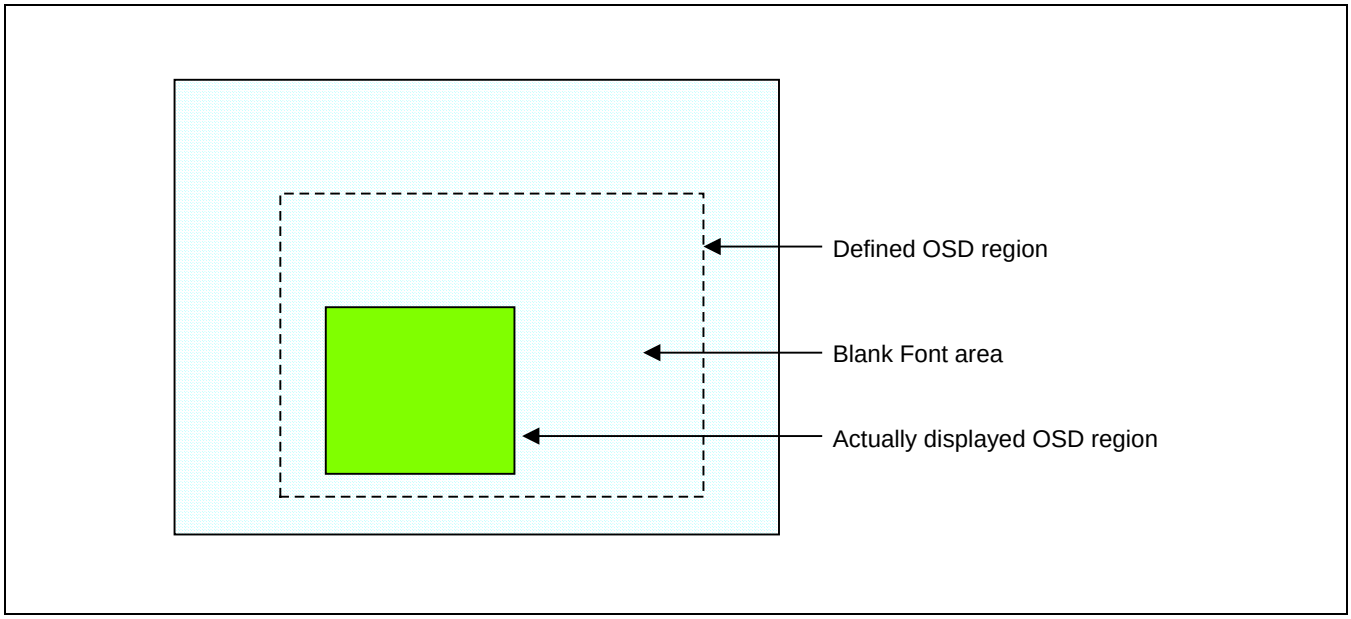


Figure 25. OSD Region Definition

5.9.10 OSD RAM

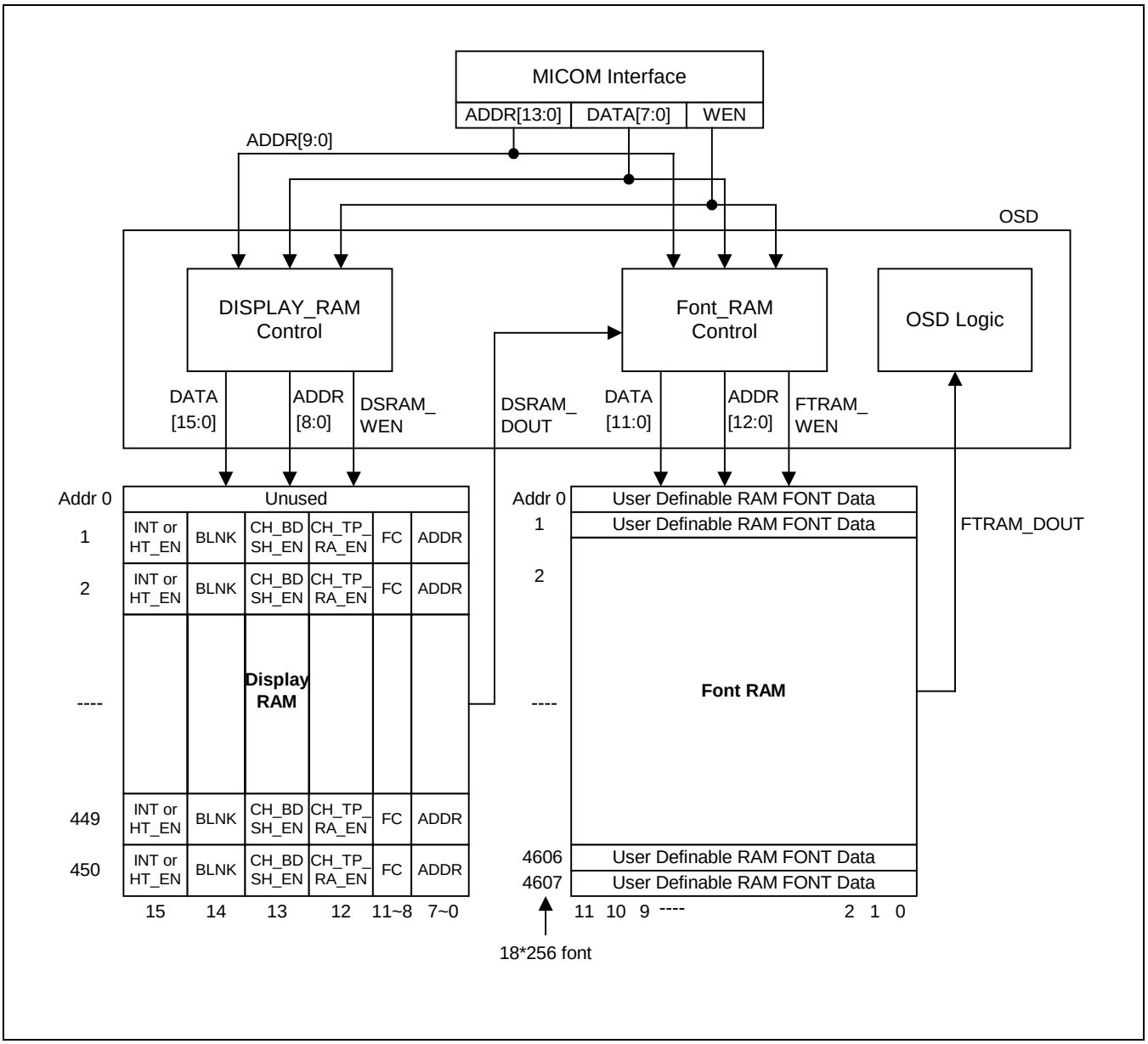


Figure 26. OSD RAM Structure

The OSD RAM is divided into the font RAM and the display RAM.
The font RAM stores 256 fonts of 12*18.
The display RAM designates the font to be displayed on the screen, and the features including color.

5.9.10.1 Font RAM Structure

The font RAM has 9216 (4608*2) addresses from 0x4000 to 0x63FF, assigning 36 addresses per font (9216/256 = 36).

Since the host interface transmits the data by 8 bits to the font RAM, in order to configure a font of 12*18 as shown in the following figure 27, an even numbered address and an odd numbered address are assigned to the upper 4 bits and the lower 8 bits of a line (12 bits), respectively.

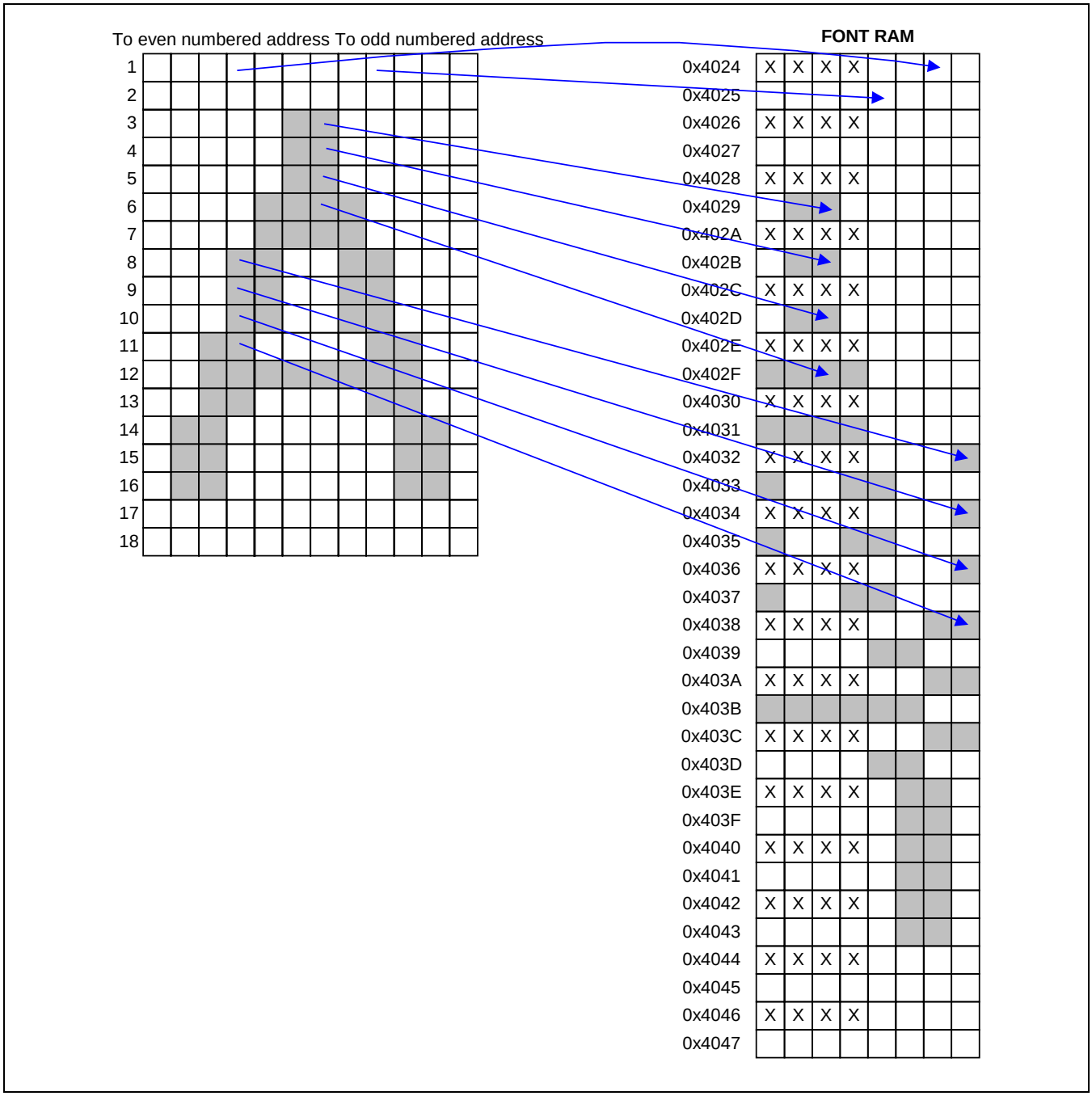


Figure 27. OSD Font Structure

5.9.10.2 Display RAM Structure

The display RAM has 900 addresses from 0x2000 to 0x2383. In other words, 2 addresses are assigned to a display RAM cell (900/450 = 2). Since the host interface transmits the data by 8 bits, in order to configure a display RAM cell of 16 bits, 2 addresses should be transmitted. A display RAM cell is composed as below. In case of a display Ram cell [15] bit, the INTENSITY function or the HALF_TONE function is selected in accordance with Register DSRAM_ATTR_CON(0x010C[1]). The remaining one attribute is selected between Register G_INT(0x010C[0]) and Register G_HT_EN(0x010B[5]).

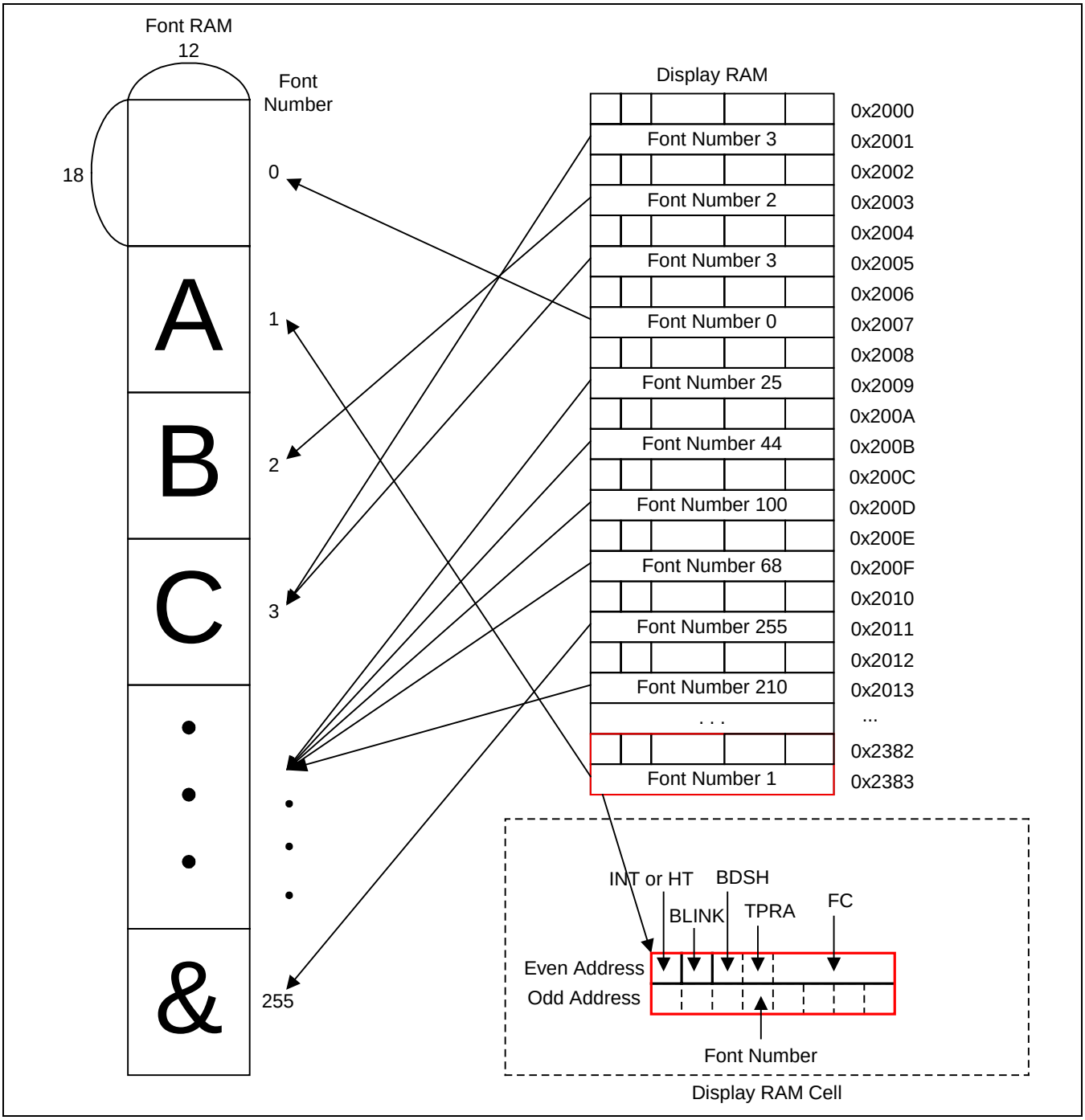


Figure 28. OSD Font RAM & Display RAM Structure

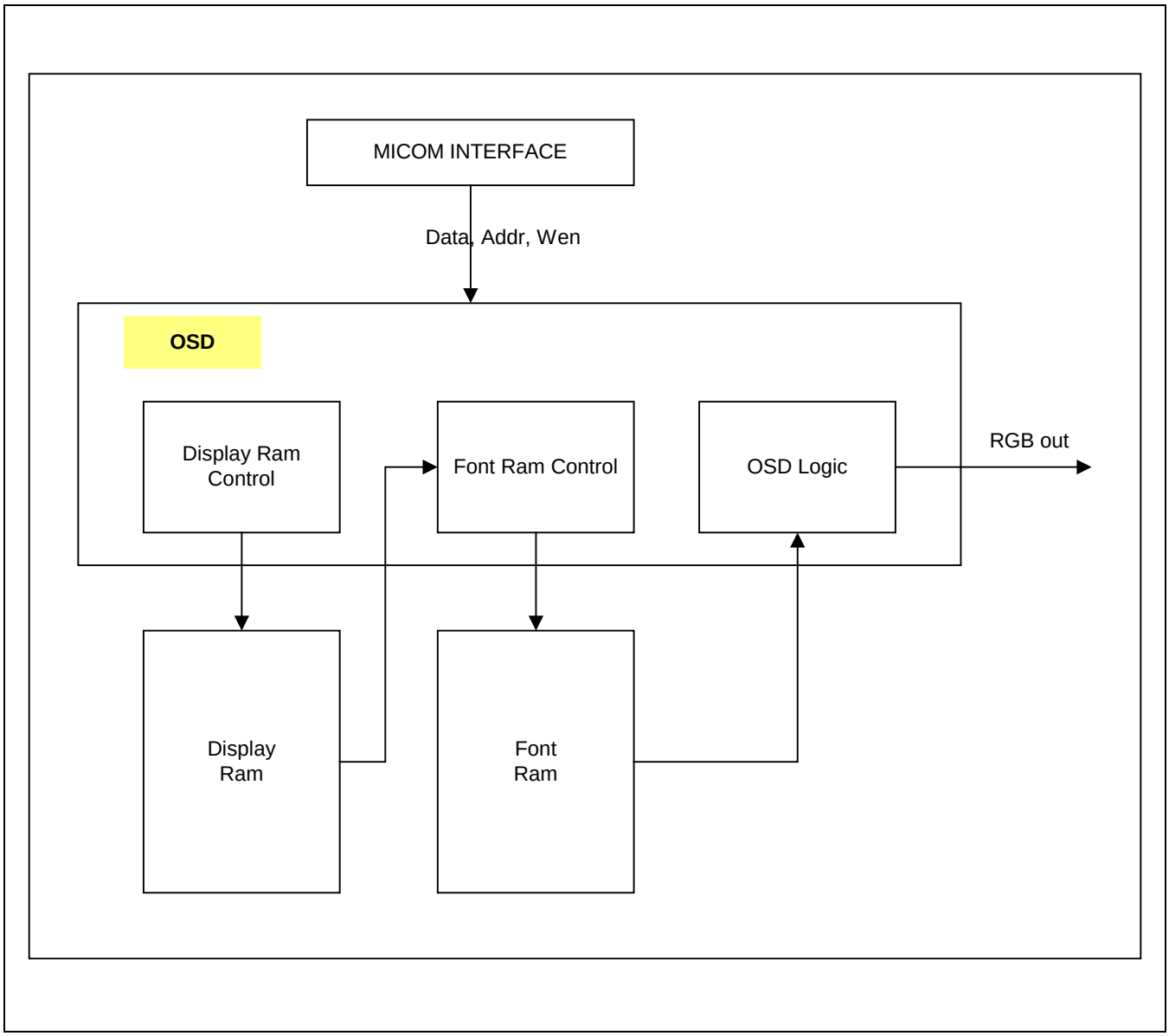


Figure 29. OSD System Block Diagram

5.10 CONTRAST CONTROL

The contrast block is designed to control R/G/B of Register BLACK (0x0081~0x0083), Register CONTRAST (0x0084~0x0086) and Register BRIGHTNESS (0x0087~0x0089). The block can also control them individually based on R. Black level and Brightness play the role of offset, and Contrast plays the role of gain.

Each pixel value is calculated as below.

Rout = [Rin - Blacklevel(Red)] * Contrast(Red) + Brightness(Red)

Gout = [Gin - Blacklevel(Green)] * Contrast(Green) + Brightness(Green)

Bout = [Bin - Blacklevel(Blue)] * Contrast(Blue) + Brightness(Blue)

5.11 GAMMA

The gamma correction block performs correction of the characteristics of the TFT-LCD panel. The block divides the input signal level into sections, generates the non-linear characteristic curve, and performs the gamma correction by substituting each section with linear function through linear interpolation. In other words, the block divides input into sections, and varies the output of each section to transform the characteristic curve for gamma correction. The input signal has the data level of 8 bits, and is equally divided into 32 sections with the interval of 8 between the sections.

The block receives the output value for each equally divided level from MCU, performs non-linear gamma correction, and for the values between the levels, the block performs gamma correction via linear interpolation.

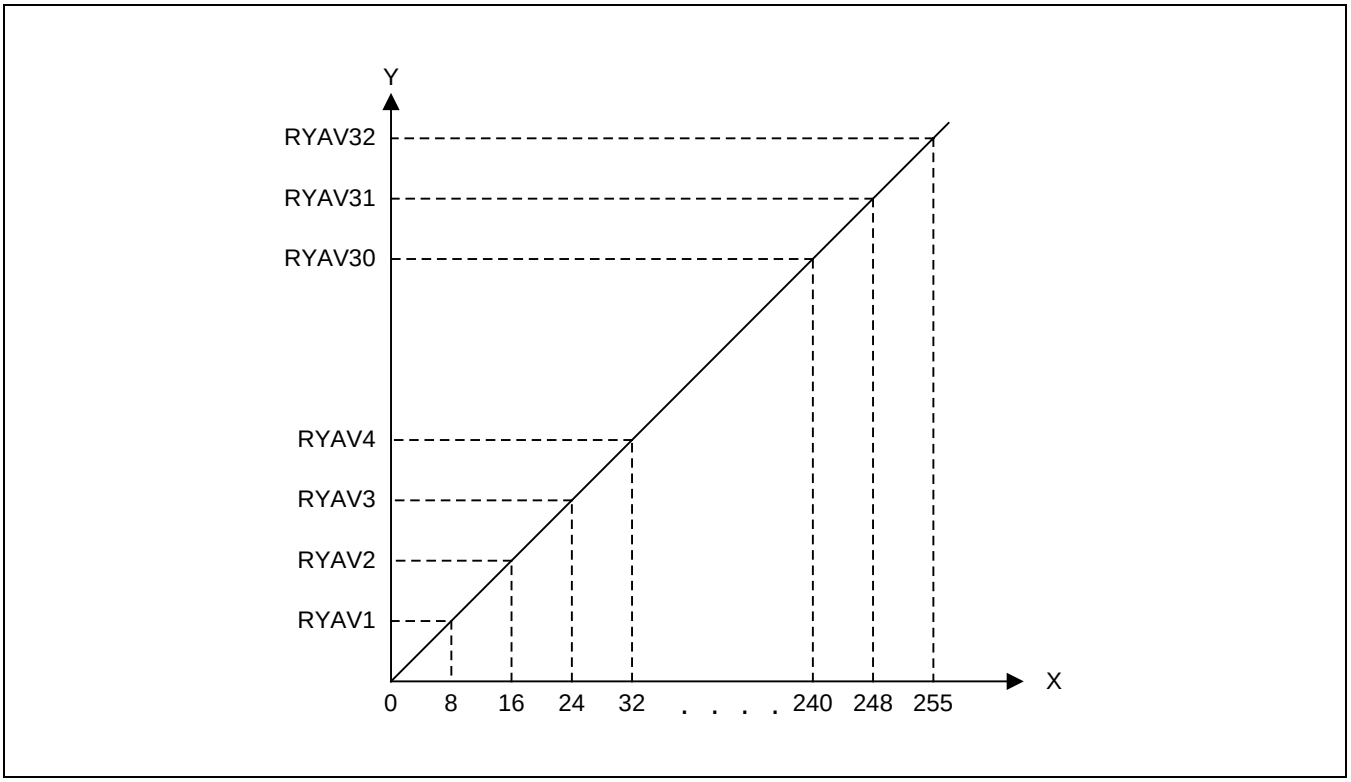


Figure 30. Gamma Graph

5.12 HOST INTERFACE

The host interface supports 3 protocols (6-Wire Host Interface Protocol, 3-Wire Host Interface Protocol and I2C Host Interface Protocol), and also supports the supplementary functions PWM and GPO. In order to use I2C Host Interface Protocol, HIF pin should be set to HIGH, and in order to use 3-Wire Host Interface Protocol, HIF pin should be set to LOW. To select 6-Wire Host Interface, as HIF = LOW, Register SIX_WIRE_ON should be set to HIGH.

5.12.1 6-wire Host Interface Protocol

S5D4100X supports data communication based on 6-WIRE Host Interface Protocol. The address used is 15 bits, and the data depth is 8 bits. 6-WIRE is active in the section where the SCSN line is LOW. The upper 1-bit of the initial 16 bits indicates R/W (R: HIGH, W: LOW), and the remaining 15 bits indicate the address. The write (or read) data are after the address and before stop. In case of address or write data, the master (MCU) should send the data at the SCL rising edge, and the slave (S5D4100X) should receive the data at the SCL falling edge. On the contrary, for read data, the slave sends the data at the SCL falling edge, and the master receives the data at the SCL rising edge.

Timing Chart (Data sequence in write/read of n registers)

Remark MS: MASTER Send to SLAVE
MR: MASTER Receive
SS: SLAVE Send to MASTER
SR: SLAVE Receive

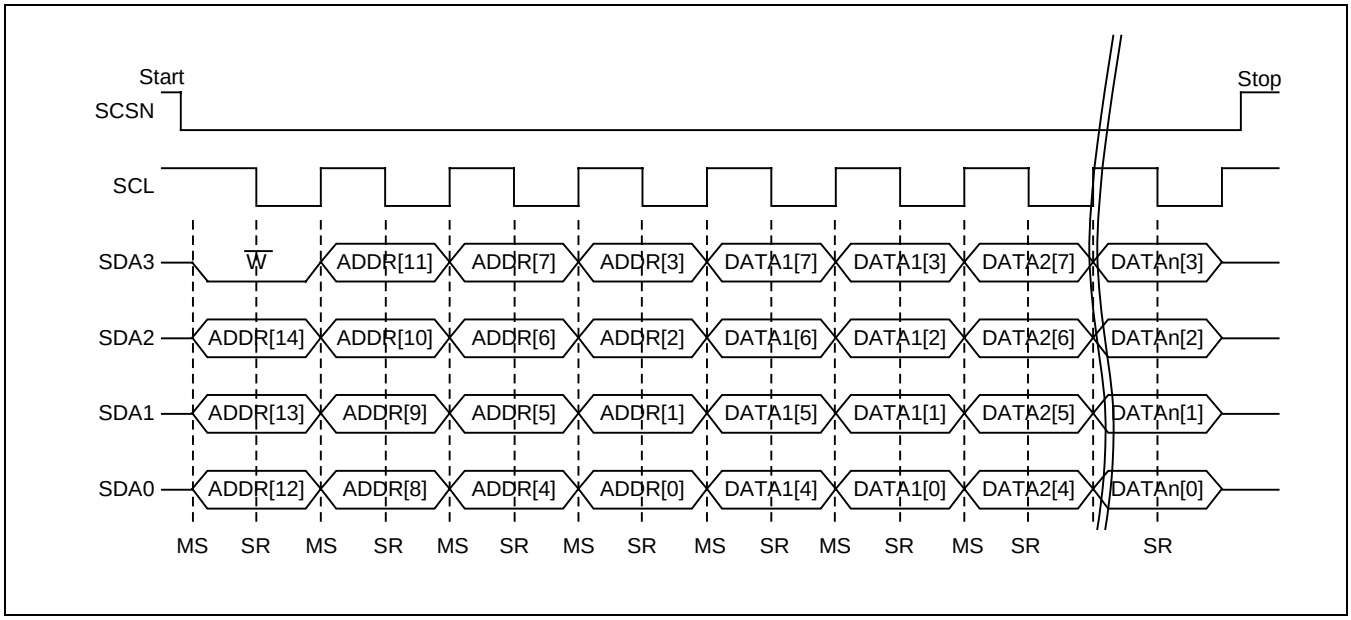


Figure 31. 6-wire Host Interface Write Data Sequence (Sending n data)

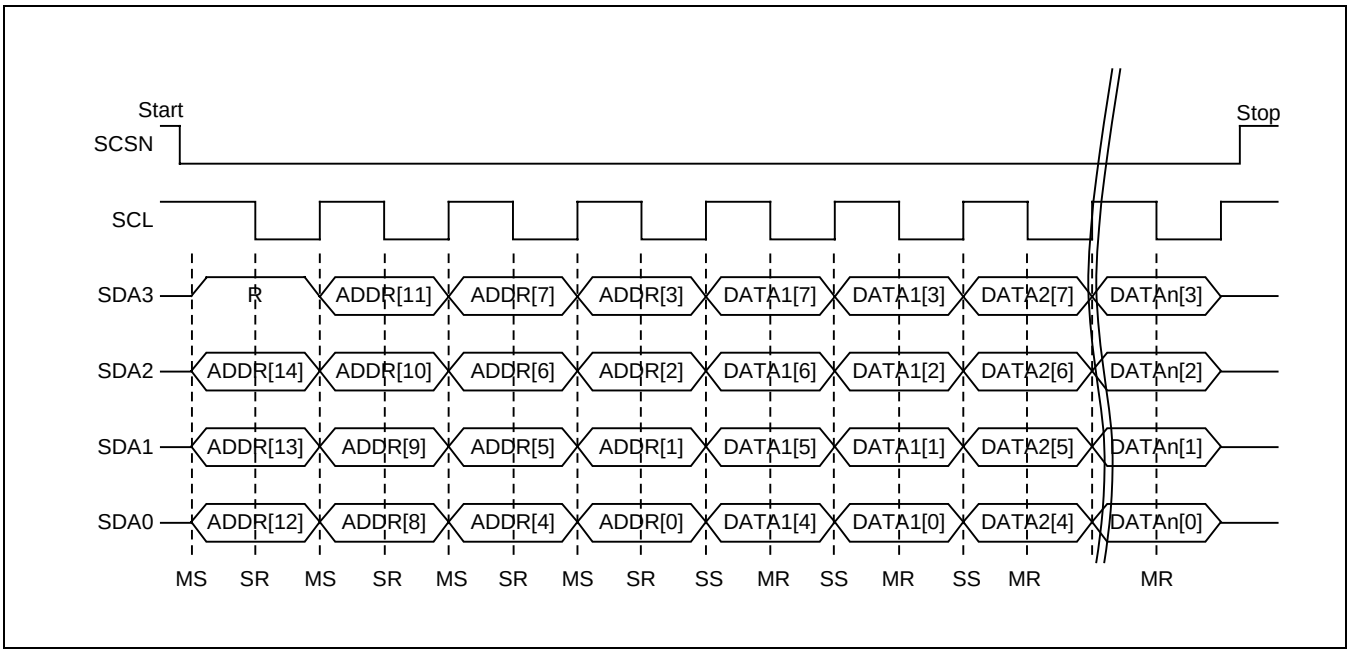


Figure 32. 6-wire Host Interface Read Data Sequence (Reading n data)

5.12.2 I2C Host Interface Protocol

S5D4100X supports data communication based on I2C Protocol. The slave address which corresponds to the device ID is 7 bits (binary “0000101”). The address used is 15 bits, and the data depth is 8 bits. Therefore, in order to access an address, the product indexes 2 bytes (Address MSB, Address LSB), and uses the 1-byte data depth. Since the address bits are 15 bits, the 1 byte for address MSB is “X A_{14} A_{13} A_{12} $A_{11}A_{10}$ A_9 A_8”, and the 1 byte for address LSB is Binary “A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0”.

1) Timing Chart (Data sequence in write/read of n registers)

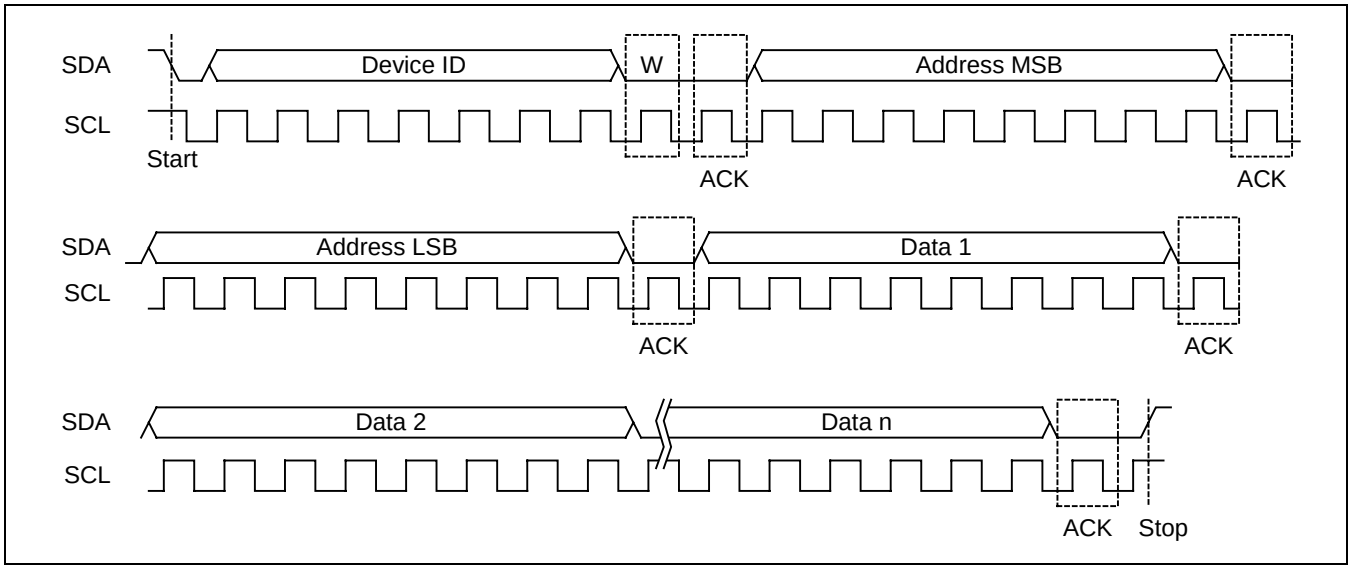


Figure 33. I2C Host Interface Write Data Sequence

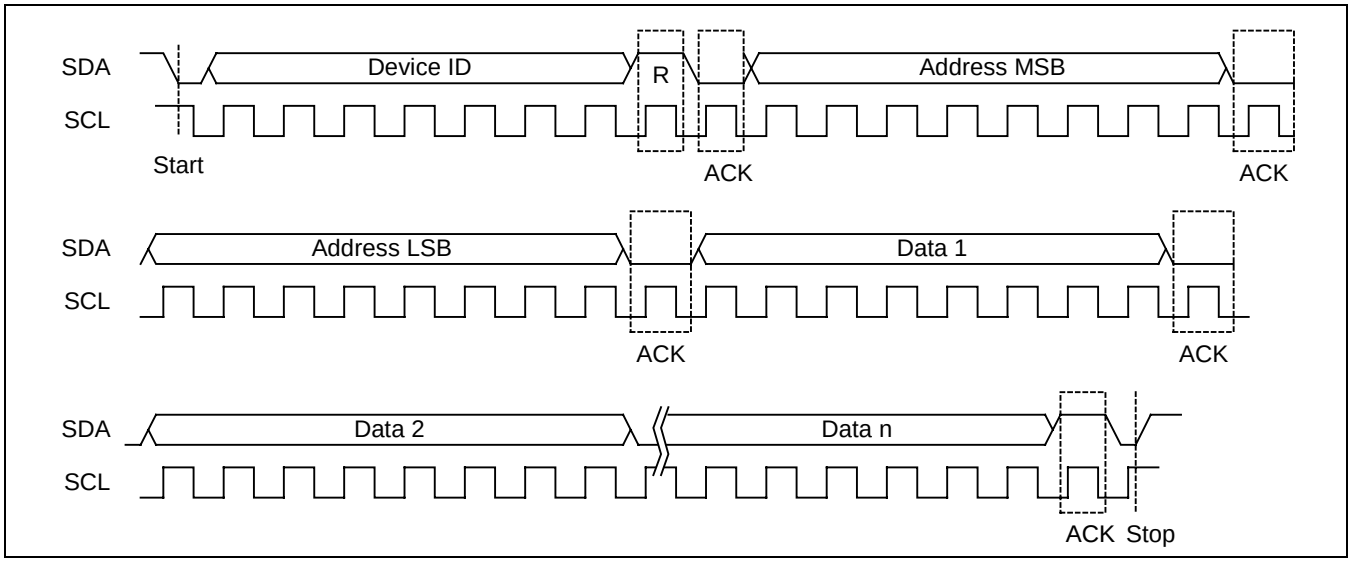
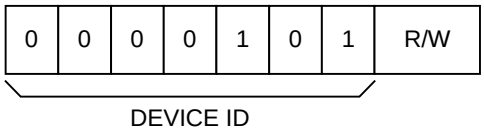


Figure 34. I2C Host Interface Read Data Sequence

In the above timing chart, the device ID (slave address) and read/write byte are as follows.



Address is 15 bits, and for the remaining upper 1 bit of the address MSB can be 0 or 1 (Don't Care: X).

2) Example

Write to one register

Send Start Signal
Send Device ID Byte (R/W Bit = LOW)
Send Address MSB
Send Address LSB
Send Data to Address
Send Stop Signal

Write to four consecutive registers

Send Start Signal
Send Device ID Byte (R/W Bit = LOW)
Send Address MSB
Send Address LSB
Send Data 1 to Address
Send Data 2 to (Address + 1)
Send Data 3 to (Address + 2)
Send Data 4 to (Address + 3)
Send Stop Signal

Read from one register

Send Start Signal
Send Device ID Byte (R/W Bit = HIGH)
Send Address MSB
Send Address LSB
Receive Data from Address
Send Stop Signal

Read form four consecutive control registers

Send Start Signal
Send Device ID Byte (R/W Bit = HIGH)
Send Address MSB
Send Address LSB
Receive Data 1 from Address
Receive Data 2 from (Address + 1)
Receive Data 3 from (Address + 2)
Receive Data 4 from (Address + 3)
Send Stop Signal

5.12.3 3-wire Host Interface Protocol

S5D4100X supports data communication based on 3-WIRE Host Interface Protocol. The address used is 15 bits, and the data depth is 8 bits. 3-WIRE is active in the section where the SCSN line is LOW. The upper 1 bit of the initial 16 bits indicates R/W (R: HIGH, W: LOW), and the remaining 15 bits indicate the address. The write (or read) data are after the address and before stop. In case of address or write data, the master (MCU) should send the data at the SCL rising edge, and the slave (S5D4100X) should receive the data at the SCL falling edge. On the contrary, for read data, the slave sends the data at the SCL falling edge, and the master receives the data at the SCL rising edge.

Remark

MS: MASTER Send to SLAVE
MR: MASTER Receive
SS: SLAVE Send to MASTER
SR: SLAVE Receive

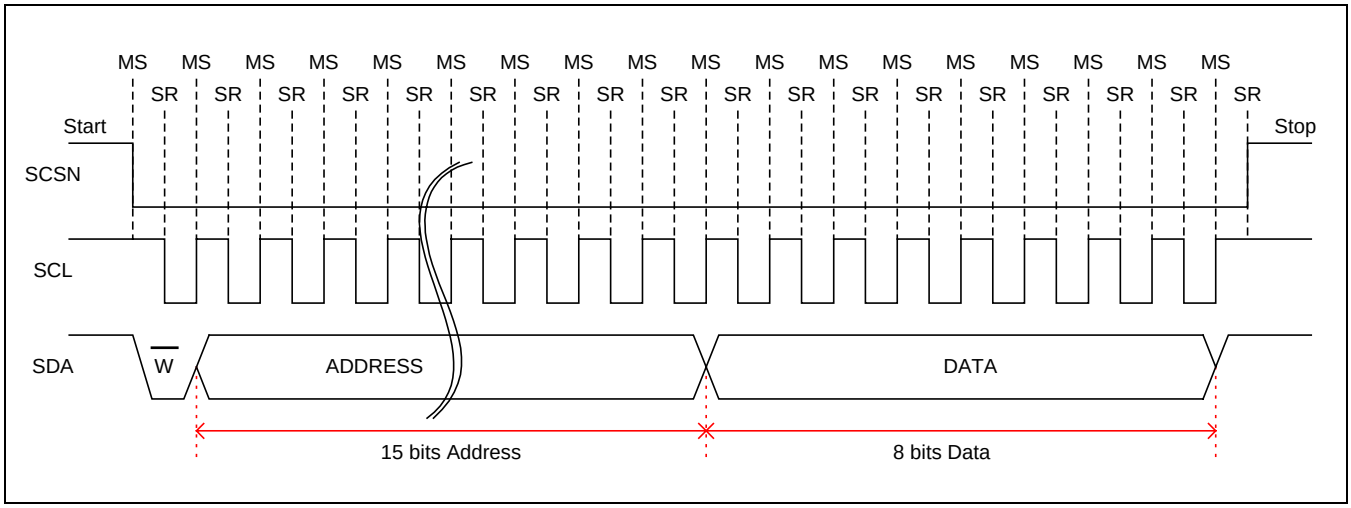


Figure 35. 3-wire Host Interface Write Data Sequence

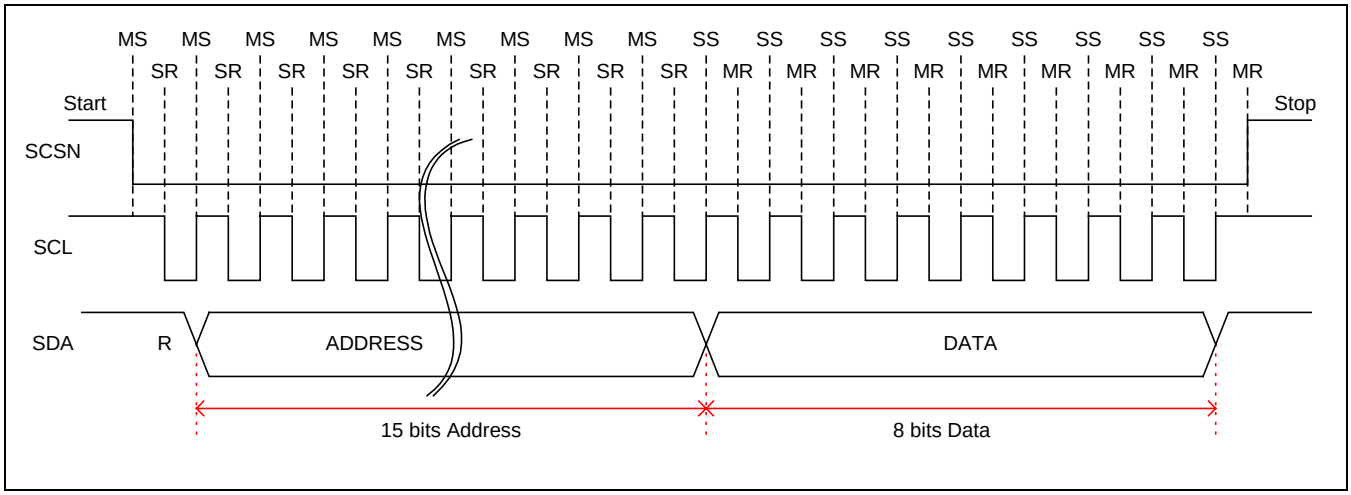


Figure 36. 3-wire Host Interface Read Data Sequence

5.12.4 Pulse Width Modulation (PWM)

PWM lets the high and low signal to have a regular width. S5D4100X has 2 PWMs; PWM0 and PWM1. To use the PWMs, Register PWM0_SEL and PWM1_SEL should be set to HIGH. In order to set PWM, PWM_PRE_SCALE should be set first. Register PWM_PRE_SCALE is 0 ~ 3, which makes PRE_SCALER to generate the clocks of bypass, 2-division, 4-division and 8-division, respectively, of CKOSC. PWM0/1 use the PRE_SCALER output as the clock, and send the HIGH signals in the unit of 256 clock for the value set in Register PWM_DATA0/1. If the final Register PWM_EN in the last output buffer is 1, the signal generated in PWM0/1 is displayed, and if it is 0, the function is disabled, and LOW signal is sent continuously. Then the signal is multiplexed by Register PWM0/1_SEL.

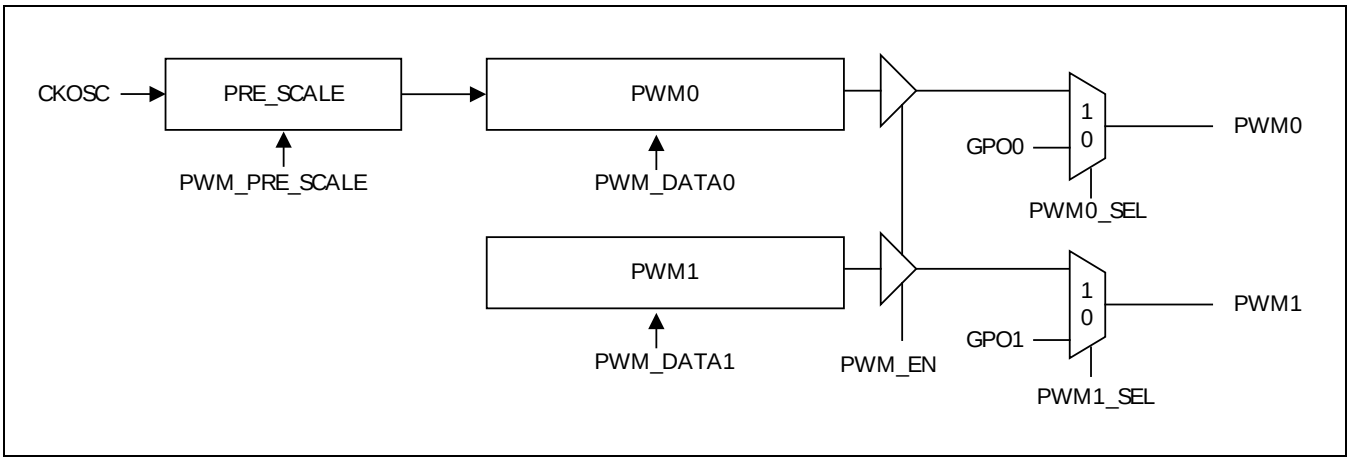


Figure 37. PWM

5.12.5 General Purpose Outputs (GPO's)

General Purpose Output (GPO) sends HIGH or LOW signal to Pins GO0~GO5 for the value set in GPO0 ~ GPO5 when Register SERIAL_ON is HIGH, and MCU controls the register. The product has 6 GPOs; GPO0 ~ GPO5. GPO0 and GPO1 can be sent to Pins PWM0/PWM1, regardless of Register SERIAL_ON, if Register PWM0_SEL and PWM1_SEL are LOW.

5.13 DATA OUTPUT FORMATTER & SERIAL INTERFACE

5.13.1 Output Formatter

S5D4100X supports output of various formats to meet various interfaces.

— R/G/B Parallel Output for RGB-Pixel Panel

— R/G/B Serial Output for RGB-Dot-Pixel LCD Panel

— ITU-R656, 8-Bit 4:2:2 Data with Embedded Sync Output for External Application

5.13.2 R/G/B Parallel output

S5D4100X sends 24-bit data to LCD panel via Output Pins RO0~RO7, GO0~GO7 and BO0~BO7, by setting Register SERIAL_ON to LOW for RGB-Pixel LCD Panel (Figure 38).

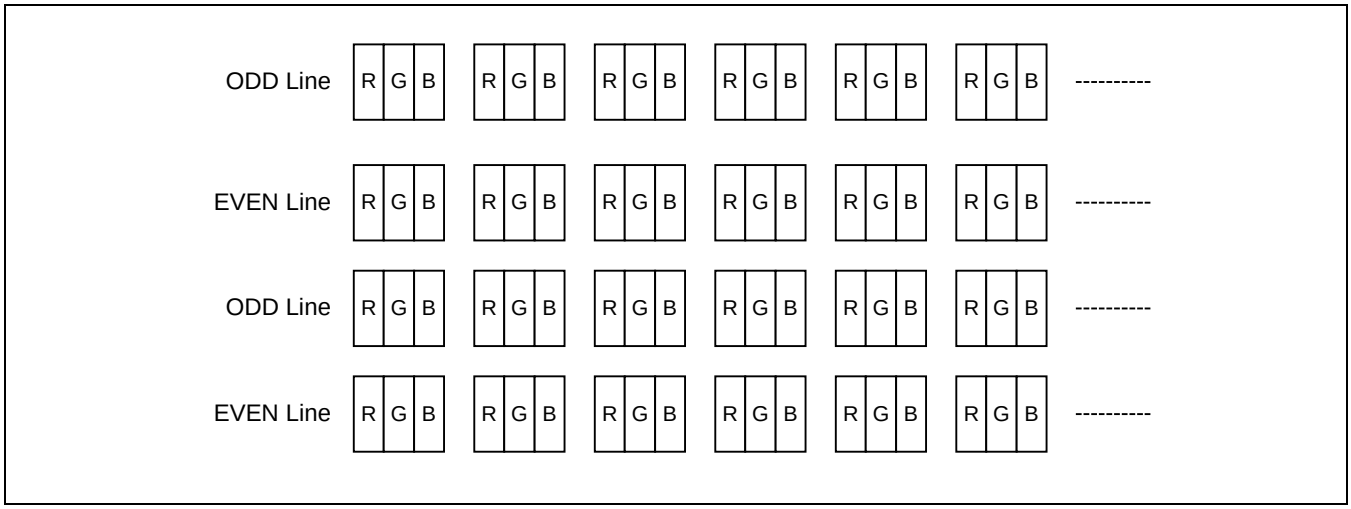


Figure 38. Parallel interface Panel Architecture

The product should support parallel data interface with the panel by sending 24-bit R/G/B data (Figure 39) in 1 clock in the R/G/B parallel output Interface mode.

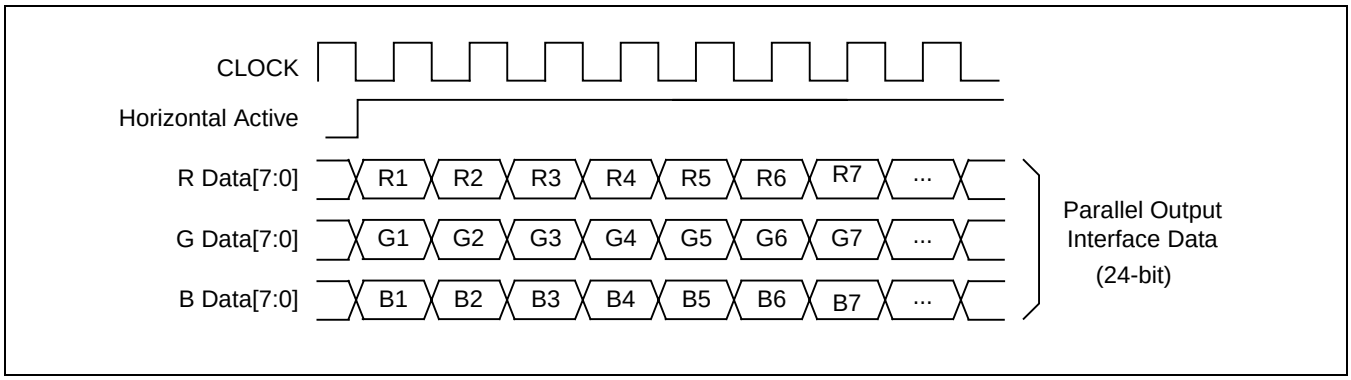


Figure 39. Parallel Output Data

5.13.3 RGB Serial output

S5D4100X sends the data in R/G/B serial output format through R Channel (OUTPUT PIN RO0~RO7) to correspond to RGB-Dot-Pixel LCD Panel (Figure 40). The product can send data to meet various delta type panel spec by setting Register SERIAL_ON HIGH, and Register ODD_SPL and EVEN_SPL. The R, G, B dot layout in Figure 40 may be changed depending on the panel spec.

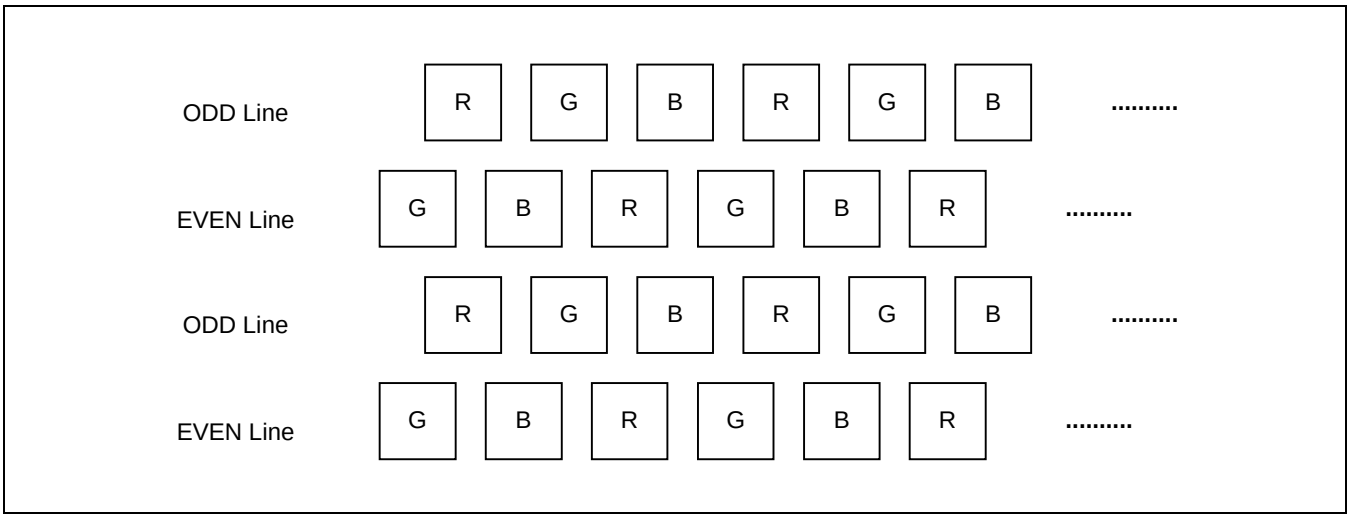


Figure 40. Delta Type Panel Architecture

Unlike the existing parallel interface panel (Figure 40) in which R/G/B data are sent in 1 clock (24-bit Parallel Output Interface Data), in the serial output interface panel, only one data (8-bit serial interface data) out of R/G/B data can be sent in 1 clock. (See Figure 41)

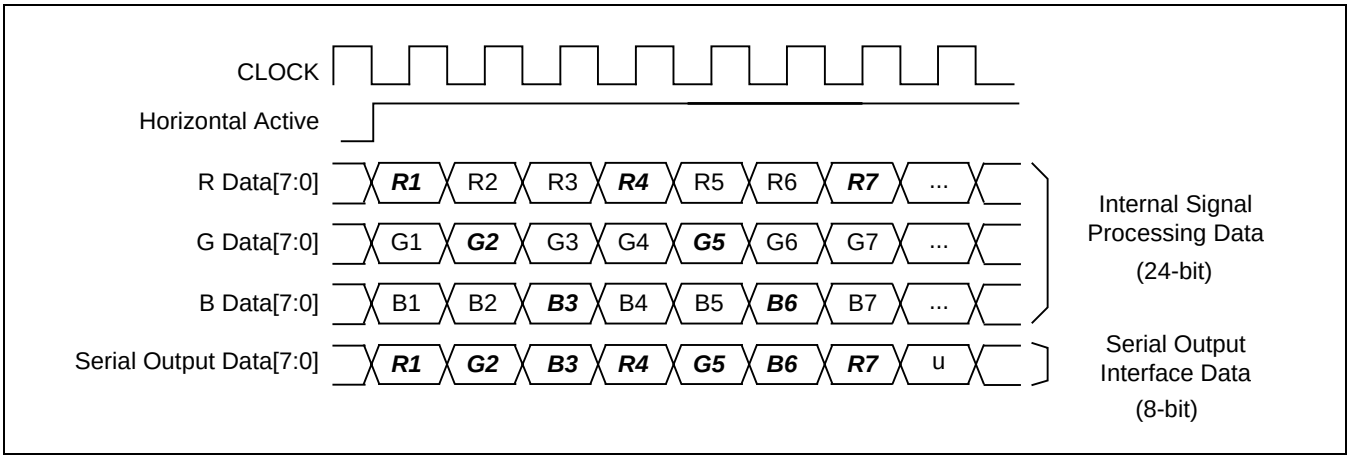


Figure 41. Serial Output Data

This table shows the sequence of R, G, B dot for register setting.

	Register HMODE = 1 (Based on DE Rising)	Register HMODE = 0 (Based on HS Falling)
Register ODD_SPL/ Register EVEN_SPL	R, G, B output order	R, G, B output order
000	R →G →B	R →G →B or G →B →R or B →R →G depending on the relationship between HS and DE
001	G →B →R	
010	B →R →G	
011	Not use	Not use
100	R →B →G	R (B (G or G (R (B or B (G (R depending on the relationship between HS and DE
101	G (R (B	
110	B (G (R	
111	Not use	Not use

In the delta type panel in Figure 40, EVEN Line is the vertically same timing data with ODD Line, but is deviated by 0.5 Dot due to the panel structure. In order to improve the delta structure display quality, set Register 0X000E[0] to 1, and set the compensation type of 0x000E[1].

If (Compensation Type = 0)

then, Compensated Pixel = (Previous Pixel + Current Pixel)/2,

if (Compensation Type = 1)

then, Compensated Pixel = (Current Pixel + Next Pixel)/2

5.13.4 ITU-656 output

S5D4100X sends data in serial output format to the panel via the R channel, and at the same time the ITU-R656 data to Channel B (OUTPUT PIN BO0 ~ BO7) to use another application.

Various path signals may be transformed to ITU-656 format in accordance with Register EN_656OUTSEL when Register SERIAL_ON and Register ENC_ON are HIGH.

5.14 POWER DOWN CONTROL

Power Down function is implemented as turning off each block and output pad. In case of Power Down Enable, you must set register value as below.

— Block Enable Register

GBI_ON(0x0001[5]) = 0
GBO_ON(0x0001[4]) = 0
BU_ON(0x0001[3]) = 0
OSD_ON(0x0001[2]) = 0
ENC_ON(0x0001[1]) = 0
SC_ON(0x0001[0]) = 0

— PLL Enable Register

PLL_PW_DN(0x000B[4]) = 1

— Pad Output Enable Register

PD_CTRL(0x0019[3]) = 1
RO_CTRL(0x0019[2]) = 1
GO_CTRL(0x0019[1]) = 1
BO_CTRL(0x0019[0]) = 1

In case of Power Down disable, you must set the value for before.

6. REGISTER MAP

Legend

Address		Address Name (Default Value)	R/W
Bits No.	**Register Name**	Function Description	

6.1 GLOBAL

0x0000		GLOBAL_BLOCK_CONTROL1 (Default: 0x 08)	R/W
7:6		Reserved	
5	**ITU656_CH**	ITU-656 Input Channel Select 0: Uses the pins YI7~YI0 for 656 data input, VCKI pin for clock input, and VD pin for VS input. 1: Uses the pins CI7~CI0 for 656 data input, HD pin for clock input, and FLD pin for VS input.	
4	**DTH_ON**	Dither Block ON/OFF Select 0: Dither OFF 1: Dither ON	
3	**SERIAL_ON**	Serial Output Mode ON/OFF 0: Sends 24-bit R/G/B data to the pins RO7~RO0 / GO7~GO0 / BO7~BO0 1: Sends 8-bit serial data to RO7~RO0	
2	**TEST_PAT_ON**	The ON/OFF register determines whether to use the internally created test pattern as the scaler input regardless of the input image. 0: Test Pattern OFF 1: Test Pattern ON	
1	**BG_COLOR_ ON**	Back Ground Color ON/OFF Register If Back Ground Color is ON, a single color image is entered to the gamma block to display the single color image on the screen regardless of the input image. The color is selected by the values 0x008A~0x008C. 0: Back Ground Color OFF 1: Back Ground Color ON	
0	**FREE_RUN**	Pseudo Sync RUN Mode The ON/OFF register determines whether to display Pseudo Sync if no Sync is received to S5D4100X (in case of 656, when no data is received). 0: Pseudo Sync Output OFF 1: Pseudo Sync Output ON	

0x0001		GLOBAL_BLOCK_CONTROL2 (Default: 0x 3F)	R/W
7	**SIX_WIRE_ON**	If HIF Pin is 1, the default value is 3-wire. In order to use Six-Wire, SIX_WIRE_ON should be set to 1. 0: 3-WIRE MODE 1: 6-WIRE MODE	
6		Reserved	
5	**GBI_ON**	Input Domain Clock ON/OFF 0: Input Domain Clock OFF 1: Input Domain Clock ON	
4	**GBO_ON**	Output Domain Clock ON/OFF 0: Output Domain Clock OFF 1: Output Domain Clock ON	
3	**BU_ON**	BOOSTUP Clock ON/OFF 0: BOOSTUP Clock OFF 1: BOOSTUP Clock ON	
2	**OSD_ON**	OSD Clock ON/OFF 0: OSD Clock OFF 1: OSD Clock ON	
1	**ENC_ON**	ENCODER Clock ON/OFF 0: ENCODER Clock OFF 1: ENCODER Clock ON	
0	**SC_ON**	SCALER Clock ON/OFF 0: SCALER Clock OFF 1: SCALER Clock ON	

0x0002		GLOBAL_TEST_PATTERN_CONTROL (Default: 0x 3F)	R/W
7	**TP_YCbCr_ON**	YUV TEST Domain Select If TP_YUV_ON is 1, TEST_PATTERN is created in the YCbCr domain, and if TP_YUV_ON is 0, TEST_PATTERN is created in the RGB domain. 0: RGB Domain Select 1: YCbCr Domain Select	
6	**TP_SYNC_ON**	Tests Sync ON If TEST_PAT_ON and TP_SYNC_ON, the internally created test sync is used as the input for the scaler. Timing for test sync is described in Figure 11. 0: Test Sync OFF 1: Test Sync ON	
5:0	**TP_RGB_ON**	Test pattern RGB ON/OFF Register 2 bits are assigned and controlled for RGB respectively. [5:4] - R , [3:2] - G , [1:0] – B See Table 5.1 for description on the 2 bits. If TP_YCbCr_ON is 1, YCbCr is controlled instead of RGB.	

0x0003		GLOBAL_TEST_PATTERN_SELECT (Default: 0x 00)	R/W
7:0	**TP_SEL**	Test Pattern Select The register is used for selection of test pattern. Figure 12 describes the register, and Figure 13 shows the types of patterns available.	

0x0004		GLOBAL_TEST_PATTERN_CONST_LEVEL_CONTROL (Default: 0x 00)	R/W
7:0	**TP_CONST_ LEVEL**	Constant Test Pattern Level Control The register is enabled when Pattern No. 6 is selected in TP_SEL. The register is used to select a specific level. Details are described in 5.5.2 Test Pat. Gen.	

0x0005		GLOBAL_TEST_PATTERN_CONST_WIDTH_CONTROL (Default: 0x 00)	R/W
7:0	**TP_CONST_ WIDTH**	Constant Test Pattern Width Control The register is enabled when Pattern No. 6 is selected in TP_SEL. The register is used to select a width of each level. Details are described in 5.5.2 Test Pat. Gen.	

0x0006		GLOBAL_INPUT_CLOCK_AND_MASK_CONTROL (Default: 0x 03)	R/W
7:4	**CKI_DLY**	Input Clock Delay The register delays the clock selected by ITU656_CH. The most significant bit of the 4 bits is the inversion signal.	
3	**CKI2_PHASE**	Changeable 2-Times Scaler Output Clock Phase 0: Normal 1: Phase Reverse	
2	**CKI_SEL**	Input Clock Select (See Figure 7 Clock System) 0: CKOSC Select 1: VCK Select	
1	**BLANK_MASK_ ON**	Input Blank Data Mask ON/OFF The register masks the blank area to black. 0: Mask OFF 1: Mask ON	
0	**ROLLING_ MASK_ON**	Input Rolling Data Mask ON/OFF The register masks the unnecessary image displayed due to rolling at moving of screen position. 0: Mask OFF 1: Mask ON	

0x0007		GLOBAL_OUTPUT_CLOCK_AND_SYNC_CONTROL (Default: 0x 00)	R/W
7:4	**CKO_DLY**	Output Clock Delay The register controls delay for the output clock sent to the PCKO pin. The most significant bit of the 4 bits is the inversion signal.	
3		Reserved	
2	**OPOL_DE**	Output Date Enable Signal (PDEO) Polarity 0: HIGH Active 1: LOW Active	
1	**OPOL_VS**	Output VS (PVSO) Polarity 0: LOW Active 1: HIGH Active	
0	**OPOL_HS**	Output HS (PHSO) Polarity 0: LOW Active 1: HIGH Active	

0x0008		GLOBAL_CLOCK_AND_SYNC_CONTROL (Default: 0x 04)	R/W
7:4	**M2CK_PHASE**	Encoder Clock Phase Control The register controls the clock phase when V601 is 1. It is controlled in the 2MUL block in Figure 7.	
3	**CKOSC_SEL**	CKOSC Clock Select 0: XI Pin 1: The clock selected by ITU656_CH (VCK or VD Pin)	
2:0	**PDEO_DLY**	PDEO Delay Output Data Enable Signal (PDEO Pin)	

0x0009		GLOBAL_GPO (Default: 0x 40)	R/W
7		Reserved	
6	**CKO_SEL**	CKO Domain Clock Select (See Figure 7 Clock System) 0: CKOSC Clock 1: PLL output Clock	
5	**GPO5**	General Purpose Output #5 (See 5.12.4)	
4	**GPO4**	General Purpose Output #4 (See 5.12.4)	
3	**GPO3**	General Purpose Output #3 (See 5.12.4)	
2	**GPO2**	General Purpose Output #2 (See 5.12.4)	
1	**GPO1**	General Purpose Output #1 (See 5.12.4)	
0	**GPO0**	General Purpose Output #0 (See 5.12.4)	

0x000A		GLOBAL_VFP_CLOCK_DOWN (Default: 0x 01)	R/W
7	**VFP_CKO_DN**	The ON/OFF signal used to determine whether to fix the PCKO clock in VFP section to LOW. 0: Normal mode 1: Clock Down	
6:0	**VDOWN**	The register designates the number of lines in which PCKO clock in VFP section should not be fixed to LOW when VFP_CKO_DN is HIGH.	

0x000B		GLOBAL_PWM_CONTROL (Default: 0x 20)	R/W
7:6	**PWM_PRE_ SCALE**	Determines the level of PWM duty to divide based on CKOSC clock when using the pulse width modulation 00: CKOSC 01: 2_Divided CKOSC 10: 4_Divided CKOSC 11: 8_Divided CKOSC	
5	**PWM_EN**	Pulse Width Modulation Enable 0: Disable (LOW Output Signal) 1: Enable (PWM Output Signal)	
4	**PLL_PW_DN**	PLL Power Down 0: Disable 1: Enable	
3:2		Reserved	
1	**PWM1_SEL**	PWM1 is sent if PWM1_SEL is HIGH, or GPO1 signal if it is LOW.	
0	**PWM0_SEL**	PWM0 is sent if PWM0_SEL is HIGH, or GPO0 signal if it is LOW.	

0x000C		GLOBAL_PWM_DATA0 (Default: 0x 00)	R/W
7	**PWM_DATA0**	Pulse Width Modulation 0 Creates, with the 256 clocks durations created by PWM_PRE_SCALE, the pulse of HIGH for the clock durations set in PWM_DATA0 and of LOW for the remaining clock durations.	

0x000D		GLOBAL_PWM_DATA1 (Default: 0x 00)	R/W
7	**PWM_DATA1**	Pulse Width Modulation1 Creates, with the 256 clocks durations created by PWM_PRE_SCALE, the pulse of HIGH for the clock durations set in PWM_DATA1 and of LOW for the remaining clock durations.	

0x000E		GLOBAL_SERIAL_CONTROL1 (Default: 0x 27)	R/W
7:6		Reserved	
5	**HMODE_SEL**	Selects the reference of serial data between HACT and HS. Since R/G/B of the serial format data should be transmitted in series, the internal counter is used. The register determines if the counter is started for HACT or HS. This indicates the section at which the valid data is transmitted via the actual serial output formatter. 0: HS 1: HACT	
4	**LINE_INV**	The signal exchanges ODD line and EVEN line. LINE_INV is used for vertical inversion display to set the color.	
3:2	**DATA_DLY**	This register is used to give delay on the data in serial interface when HS is fixed. This is added to meet various panel structures. The default is DATA_DLY = [01].	
1	**COMP_TYPE**	Depending on the panel structure, the EVEN line may starts earlier/later than ODD line by 0.5 pixel. Therefore, compensation type can be divided as follows. 0: Compensation between the previous pixel and the current pixel 1: Compensation between the current pixel and the next pixel	
0	**EVEN_COMP_ SEL**	Although the EVEN Line is of the same timing data with the ODD Line, but it may be deviated by 0.5 Dot due to the panel structure. In order to improve the display quality of the delta structure, set Register 0X000E[0] to 1, and set the compensation type of 0x000E[1].	

0x000F		GLOBAL_SERIAL_CONTROL2 (Default: 0x01)	R/W
7		Reserved	
6:4	**ODD_SPL**	Sends the data in the ODD line in the following sequence. If 0X000F[6] = 0, …→ R → G → B → R → G → B → … If 0X000F[6] = 1, …→ R → B → G → R → B → G → … The first data of the line is determined in accordance with 0X000F[5:4]. If HMODE_SEL = HIGH, the first data are ODD_SPL[1:0]= [00] → R, ODD_SPL[1:0]= [01] → G, ODD_SPL[1:0]= [10] → B. If HMODE_SEL =LOW, because the counter is fixed, the first data may vary. 0x000F[5:4] = [11] is not used.	
3		Reserved	
2:0	**EVEN_SPL**	Sends the data in the EVEN line in the following sequence. If 0X000F[2] = 0, …→ R → G → B → R → G → B → … If 0X000F[2] = 1, …→ R → B → G → R → B → G → … The first data of the line is determined in accordance with 0X000F[1:0]. If HMODE_SEL = HIGH, the first data are EVEN_SPL[1:0]= [00] → R, EVEN_SPL[1:0]= [01] → G, EVEN_SPL[1:0]= [10] → B. If HMODE_SEL = LOW, because the counter is fixed, the first data may vary. 0x000F[1:0] = [11] is not used.	

0x0010		GLOBAL_OUTPUT_MASK_HMIN_MSB (Default: 0x 08)	R/W
7:4		Reserved	
3	**DEMODE**	Horizontal Output MASK Mode Select 0: SYNC MODE 1: DE MODE	
2:0	**HOUTMIN[10:8]**	Horizontal Output MASK min number	

0x0011		GLOBAL_OUTPUT_MASK_HMIN_LSB (Default: 0x 00)	R/W
2:0	**HOUTMIN[7:0]**	Horizontal Output MASK min number	

0x0012		GLOBAL_OUTPUT_MASK_HMAX_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**HOUTMAX [10:8]**	Horizontal Output MASK max number	

0x0013		GLOBAL_OUTPUT_MASK_HMAX_LSB (Default: 0x 00)	R/W
2:0	**HOUTMAX[7:0]**	Horizontal Output MASK max number	

0x0014		GLOBAL_OUTPUT_MASK_VMIN_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**VOUTMIN[10:8]**	Vertical Output MASK min number	

0x0015		GLOBAL_OUTPUT_MASK_VMIN_LSB (Default: 0x 00)	R/W
2:0	**VOUTMIN[7:0]**	Vertical Output MASK min number	

0x0016		GLOBAL_OUTPUT_MASK_VMAX_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**VOUTMAX[10:8]**	Vertical Output MASK max number	

0x0017		GLOBAL_OUTPUT_MASK_VMAX_LSB (Default: 0x 00)	R/W
2:0	**VOUTMAX[7:0]**	Vertical Output MASK max number	

0x0018		GLOBAL_VFP_HS_DOWN (Default: 0x 00)	R/W
7	**HS_DN_ON**	The ON/OFF signal used to determine whether to fix the PHSO in VFP section to LOW. 0: Normal mode 1: HS down	
6:0	**HS_DN**	The register designates the number of lines in which PHSO in VFP section should not be fixed to LOW when HS_DN_ON is HIGH.	

0x0019		GLOBAL_PAD_CONTROL (Default: 0x00)	R/W
3	**PD_CTRL**	PVSO/PHSO/PDEO/PCKO Output Enable Signal 0: Output enable 1: Output Disable	
2	**RO_CTRL**	RO0 ~ RO7 Output Enable Signal 0: Output enable 1: Output Disable	
1	**GO_CTRL**	GO0 ~ GO7 Output Enable Signal 0: Output enable 1: Output Disable	
0	**BO_CTRL**	BO0 ~ BO7 Output Enable Signal 0: Output enable 1: Output Disable	

6.2 TIMING GENERATOR

0x0020		TG_TIMING_CONTROL (Default: 0x84)	R/W
7	**AUTO_TOTAL**	Auto TOTAL setting register Determines whether to use the internally calculated value or the register setting for the addresses 0x0021 ~ 0x0025. 1: Auto Set (Internally calculated value) 0: Manual Set (Register setting)	
6	**HVSO_DET**	For inversion, resets and detects TG sync creation to create output sync.	
5		Reserved	
4:3	**DET_FRAME**	Sets the TG detection start frame (1 ~ 4 Frame). Sets the number of frames to be referred for detection in order to create normal sync after inversion of HVSO_DET.	
2		Reserved	
1:0	**PLL_FIN_SEL**	PLL PFD Input Signal Select (See Figure 16) 0: Pre-Divider Output 1: Not Used 2, 3: HS	

0x0021		TG _ADDED_LINE(Default: 0x 01)	R/W
7:0	**ADDED_LINE**	Sets the difference value between the odd and the even field.	

0x0022		TG _INPUT_HTOTAL_MSB (Default: 0x 03)	R/W
7:3		Reserved	
2:0	**HTOTAL[10:8]**	Horizontal Input Total Pixel Value	

0x0023		TG _INPUT_HTOTAL_LSB (Default: 0x 5A)	R/W
7:0	**HTOTAL[7:0]**	Horizontal Input Total Pixel Value	

0x0024		TG _INPUT_VTOTAL_MSB (Default: 0x 01)	R/W
7:3		Reserved	
2:0	**VTOTAL[10:8]**	Vertical Input Total Pixel Value	

0x0025		TG _INPUT_VTOTAL_LSB (Default: 0x 07)	R/W
7:0	**VTOTAL[7:0]**	Vertical Input Total Pixel Value	

0x0026		TG _INPUT_H_START_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**H_STR[10:8]**	Horizontal Active Input Start Point	

0x0027		TG _INPUT_H_START_LSB (Default: 0x86)	R/W
7:0	**H_STR[7:0]**	Horizontal Active Input Start Point	

0x0028		TG _INPUT_V_START_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**V_STR[10:8]**	Vertical Active Input Start Point	

0x0029		TG _INPUT_V_START_LSB (Default: 0x 14)	R/W
7:0	**V_STR[7:0]**	Vertical Active Input Start Point	

0x002A		TG _HOFP (Default: 0x 2B)	R/W
7:0	**HOFP**	Horizontal Output Front Porch	

0x002B		TG _HOSW (Default: 0x 2E)	R/W
7:0	**HOSW**	Horizontal Output Sync Width	

0x002C		TG L_HOBP_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**HOBP [10:8]**	Horizontal Output Back Porch	

0x002D		TG_HOBP_LSB (Default: 0x 32)	R/W
7:0	**HOBP[7:0]**	Horizontal Output Back Porch	

0x002E		TG_VOFP (Default: 0x 01)	R/W
7:0	**VOFP[7:0]**	Vertical Output Front Porch	

0x002F		TG_VOSW (Default: 0x 03)	R/W
7:0	**VOSW[7:0]**	Vertical Output Front Porch	

0x0030		TG_HIAS_MSB (Default: 0x 02)	R/W
7:3		Reserved	
2:0	**HIAS [10:8]**	Horizontal Input Active Size	

0x0031		TG_HIAS_LSB (Default: 0x D0)	R/W
7:0	**HIAS[7:0]**	Horizontal Input Active Size	

0x0032		TG_VIAS_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**VIAS [10:8]**	Vertical Input Active Size	

0x0033		TG_VIAS_LSB (Default: 0x F0)	R/W
7:0	**VIAS[7:0]**	Vertical Input Active Size	

0x0034		TG_HOAS_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**HOAS [10:8]**	Horizontal Output Active Size	

0x0035		TG_HOAS_LSB (Default: 0x E0)	R/W
7:0	**HOAS[7:0]**	Horizontal Output Active Size	

0x0036		TG_VOAS_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**VOAS [10:8]**	Vertical Output Active Size	

0x0037		TG_VOAS_LSB (Default: 0x F0)	R/W
7:0	**VOAS[7:0]**	Vertical Output Active Size	

0x0038		TG_PLL_P_MSB (Default: 0x 04)	R/W
7:0	**PLL_P[7:0]**	PLL Programmable Pre-Divider	

0x0039		TG_PLL_P_LSB (Default: 0x 38)	R/W
7:0	**PLL_P[7:0]**	PLL Programmable Pre-Divider	

0x003A		TG_PLL_M_MSB (Default: 0x 0C)	R/W
7:6		Reserved	
5:0	**PLL_M [13:8]**	PLL Programmable Main-Divider	

0x003B		TG_PLL_M_LSB (Default: 0x 21)	R/W
7:0	**PLL_M[7:0]**	PLL Programmable Main-Divider	

0x003C		TG_PLL_S (Default: 0x 03)	R/W
7:5		Reserved	
4:0	**PLL_S**	PLL Programmable Post Scaler, S= PLL_S[4: 2] + PLL_S[1: 0]	

0x003D		TG_PLL_M_FRACT_LSB (Default: 0x 92)	R/W
7:0	**PLL_M_FRACT**	TG's PLL_M register Fraction bits	

0x0042		TG_HOFFSET_MSB (Default: 0x 00)	R/W
7:6		Reserved	
5:0	**HOFFSET[13:8]**	Horizontal Output Active Point Offset Delay	

0x0043		TG_HOFFSET_LSB (Default: 0x 84)	R/W
7:0	**HOFFSET[7:0]**	Horizontal Output Active Point Offset Delay	

0x0044		TG_HOFFSET_ODD_MSB (Default: 0x 00)	R/W
7:6		Reserved	
5:0	**HOFFSET_ODD [13:8]**	Horizontal Output Active Point Offset Delay. (Odd Field Only)	

0x0045		TG_HOFFSET_ODD_LSB (Default: 0x 00)	R/W
7:0	**HOFFSET_ODD [7:0]**	Horizontal Output Active Point Offset Delay. (Odd Field Only)	

0x0046		TG_HPOS_MSB (Default: 0x 00)	R/W
7:4		Reserved	
3:0	**HPOS[11:8]**	Horizontal Position *(Engineering Test Mode, User Forbidden)*	

0x0047		TG_HPOS_LSB (Default: 0x 00)	R/W
7:0	**HPOS[7:0]**	Horizontal Position (Engineering Test Mode, User Forbidden)	

0x0048		TG_VPOS (Default: 0x 00)	R/W
7:0	**VPOS[7:0]**	Vertical Position (Engineering Test Mode, User Forbidden)	

0x004B		TG_VMIN_ODD	RO
7:0	**VMIN_ODD[7:0]**	Odd Field Output Vertical min number	

0x004C		TG_VMIN_EVEN	RO
7:0	**VMIN_EVEN[7:0]**	Odd Field Output Vertical min number	

6.3 YC PROCESSOR

0x0050		YCP_SYNC_CONTROL (Default: 0x7C)	R/W
7		Reserved	
6	**SEL_DI**	Decoding domain select 0: YCbCr Domain 1: YUV Domain	
5	**DI_FIELD_POL**	Input FIELD Signal Polarity 0: Even Field HIGH, Odd Field LOW - 656 SPEC 1: Odd Field HIGH, Even Field LOW - Required Design	
4	**DI_HACT_POL**	HACT Signal Polarity 0: Active LOW - 656 SPEC 1: Active HIGH - Required Design	
3	**DI_VACT_POL**	VACT Signal Polarity 0: Active LOW - 656 SPEC 1: Active HIGH - Required Design	
2	**DI_SYNC_GEN**	Sync Generation Block Selection 0: New Adjustment (Required Design) 1: S5D0127X Version	
1	**DI_C_SIGN**	Chroma Sign Bit Determination 0: Positive Number – SPEC (Required Design) 1: 2's Complementary - Non SPEC	
0	**DI_CBCR_SEL**	Cb / Cr Signal Input Type Selection 0: CB Y CR Y CB Y ... - SPEC (Required Design) 1: CR Y CB Y CR Y ... - NON_SPEC	

0x0051		YCP_SYNC_SELECT (Default: 0x80)	R/W
7	**V601**	601/656 Data Input Select 0: ITU-R656 Format 1: ITU-R601 Format	
6		Reserved	
5	**MASK_ON**	Input Masking Enable Input data is masked by the registers of 0X0057 ~ 0X005E. The register turns ON/OFF this masking process. 0: MASKING OFF 1: MASKING ON	
4	**INT_FLD_SEL**	Internal 601 Field select 0: External Field 1: Internal Field	
3	**FIELD_OUT_POL**	Field Output Polarity	
2	**DI_HS_SEL**	656 Data Input Hsync Select 0: 656 Data Hsync use 1: HD Pin Input Hsync use	
1	**DI_VS_SEL**	656 Data Input Vsync Select 0: 656 Data Vsync use 1: VD Pin Input Vsync use	
0		Reserved	

0x0052		YCP_VSYNC_DELAY (Default: 0x10)	R/W
7:4	**VS_ODD_DLY**	Vsync Odd Field Vertical Delay Select	
3:0	**VS_EVEN_DLY**	Vsync Even Field Vertical Delay Select	

0x0053		YCP_DI_HFP (Default: 0x0A)	R/W
7:0	**DI_HFP**	Horizontal Front Porch for HSync Output	

0x0054		YCP_DI_HSW (Default: 0x1E)	R/W
7:0	**DI_HSW**	Horizontal Pulse Width for HSync Output	

0x0055		YCP_DI_VFP (Default: 0x02)	R/W
7:0	**DI_VFP**	Vertical Front Porch for VSync Output	

0x0056		YCP_DI_VSW (Default: 0x08)	R/W
7:0	**DI_VSW**	Vertical Pulse Width for VSync Output This should be set to 0x01 if the setting should be made regardless of the scale factor.	

0x0057		YCP_HACT_MIN_MSB (Default: 0x00)	R/W
7:3		Reserved	
2:0	**DI_HACT_MIN [10:8]**	Horizontal Active Input Start Point Sets the start point of the input image based on the rising time of the sync selected by DI_HS_SEL.	

0x0058		YCP_HACT_MIN_LSB (Default: 0x00)	R/W
7:0	**DI_HACT_MIN [7:0]**	Horizontal Active Input Start Point Sets the start point of the input image based on the rising time of the sync selected by DI_HS_SEL.	

0x0059		YCP_HACT_MAX_MSB (Default: 0x00)	R/W
7:3		Reserved	
2:0	**DI_HACT_MAX [10:8]**	Horizontal Active Input End Point Sets the end point of the input image based on the rising time of the sync selected by DI_HS_SEL.	

0x005A		YCP_HACT_MAX_LSB (Default: 0x00)	R/W
7:0	**DI_HACT_MAX [7:0]**	Horizontal Active Input End Point Sets the end point of the input image based on the rising time of the sync selected by DI_HS_SEL.	

0x005B		YCP_VACT_MIN_MSB (Default: 0x00)	R/W
7:3		Reserved	
2:0	**DI_VACT_MIN [10:8]**	Vertical Active Input Start Point Sets the start point of the input image based on the rising time of the sync selected by DI_VS_SEL.	

0x005C		YCP_VACT_MIN_LSB (Default: 0x00)	R/W
7:0	**DI_VACT_MIN [7:0]**	Vertical Active Input Start Point Sets the start point of the input image based on the rising time of the sync selected by DI_VS_SEL.	

0x005D		YCP_VACT_MAX_MSB (Default: 0x00)	R/W
7:3		Reserved	
2:0	**DI_VACT_MAX [10:8]**	Vertical Active Input End Point Sets the end point of the input image based on the rising time of the sync selected by DI_VS_SEL.	

0x005E		YCP_VACT_MAX_LSB (Default: 0x00)	R/W
7:0	**DI_VACT_MAX [7:0]**	Vertical Active Input End Point Sets the end point of the input image based on the rising time of the sync selected by DI_VS_SEL.	

0x005F		YCP_FIELD_601_TH (Default: 0x00)	R/W
7:0	**INT_FIELD_601_ TH**	Internal 601 Field Threshold Sets the threshold for creation of internal field when INT_FLD_SEL is HIGH.	

0x0060		YCP_CORE (Default: 0x00)	R/W
7:4	**CORE_H**	EDGE Coring HIGH level (See Figure 10)	
3:0	**CORE_L**	EDGE Coring LOW level (See Figure 10)	

0x0061		YCP_EDGE_CONTROL (Default: 0x54)	R/W
7:6	**EDGE_FIL_SEL**	EDGE Filter Select 0: Filter0 1: Filter1 2: Not Use 3: Filter2	
5:4	**CORE_RATE**	EDGE Coring Gain (See Figure 10)	
3:0	**EDGE_GAIN**	EDGE Gain The default value 4 means x1. The higher the value, the edge strength increases, and vice versa. (See 0x006E.)	

0x0062		YCP_BLACK (Default: 0x00)	R/W
7:0	**YCP_BLACK**	Black Level of Y element YOUT = (YIN – YCP_BLACK) * YCP_CONTRAST + YCP_BRIGHTNESS	

0x0063		YCP_CONTRAST (Default: 0x80)	R/W
7:0	**YCP_CONTRAST**	Contrast Control of Y element YOUT = (YIN – YCP_BLACK) * YCP_CONTRAST + YCP_BRIGHTNESS	

0x0064		YCP_BRIGHTNESS (Default: 0x00)	R/W
7:0	**YCP_ BRIGHTNESS**	BRIGHTNESS Control of Y element 2's complement in negative number. YOUT = (YIN – YCP_BLACK) * YCP_CONTRAST + YCP_BRIGHTNESS	

0x0065		YCP_HUE_MSB (Default: 0x00)	R/W
7:2		Reserved	
1:0	**HUE[9:8]**	HUE Control 2'complement between -512 and +511. The value is between -180 deg and +180 deg.	

0x0066		YCP_HUE_LSB (Default: 0x00)	R/W
7:0	**HUE[7:0]**	HUE Control 2'complement between -512 and +511. The value is between -180 deg and +180 deg.	

0x0067		YCP_SATURATION (Default: 0x80)	R/W
7:0	**SATURATION**	SATURATION Control	

0x0068		YCP_ENCODER_SELECT (Default: 0x18)	R/W
7:6	**EN_656OUTSEL**	656 OUTPUT SELECT (See Table 2)	
5		Reserved	
4	**EN_HPOL**	Encoder Horizontal Active Polarity Select	
3	**EN_VPOL**	Encoder Vertical Active Polarity Select	
2	**EN_FPOL**	Encoder Field Polarity Select	
1	**EN_LIM16**	Encoder Data Range Select (1:16 ~ 240, 0:1~254)	
0	**EN_VSO_SEL**	Encoder Vertical Timing Select 0: Vertical Active Signal Select 1: Vsync Signal Select	

0x0069		YCP_ENCODER_CLOCK_DELAY (Default: 0x00)	R/W
7:4		Reserved	
3:0	**EN_CK_DLY**	Encoder Output Clock Delay The register controls delay for the output clock sent to the Pin GO7 when the encoder runs. The most significant bit of the 4 bits is the inversion signal.	

0x006A		YCP_OUT_HSYNC_CONTROL_MSB (Default: 0x02)	R/W
7	**HOUT_DET**	Horizontal Timing Detection Select 0:Falling Time 1:Rising Time	
6:3		Reserved	
2:0	**IN_WIDTH[10:8]**	Horizontal Timing Width (Used in timing detection)	

0x006B		YCP_OUT_HSYNC_CONTROL_LSB (Default: 0xD0)	R/W
7:0	**IN_WIDTH[7:0]**	Horizontal Timing Width (Used in timing detection)	

0x006C		YCP_OUT_VSYNC_CONTROL_MSB (Default: 0x00)	R/W
7	**VOUT_DET**	Vertical Timing Detection Select 0: Falling Time 1: Rising Time	
6:3		Reserved	
2:0	**IN_LINE[10:8]**	Vertical Timing Line (Used in timing detection)	

0x006D		YCP_OUT_VSYNC_CONTROL_LSB (Default: 0xF0)	R/W
7:0	**IN_LINE[7:0]**	Vertical Timing Line (Used in timing detection)	

0x006E		YCP_EDGE_LIMIT (Default: 0x10)	R/W
7		Reserved	
6:0	**EDGE_LIM**	EDGE LIMIT (See Figure 10)	

6.4 SCALER

0x0071		SCALER_IVZOOM_MSB (Default: 0x20)	R/W
7:0	**IVZOOM[23:16]**	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

0x0072		SCALER_IVZOOM_MID (Default: 0x00)	R/W
7:0	**IVZOOM[15:8]**	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

0x0073		SCALER_IVZOOM_LSB (Default: 0x00)	R/W
7:0	**IVZOOM[7:0]**	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

0x0075		SCALER_IHZOOM_MSB (Default: 0x2F)	R/W
7:0	**IHZOOM[23:16]**	Inversed Horizontal Zoom Ratio (= VIAS/VOAS)	

0x0076		SCALER_IHZOOM_MID (Default: 0x55)	R/W
7:0	**IHZOOM[15:8]**	Inversed Horizontal Zoom Ratio (= VIAS/VOAS)	

0x0077		SCALER_IHZOOM_LSB (Default: 0x55)	R/W
7:0	**IHZOOM[7:0]**	Inversed Horizontal Zoom Ratio (= VIAS/VOAS)	

0x0078		SCALER_HSTR_OFFSET (Default: 0x00)	R/W
7:5		Reserved	
4:0	**HSTR_OFFSET**	Always 0 Setting	

0x0079		SCALER_VSTR_OFFSET (Default: 0x00)	R/W
7:5		Reserved	
4:0	**VSTR_OFFSET**	Always 0 Setting	

0x007A		SCALER_FILTER_SELECT (Default: 0x04)	R/W
7:6	**HFSEL**	Horizontal Scaling Filter Select	
5:4	**VFSEL**	Vertical Scaling Filter Select	
3	**DP_ARCH**	Scaler Frequency Control Select 0: Normal Data Control 1: abnormal Data Control	
2:0		Reserved	

0x007B		SCALER_VSTR_OFFSET_ODD (Default: 0x00)	R/W
7:5		Reserved	
4:0	**VSTR_OFFSET_ODD**	Always 0 Setting	

6.5 CONTRAST

0x0080		CONTRAST_CONTROL (Default: 0x17)	R/W
7:5		Reserved	
5:4	**CONT_TYPE**	Decides the ratio of the contrast control area 00: 0 ~ 0.99609375 01: 0.5 ~ 1.49609375 10: 0 ~ 1.9921875 11: 0 ~ 3.984375	
3		Reserved	
2	**BLACK_CT**	Black level control type 1: Adjust R/G/B simultaneously based on R 0: Adjust R/G/B individually	
1	**CONT_CT**	Contrast control type 0: Adjust R/G/B individually 1: Adjust R/G/B simultaneously based on R	
0	**BRIGHT_CT**	Brightness control type 0: Adjust R/G/B individually 1: Adjust R/G/B simultaneously based on R	

0x0081		CONTRAST_R_BLACK (Default: 0x00)	R/W
7:5		Reserved	
5:0	**R_BLACK**	Adjusts R Channel Black level	

0x0082		CONTRAST_G_BLACK (Default: 0x00)	R/W
7:5		Reserved	
5:0	**G_BLACK**	Adjusts G Channel Black level	

0x0083		CONTRAST_B_BLACK (Default: 0x00)	R/W
7:5		Reserved	
5:0	**B_BLACK**	Adjusts B Channel Black level	

0x0084		CONTRAST_R_CONTRAST (Default: 0x80)	R/W
7:0	**R_CONTRAST**	Adjusts R Channel Contrast level	

0x0085		CONTRAST_G_CONTRAST (Default: 0x80)	R/W
7:0	**G_CONTRAST**	Adjusts G Channel Contrast level	

0x0086		CONTRAST_B_CONTRAST (Default: 0x80)	R/W
7:0	**B_CONTRAST**	Adjusts B Channel Contrast level	

0x0087		CONTRAST_R_ BRIGHTNESS (Default: 0x00)	R/W
7:0	**R_BRIGHT**	Adjusts R Channel Brightness level	

0x0088		CONTRAST_G_ BRIGHTNESS (Default: 0x00)	R/W
7:0	**G_BRIGHT**	Adjusts G Channel Brightness level	

0x0089		CONTRAST_B_BRIGHTNESS (Default: 0x00)	R/W
7:0	**B_BRIGHT**	Adjusts B Channel Brightness level	

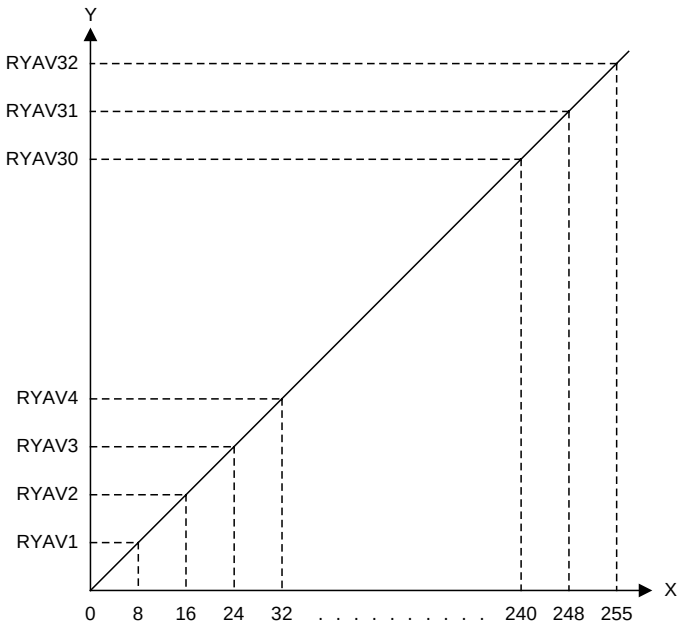
0x008A		CONTRAST_BG_COLOR_R (Default: 0x00)	R/W
7:0	**BG_COLOR_R**	R Channel Background Color If BG_COLOR_ON is HIGH, the color selected by BG_COLOR_R, BG_COLOR_G and BG_COLOR_B is displayed on the entire screen.	

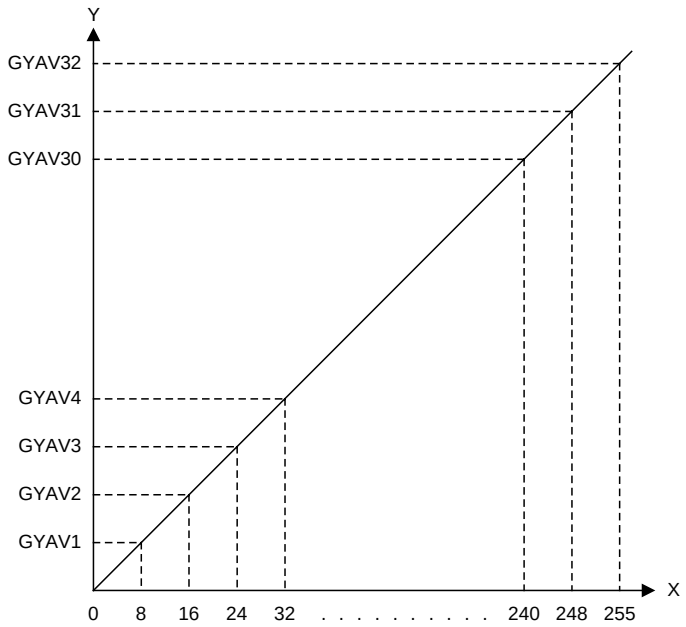
0x008B		CONTRAST_BG_COLOR_G (Default: 0x00)	R/W
7:0	**BG_COLOR_G**	G Channel Background Color If BG_COLOR_ON is HIGH, the color selected by BG_COLOR_R, BG_COLOR_G and BG_COLOR_B is displayed on the entire screen.	

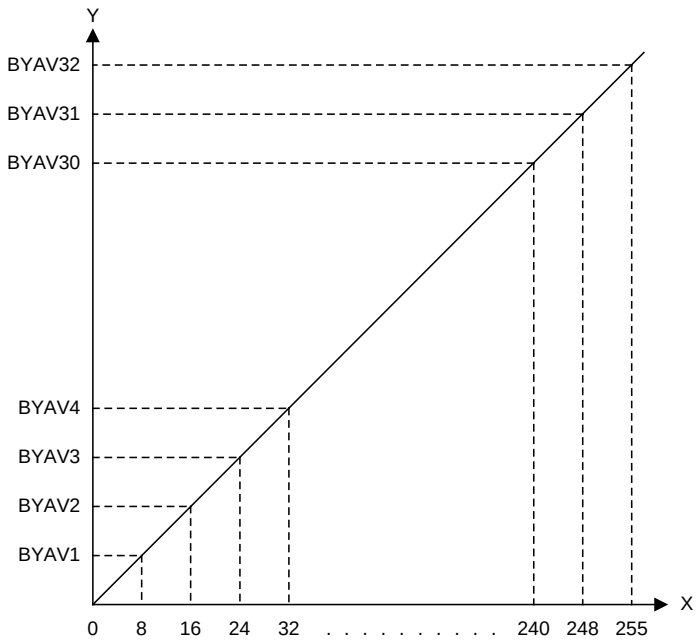
0x008C		CONTRAST_BG_COLOR_B (Default: 0x00)	R/W
7:0	**BG_COLOR_B**	B Channel Background Color If BG_COLOR_ON is HIGH, the color selected by BG_COLOR_R, BG_COLOR_G and BG_COLOR_B is displayed on the entire screen.	

6.6 GAMMA

0x0090		RAM_R_LUT_1_2	R/W
⋮		⋮	⋮
0x00AF		RAM_R_LUT_31_32	R/W
7:0	RYAV1	RED Output (Y) Axis Value for Input (X) Axis Value 8, 16, … , 240, 248, 255	8'h08
7:0	RYAV2		8'h10
7:0	RYAV3		8'h18
7:0	RYAV4		8'h20
7:0	RYAV5		8'h28
7:0	RYAV6		8'h30
7:0	RYAV7		8'h38
7:0	RYAV8		8'h40
7:0	RYAV9		8'h48
7:0	RYAV10		8'h50
7:0	RYAV11		8'h58
7:0	RYAV12		8'h60
7:0	RYAV13		8'h68
7:0	RYAV14		8'h70
7:0	RYAV15		8'h78
7:0	RYAV16		8'h80
7:0	RYAV17		8'h88
7:0	RYAV18		8'h90
7:0	RYAV19		8'h98
7:0	RYAV20		8'hA0
7:0	RYAV21		8'hA8
7:0	RYAV22		8'hB0
7:0	RYAV23		8'hB8
7:0	RYAV24		8'hC0
7:0	RYAV25		8'hC8
7:0	RYAV26		8'hD0
7:0	RYAV27		8'hD8
7:0	RYAV28		8'hE0
7:0	RYAV29		8'hE8
7:0	RYAV30		8'hF0
7:0	RYAV31		8'hF8
7:0	RYAV32		8'hFF



0x00B0		GAM_G_LUT_1_2	R/W
⋮		⋮	⋮
0x00CF		GAM_G_LUT_31_32	R/W
7:0	**GYAV1**	GREEN Output (Y) Axis Value for Input (X) Axis Value 8, 16, … , 240, 248, 255 	8'h08
7:0	**GYAV2**		8'h10
7:0	**GYAV3**		8'h18
7:0	GYAV4		8'h20
7:0	**GYAV5**		8'h28
7:0	**GYAV6**		8'h30
7:0	**GYAV7**		8'h38
7:0	**GYAV8**		8'h40
7:0	**GYAV9**		8'h48
7:0	**GYAV10**		8'h50
7:0	**GYAV11**		8'h58
7:0	**GYAV12**		8'h60
7:0	**GYAV13**		8'h68
7:0	**GYAV14**		8'h70
7:0	**GYAV15**		8'h78
7:0	**GYAV16**		8'h80
7:0	**GYAV17**		8'h88
7:0	**GYAV18**		8'h90
7:0	**GYAV19**		8'h98
7:0	**GYAV20**		8'hA0
7:0	**GYAV21**		8'hA8
7:0	**GYAV22**		8'hB0
7:0	**GYAV23**		8'hB8
7:0	**GYAV24**		8'hC0
7:0	**GYAV25**		8'hC8
7:0	**GYAV26**		8'hD0
7:0	**GYAV27**		8'hD8
7:0	**GYAV28**		8'hE0
7:0	**GYAV29**		8'hE8
7:0	**GYAV30**		8'hF0
7:0	**GYAV31**		8'hF8
7:0	**GYAV32**		8'hFF

0x00D0		GAM_B_LUT_1_2	R/W
⋮		⋮	⋮
0x00EF		GAM_B_LUT_31_32	R/W
7:0	**BYAV1**	BLUE Output (Y) Axis Value for Input (X) Axis Value 8, 16, … , 240, 248, 255 	8'h08
7:0	**BYAV2**		8'h10
7:0	**BYAV3**		8'h18
7:0	**BYAV4**		8'h20
7:0	**BYAV5**		8'h28
7:0	**BYAV6**		8'h30
7:0	**BYAV7**		8'h38
7:0	**BYAV8**		8'h40
7:0	**BYAV9**		8'h48
7:0	**BYAV10**		8'h50
7:0	**BYAV11**		8'h58
7:0	**BYAV12**		8'h60
7:0	**BYAV13**		8'h68
7:0	**BYAV14**		8'h70
7:0	**BYAV15**		8'h78
7:0	**BYAV16**		8'h80
7:0	**BYAV17**		8'h88
7:0	**BYAV18**		8'h90
7:0	**BYAV19**		8'h98
7:0	**BYAV20**		8'hA0
7:0	**BYAV21**		8'hA8
7:0	**BYAV22**		8'hB0
7:0	**BYAV23**		8'hB8
7:0	**BYAV24**		8'hC0
7:0	**BYAV25**		8'hC8
7:0	**BYAV26**		8'hD0
7:0	**BYAV27**		8'hD8
7:0	**BYAV28**		8'hE0
7:0	**BYAV29**		8'hE8
7:0	**BYAV30**		8'hF0
7:0	**BYAV31**		8'hF8
7:0	**BYAV32**		8'hFF

6.7 OSD

0x0100		OSD_FADE_ENABLE, FONT_SIZE (Default: 0 x 00)	R/W
7	**FADE_EN**	Fade function enable. 0: Disable 1: Enable	
6:5	**FADE_CTRL**	Fade function Speed Control 0: x 4 1: x 3 2: x 2 3: x 1 (for 1 frame)	
4	**OSD_EN**	OSD ON/OFF Register 0: Disable 1: Enable	
3:2	**CH_HSZ**	Determines the character horizontal size based on the default font size (12 * 18). For example, if CH_HSZ is 1, the character horizontal size is 24(12*2) pixel. 0: 12 1: 24 2: 36 3: 48	
1:0	**CH_VSZ**	Determines the character vertical size based on the default font size (12 * 18). For example, if CH_VSZ is 3, the character vertical size is 36(18*2) pixel. 0: 18 1: 36 2: 54 3: 72	

0x0101		OSD_SPACE_SIZE (Default: 0 x 00)	R/W
7		Reserved	
6:4	**COL_SP**	Controls the number of column spaces between the fonts. Column Space = COL_SP * CH_HSZ * 2 pixel	
3:0	**ROW_SP**	Controls the number of row spaces between the fonts. The number of vertical pixels is determined in accordance with the character vertical size. For example, if ROW_SP is 2 and CH_VSZ is 2, the row spaces are 4 lines.	

0x0102		OSD_HFONT (Default: 0 x 00)	R/W
7		Reserved	
6:0	**OSD_HFONT**	The number of horizontal fonts of OSD	

0x0103		OSD_VFONT (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	**OSD_VFONT**	The number of vertical fonts of OSD	

0x0104		OSD_HSP_MSB (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	**OSD_HSP[10:8]**	Horizontal start point of OSD	

0x0105		OSD_HSP_LSB(Default: 0 x 00)	R/W
7:0	**OSD_HSP[7:0]**	Horizontal start point of OSD	

0x0106		OSD_VSP_MSB (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	**OSD_VSP[10:8]**	Vertical start point of OSD	

0x0107		OSD_VSP_LSB (Default: 0 x 00)	R/W
7:0	**OSD_VSP[7:0]**	Vertical start point of OSD	

0x0108		OSD_BORDER_SHADOW_COLTROL (Default: 0 x 00)	R/W
7	**BDSH_TYPE_SEL**	Selects thickness of Border/Shadow 1: Border/Shadow is fixed to 1 pixel regardless of the character size. 0: Border/Shadow pixel interworks with the character size.	
6	**BDSH_PASS**	See Figure 21. 1: The font border/shadow is shifted to the next font if the right side of the current font is full. (When the next font is Borer/Shadow On) 0: Border/Shadow is displayed within the font area only.	
5	**G_BDSH_EN**	Controls Character Border/Shadow globally 1: Controls border/shadow with DSRAM[13] 0: Border/Shadow is disabled regardless of DSRAM[13]	
4	**BDSH_SEL**	Selects Border or Shadow when Character Border/Shadow On (G_BDSH_EN = 1 & DSRAM[13]=1) 1: Border select 0: Shadow select	
3:0	**CH_BSC**	Selects Character Border / Shadow Color as G_BDSH_EN = 1	

0x0109		OSD_MCF_CONTROL (Default: 0 x 00)	R/W
7	**MCF_SEL**	Multi Color Font Mode Select 0: MCF3 mode (3 fonts combination) 1: MCF2 mode (2 fonts combination)	
6:0	**N_MCF**	Number of Multi-Colored RAM Font	

0x010A		OSD_BLINK_CONTROL (Default: 0 x 00)	R/W
7:5		Reserved	
4:2	**BLNK_SEL**	Blink duty (visible: invisible) Select 0: 0.5sec: 0.5sec 1: 1sec: 0.5sec 2: 0.5sec: 1sec 3: 1sec: 1sec 4: 1.5sec: 1.5sec 5: 2sec: 1sec 6: 1sec: 2sec 7: 2sec: 2sec	
1	**BL_NTRA**	Blink or No_Tone_Raster 1: Blink Enable 0: No tone Raster	
0	**BLNC_C**	Blink Color inversion 1: On 0: OFF	

0x010B		OSD_HALF_TONE_CONTROL (Default: 0 x 00)	R/W
7	**G_RA_EN**	1: Global Raster Enable 0: disable (default)	
6	**CH_TONE**	Character half Toning 1: Half tone is applied to the character 0: Half tone is not applied to the character	
5	**G_HT_EN**	OSD half Toning 1:Global Half Ton Enable 0:Half Tone Disable	
4:0	**HALF_TONE_ CTRL**	OSD half Tone Level Control 0: 0% OSD 1: 1/32 % OSD 2: 2/32% OSD 3: 3/32%OSD …. 31:31/33%OSD	

0x010C		OSD DSRAM CONTROL (Default: 0x7C)	R/W
7:3		Reserved	
2	**FRONT_OSD**	FRONT OSD ON (OSD mixing before scaling) 1: ON 0: OFF (Default)	
1	**DSRAM_ATTR_ CON**	Designates the attribute or the display RAM attribute [15] 1: INT (Intensity) is selected for the display RAM attribute [15] 0: OSD HT_EN is selected for the display RAM attribute [15]	
0	**G_INT**	Global attribute is applied if INT is not selected for DSRAM attribute 1: Intensity On 0: Intensity Off	

0x010D		OSD_FTRAM_CS_START_OFFSET_ADDR_MSB (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	**FTRAM_CS_ START_ADDR[8]**	Designates the Font RAM Checksum Start offset Address	

0x010E		OSD_FTRAM_CS_START_OFFSET_ADDR_LSB (Default: 0 x 00)	R/W
7:0	**FTRAM_CS_START _ADDR[7:0]**	Designates the Font RAM Checksum Start offset Address	

0x010F		OSD_FTRAM_CS_END_OFFSET_ADDR_MSB (Default: 0 x 11)	R/W
7:5		Reserved	
4:0	**FTRAM_CS_END_ ADDR[8]**	Designates the Font RAM Checksum End Offset Address	

0x0110		OSD_FTRAM_CS_END_OFFSET_ADDR_LSB (Default: 0 x FF)	R/W
7:0	**FTRAM_CS_END_ ADDR[7:0]**	Designates the Font RAM Checksum End Offset Address	

0x0111		FTRAM_CHECKSUM_MSB	RO
7:4		Reserved	
3:0	**FTRAM_ CHECKSUM[11:8]**	Font RAM Checksum, Read Only	

0x0112		FTRAM_CHECKSUM_LSB	RO
7:0	FTRAM_ CHECKSUM[7:0]	Font RAM Checksum, Read Only	

0x0113		DSRAM_CS_START_OFFSET_ADDR_MSB (Default: 0 x 00)	R/W
7:1		Reserved	
0	DSRAM_CS_ START_ADDR[8]	Designates the Display RAM Checksum Start Offset Address	

0x0114		DSRAM_START_OFFSET_ADDR_LSB (Default: 0 x 00)	R/W
7:0	DSRAM_CS_START _ADDR[7:0]	Designates the Display RAM Checksum Start Offset Address	

0x0115		DSRAM_CS_END_OFFSET_ADDR_MSB (Default: 0 x 01)	R/W
7:1		Reserved	
0	DSRAM_CS_ END_ADDR[8]	Designates the Display RAM Checksum End Offset Address	

0x0116		DSRAM_CS_END_OFFSET_ADDR_LSB (Default: 0 x C1)	R/W
7:0	DSRAM_CS_ END_ADDR[7:0]	Designates the Display RAM Checksum End Offset Address	

0x0117		DSRAM_CHECKSUM_MSB	RO
7:0	DSRAM_ CHECKSUM[15:8]	Displays RAM Checksum, Read Only	

0x0118		DSRAM_CHECKSUM_LSB	RO
7:0	DSRAM_ CHECKSUM[7:0]	Displays RAM Checksum, Read Only	

0x0119		OSD_RAM_CHECKSUM_END_FLAG	RO
7:2		Reserved	
1	DSRAM_CS_ END_FLAG	0 → 1 at the end of display RAM checksum	
0	FTRAM_CS_ END_FLAG	0 → 1 at the end of front RAM checksum	

0x011A		MEMORY CHECKSUM & CLEAR (Default: 0 x 00)	R/W
7:4		Reserved	
3	**DSRAM_ CHECKSUM_EN**	DSRAM CHECKSUM START	
2	**FTRAM_ CHECKSUM_EN**	FTRAM CHECKSUM START	
1	**DSRAM_CLRN**	DSRAM Clear	
0		Reserved	

0x0120		OSD_LUT0 (Default: 0 x 00)	R/W
7:0	**LUT0[7:0]**	Look Up Table #0	

0x0121		OSD_LUT1 (Default: 0 x 00)	R/W
7:0	**LUT1[7:0]**	Look Up Table #1	

0x0122		OSD_LUT2 (Default: 0 x 00)	R/W
7:0	**LUT2[7:0]**	Look Up Table #2	

0x0123		OSD_LUT3 (Default: 0 x 00)	R/W
7:0	**LUT3[7:0]**	Look Up Table #3	

0x0124		OSD_LUT4 (Default: 0 x 00)	R/W
7:0	**LUT4[7:0]**	Look Up Table #4	

0x0125		OSD_LUT5 (Default: 0 x 00)	R/W
7:0	**LUT5[7:0]**	Look Up Table #5	

0x0126		OSD_LUT6 (Default: 0 x 00)	R/W
7:0	**LUT6[7:0]**	Look Up Table #6	

0x0127		OSD_LUT7 (Default: 0 x 00)	R/W
7:0	**LUT7[7:0]**	Look Up Table #7	

0x0128		OSD_LUT8 (Default: 0 x 00)	R/W
7:0	**LUT8[7:0]**	Look Up Table #8	

0x0129		OSD_LUT9 (Default: 0 x 00)	R/W
7:0	**LUT9[7:0]**	Look Up Table #9	

0x012A		OSD_LUT10 (Default: 0 x 00)	R/W
7:0	**LUT10[7:0]**	Look Up Table #10	

0x012B		OSD_LUT11 (Default: 0 x 00)	R/W
7:0	**LUT11[7:0]**	Look Up Table #11	

0x012C		OSD_LUT12 (Default: 0 x 00)	R/W
7:0	**LUT12[7:0]**	Look Up Table #12	

0x012D		OSD_LUT13 (Default: 0 x 00)	R/W
7:0	**LUT13[7:0]**	Look Up Table #13	

0x012E		OSD_LUT14 (Default: 0 x 00)	R/W
7:0	**LUT14[7:0]**	Look Up Table #14	

0x012F		OSD_LUT15 (Default: 0 x 00)	R/W
7:0	**LUT15[7:0]**	Look Up Table #15	

6.8 BOOSTUP

0x0140		BU_X1_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**X1[10:8]**	Boost Up Calculation Area for Left Top Horizontal point	

0x0141		BU_X1_LSB (Default: 0x 00)	R/W
7:0	**X1[7:0]**	Boost Up Calculation Area for Left Top Horizontal point	

0x0142		BU_Y1_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**Y1[10:8]**	Boost Up Calculation Area for Left Top Vertical point	

0x0143		BU_Y1_LSB (Default: 0x 00)	R/W
7:0	**Y1[7:0]**	Boost Up Calculation Area for Left Top Vertical point	

0x0144		BU_X2_MSB (Default: 0x 02)	R/W
7:3		Reserved	
2:0	**X2[10:8]**	Boost Up Calculation Area for Right Bottom Horizontal point	

0x0145		BU_X2_LSB (Default: 0xD0)	R/W
7:0	**X2[7:0]**	Boost Up Calculation Area for Right Bottom Horizontal point	

0x0146		BU_Y2_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**Y2[10:8]**	Boost Up Calculation Area for Right Bottom Vertical point	

0x0147		BU_Y2_LSB (Default: 0x F0)	R/W
7:0	**Y2[7:0]**	Boost Up Calculation Area for Right Bottom Vertical point	

0x0148		BU_X3_MSB (Default: 0x 00)	R/W
7	**DISP_AREA_SEL**	Boost Up Display Area Select 0: The value set in 0x0148 ~ 0x014F is applied to the display area. 1: The value set in 0x0140 ~ 0x0147 is applied to the display area.	
6:3		Reserved	
2:0	**X3[10:8]**	Boost Up Display Area for Left Top Horizontal point	

0x0149		BU_X3_LSB (Default: 0x00)	R/W
7:0	**X3[7:0]**	Boost Up Display Area for Left Top Horizontal point	

0x014A		BU_Y3_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**Y3[10:8]**	Boost Up Display Area for Left Top Vertical point	

0x014B		BU_Y3_LSB (Default: 0x 00)	R/W
7:0	**Y3[7:0]**	Boost Up Display Area for Left Top Vertical point	

0x014C		BU_X4_MSB (Default: 0x 02)	R/W
7:3		Reserved	
2:0	**X4[10:8]**	Boost Up Display Area for Right Bottom Horizontal point	

0x014D		BU_X4_LSB (Default: 0xD0)	R/W
7:0	**X4[7:0]**	Boost Up Display Area for Right Bottom Horizontal point	

0x014E		BU_Y4_MSB (Default: 0x 00)	R/W
7:3		Reserved	
2:0	**Y4[10:8]**	Boost Up Display Area for Right Bottom Vertical point	

0x014F		BU_Y4_LSB (Default: 0x F0)	R/W
7:0	**Y4[7:0]**	Boost Up Display Area for Right Bottom Vertical point	

0x0150		BU_ACC (Default: 0x 10)	R/W
7	**CAL_AREA_ON**	The calculation area is indicated on the screen. 0: Calculation area indication OFF 1: Calculation area indication ON	
6	**DISP_AREA_ON**	The display area is indicated on the screen. 0: Display area indication OFF 1: Display area indication ON	
5	**GRAPH_ON**	The LUT graph is displayed on the screen. 0: LUT GRAPH OFF 1: LUT GRAPH ON	
4	**BU_ST_ON**	Adaptive Contrast Control ON/OFF 0: OFF 1: ON	
3:2	**Ymax_ctrl**	Method of modifying Max value used in adaptive contrast control 0: 1/2 of the initially created Max value 1: 1/4 of the initially created Max value 2: 1/8 of the initially created Max value 3: 1/16 of the initially created Max value	
1:0	**Ymin_ctrl**	Method of modifying Min value used in adaptive contrast control 0: 1/2 of the initially created Min value 1: 1/4 of the initially created Min value 2: 1/8 of the initially created Min value 3: 1/16 of the initially created Min value	

0x0151		BU_MAX_NUM (Default: 0x 80)	R/W
7	**Ymax_num**	Minimum pixels to be found with the MAX value	

0x0152		BU_MIN_NUM (Default: 0x 80)	R/W
7	**Ymin_num**	Minimum pixels to be found with the MIN value	

0x0153		BU_MAX_MIN_ALPHA (Default: 0x 44)	R/W
7:4	**MAX_ALPHA**	Adaptive IIR Filter Gain for MAX value	
3:0	**MIN_ALPHA**	Adaptive IIR Filter Gain for MIN value	

0x0154		BU_TURN_POINT (Default: 0x 00)	R/W
7:0	**TURN_POINT**	Inflection point of the LUT ram graph	

0x0155		BU_CORING (Default: 0x 00)	R/W
7:0	**BU_CORING**	Adaptive Brightness Control Coring Value	

0x0156		BU_AVR_ALPHA_GAIN (Default: 0x 44)	R/W
7:4	**AVR_ALPHA**	Adaptive IIR Filter Gain for Average value	
3:0	**BU_GAIN**	Adaptive Brightness Control Gain value	

0x0157		DI_HTOTAL_MSB	RO
2:0	**DI_HTOTAL[10:8]**	Horizontal Input Total Pixel Value, Read Only	

0x0158		DI_HTOTAL_LSB	RO
7:0	**DI_HTOTAL[7:0]**	Horizontal Input Total Pixel Value, Read Only	

0x0159		DI_VTOTAL_ODD_MSB	RO
2:0	**DI_VTOTAL_ ODD [10:8]**	Vertical Input Total ODD Pixel Value, Read Only	

0x015A		DI_VTOTAL_ODD_LSB	RO
7:0	**DI_VTOTAL_ ODD [7:0]**	Vertical Input Total ODD Pixel Value, Read Only	

0x015B		DI_VTOTAL_EVEN_MSB	RO
2:0	**DI_VTOTAL_ EVEN[10:8]**	Vertical Input Total EVEN Pixel Value, Read Only	

0x015C		DI_VTOTAL_EVEN_LSB	RO
7:0	**DI_VTOTAL_ EVEN[7:0]**	Vertical Input Total EVEN Pixel Value, Read Only	

7. ELECTRICAL SPECIFICATION

7.1 ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	V_{DD}	1.8V V_{DD}	2.7	V
		3.3V V_{DD}	3.8	
DC Input Voltage	V_{IN}	3.3V input buffer	3.8	
		3.3V interface / 5V tolerant input buffer	6.5	
DC Output Voltage	V_{OUT}	1.8V output buffer	2.7	
		3.3V output buffer	3.8	
Latch Up Current	I_{Latch}	± 100		mA
Storage temperature	T_{STG}	Plastic	- 65 to 150	°C

7.2 RECOMMENDED OPERATION CONDITIONS

Table 5. Recommended Operating Conditions

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	V_{DD}	1.8V V_{DD}	1.8 ± 0.15	V
		3.3V V_{DD}	3.3 ± 0.3	
DC Input Voltage	V_{IN}	3.3V input buffer	3.3 ± 0.3	
		3.3V interface / 5V tolerant input buffer	3.0 ~ 5.25	
DC Output Voltage	V_{OUT}	1.8V output buffer	1.8 ± 0.15	
		3.3V output buffer	3.3 ± 0.3	
Operating Temperature	T_A	Commercial	0 to 70	°C

7.3 DC ELECTRICAL CHARACTERISTICS

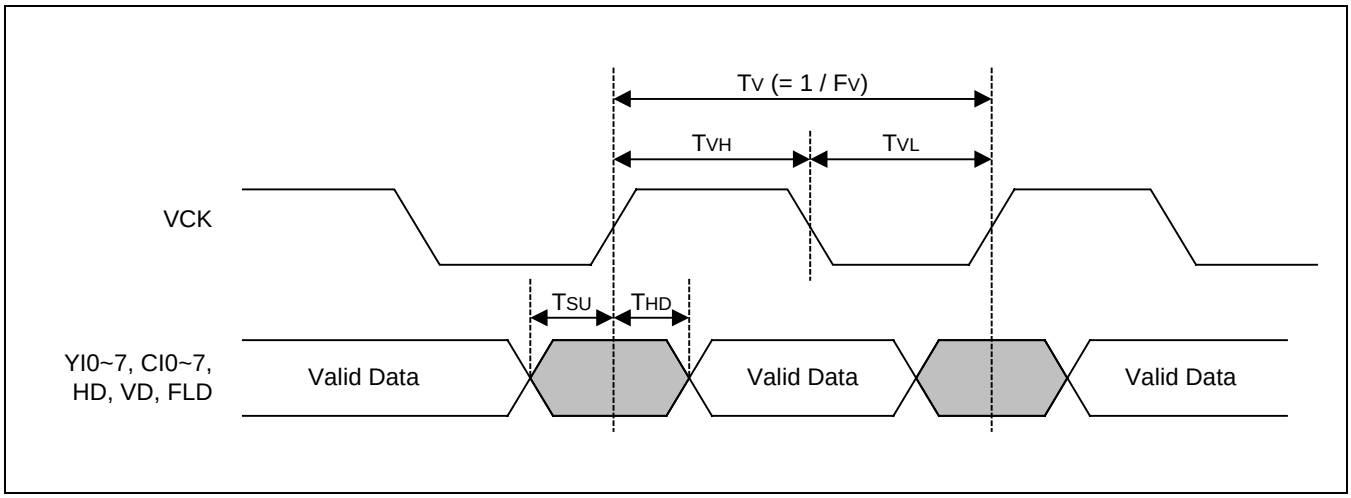
Table 6. DC Electrical Characteristics at 3.3V

V_{DD1} = 3.3V ± 0.3V, V_{DD2} = V_{DDA} = 1.8V ± 0.15V, T_A = 25°C

Item			Symbol		Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Digital Power 1		V_{DD}	V_{DD1}		3.0	3.3	3.6	V
	Digital Power 2			V_{DD2}		1.65	1.8	1.95	V
	Analog Power			V_{DDA}		1.65	1.8	1.95	V
Input Voltage	High Level		V_{IH}			2.0			V
	Low Level		V_{IL}					0.8	V
					I_{OH} = -4mA	2.4			V
					I_{OH} = -20mA	2.4			V
					I_{OL} = 4mA			0.4	V
					I_{OL} = 20mA			0.4	V
Schmitt Trigger	Positive-going threshold		VT^+		CMOS			2.0	V
	Negative-going threshold		VT^-		CMOS	0.8			V
Input Current	High Level	Input buffer	I_{IH}		V_{IN} = V_{DD}	-10		10	µA
		Input buffer with Pull-down				10	-33	60	µA
	Low Level	Input buffer	I_{IL}		V_{IN} = V_{SS}	-10		10	µA
Tri-state Output Leakage Current			I_{OZ}		V_{OUT} = V_{SS} or V_{DD}	-10		10	µA
Power Consumption			P_d		PCKO = 80MHz			600	mW

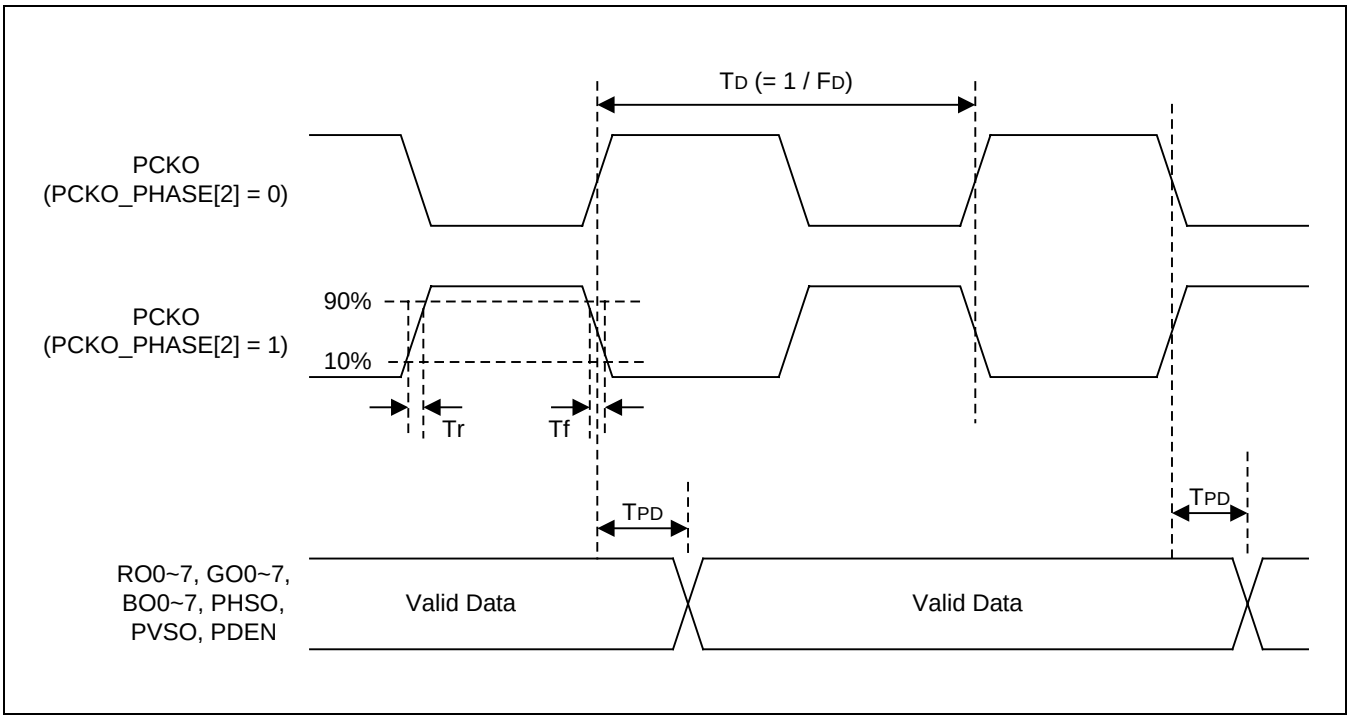
7.4 AC ELECTRICAL CHARACTERISTICS

7.4.1 Video Input Timing Characteristics



Item	Symbol	Min.	Typ.	Max.	Units
Setup Time to VCK, input YI0~7, CI0~7, HD, VD, FLD	T_{SU}	2.0			ns
Hold Time to VCK, input YI0~7, CI0~7, HD, VD, FLD	T_{HD}	2.0			ns
Input Frequency	F_V		27		MHz
Input High Duration Time	T_{VH}	3.0			ns
Input Low Duration Time	T_{VL}	3.0			ns

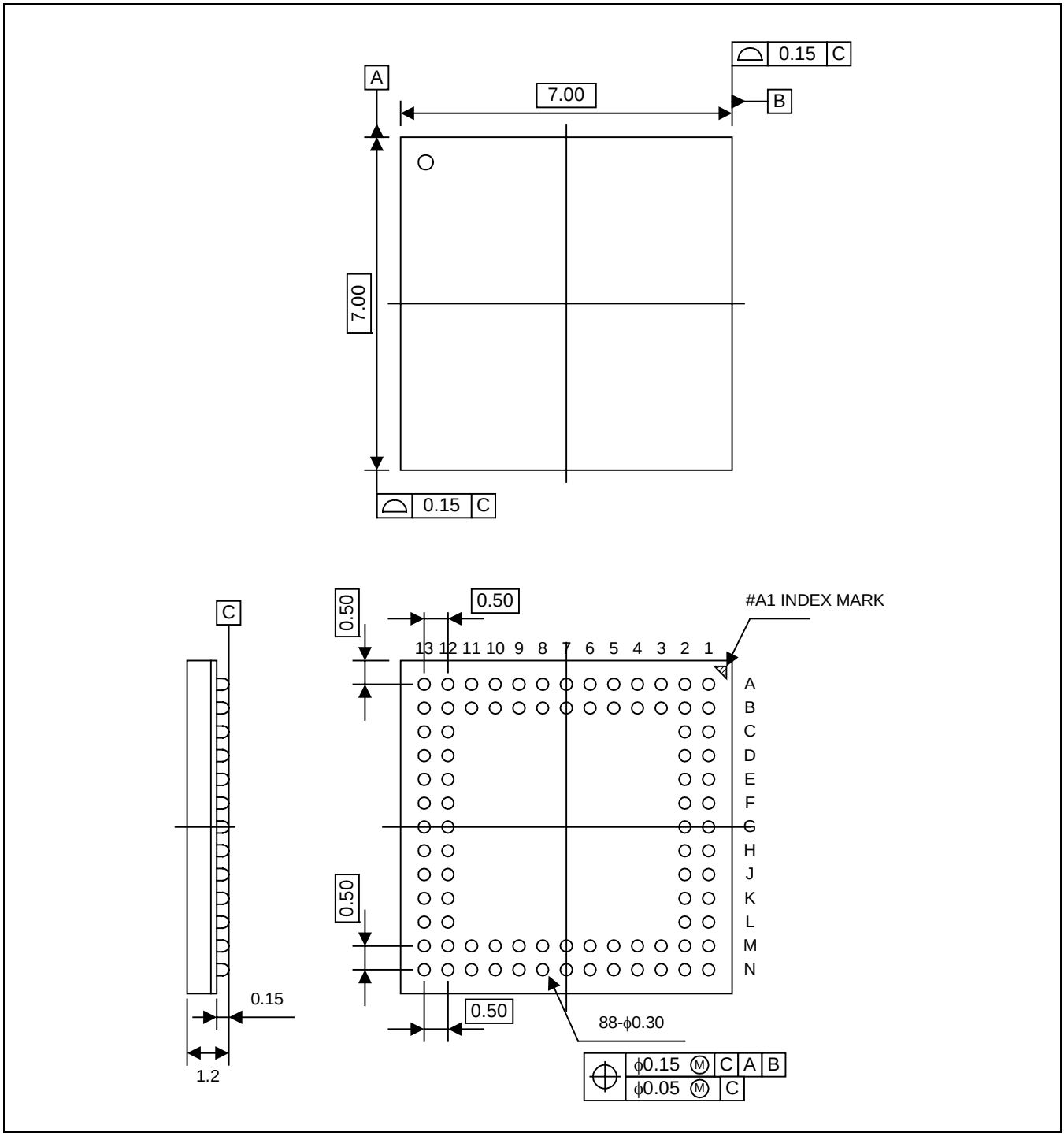
7.4.2 Display Output Timing Characteristics



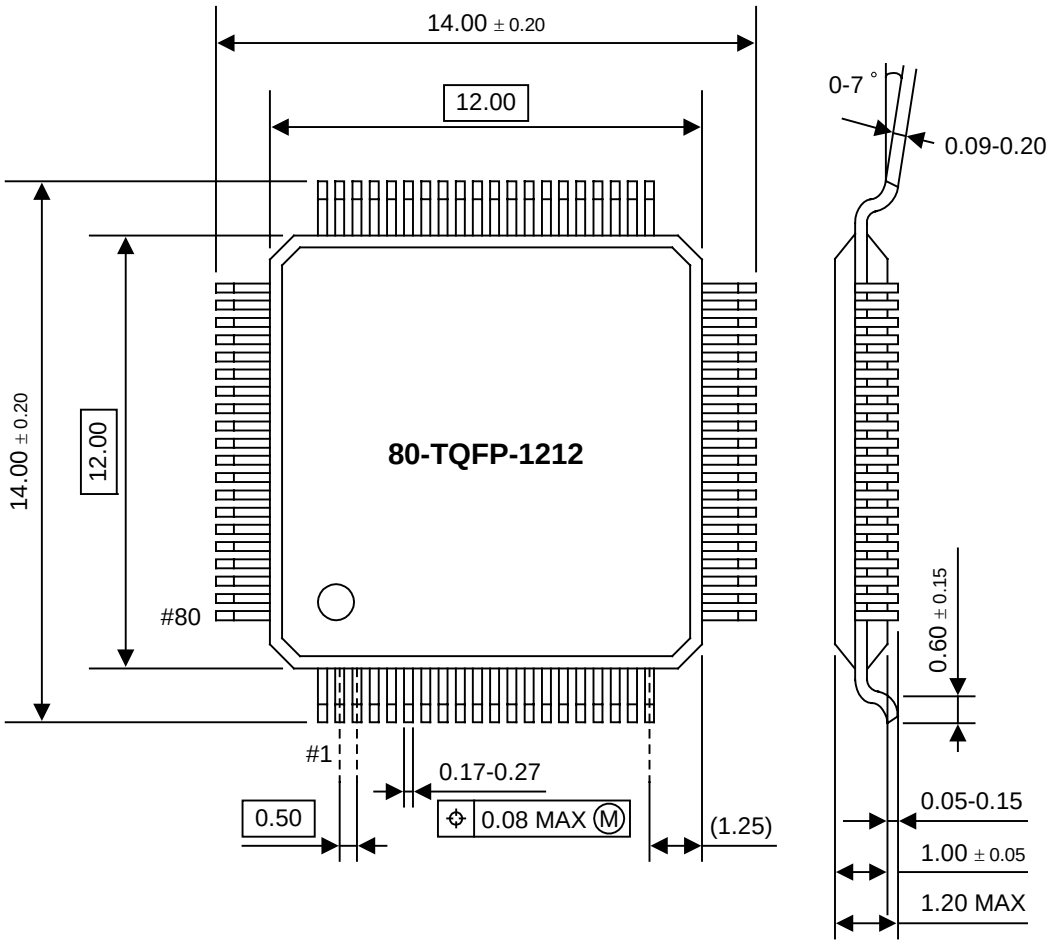
Item	Symbol	Min.	Typ.	Max.	Units
Propagation Delay Time from PCKO, Output RO0~7, GO0~7, BO0~7, PHSO, PVSO, PDEN	T_{PD}	- 3	0	3	ns
Frequency, Output Display Clock PCKO	F_D			80	MHz
Duty Cycle, Output Display Clock PCKO	C_{duty}	45	50	55	%
Rise Time, Output Display Clock PCKO	T_r			3	ns
Fall Time, Output Display Clock PCKO	T_f			3	ns

8. PACKAGE DIMENSION

8.1 88-FBGA-0707



8.2 80-TQFP-1212



NOTE: Dimensions are in millimeters.