

70A, 60V, 0.014 Ohm, N-Channel Power MOSFET

The RFK70N06 N-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49007.

Ordering Information

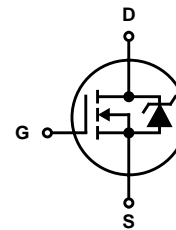
PART NUMBER	PACKAGE	BRAND
RFK70N06	TO-204AE	RFK70N06

NOTE: When ordering, use the entire part number.

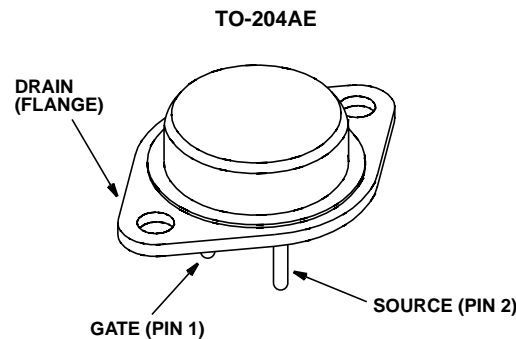
Features

- 70A, 60V
- $r_{DS(ON)} = 0.014\Omega$
- Temperature Compensating PSpice Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Symbol



Packaging



RFK70N06

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ Unless Otherwise Specified

	RFK70N06	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	60 V
Continuous Drain Current	I_D	70 A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve
Gate to Source Voltage	V_{GS}	± 20 V
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve
Power Dissipation	P_D	150 W
Linear Derating Factor		1.0 $W/^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s.	T_L	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 70\text{A}, V_{GS} = 10\text{V}$ (Figure 10)	-	-	0.014	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}, I_D \approx 70\text{A}, R_L = 0.43\Omega,$ $V_{GS} = 10\text{V}, R_G = 2.5\Omega$ (Figures 14, 17, 18)	-	-	125	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns
Rise Time	t_r		-	50	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	-	ns
Fall Time	t_f		-	15	-	ns
Turn-Off Time	t_{OFF}		-	-	125	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } 20\text{V}$	-	185	215	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V to } 10\text{V}$				
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } 2\text{V}$				
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 13)	-	3000	-	pF
Output Capacitance	C_{OSS}		-	900	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	300	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.0	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	80	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 70\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 70\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

NOTES:

- Pulse test: pulse width $\leq 300\text{ms}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width is limited by maximum junction temperature. See Transient Thermal Temperature curve (Figure 3).

Typical Performance Curves

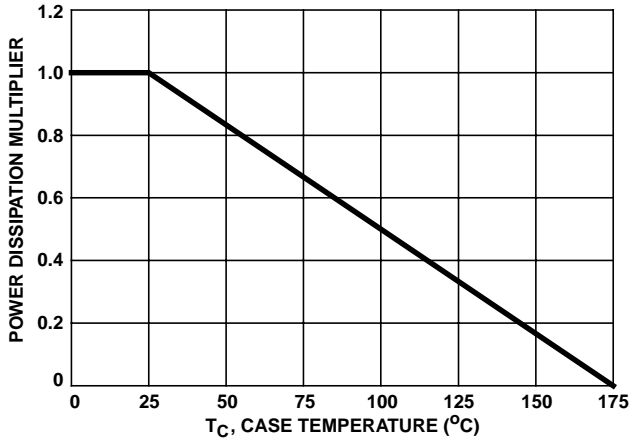


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

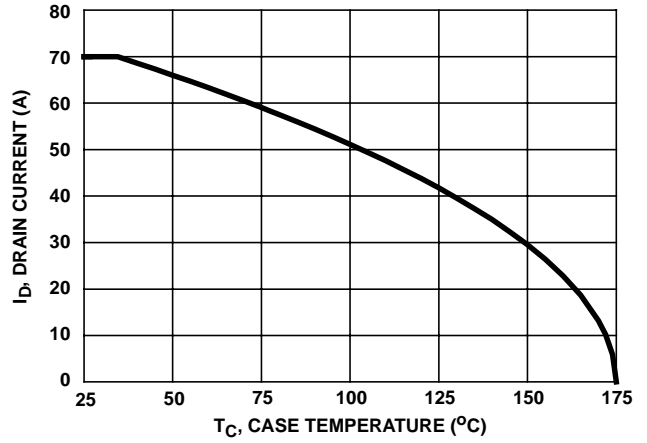


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

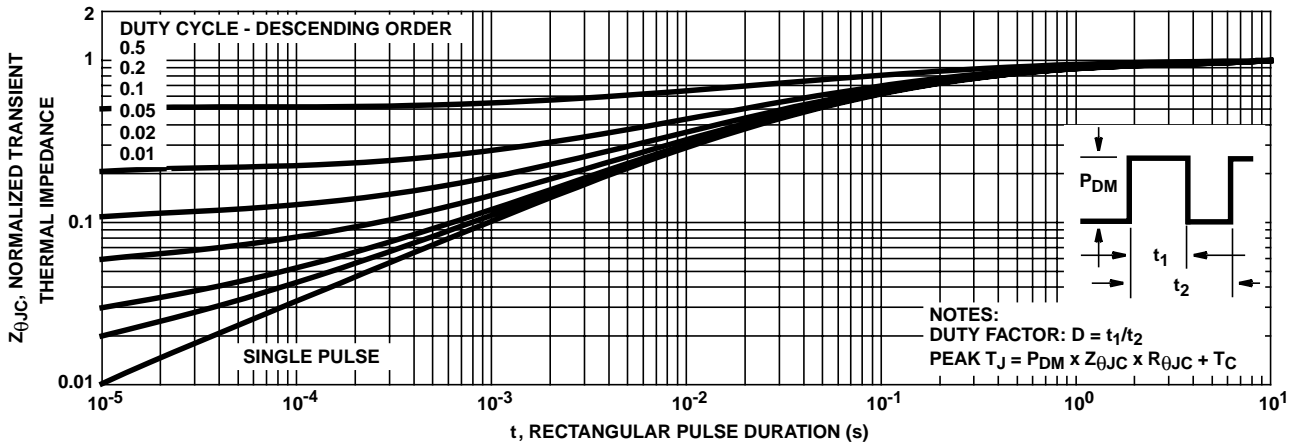


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

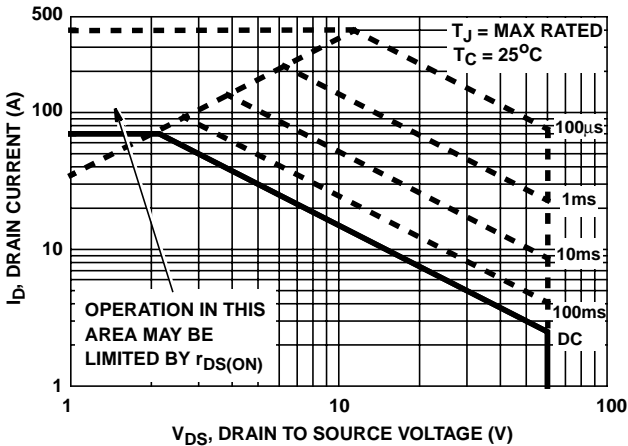


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

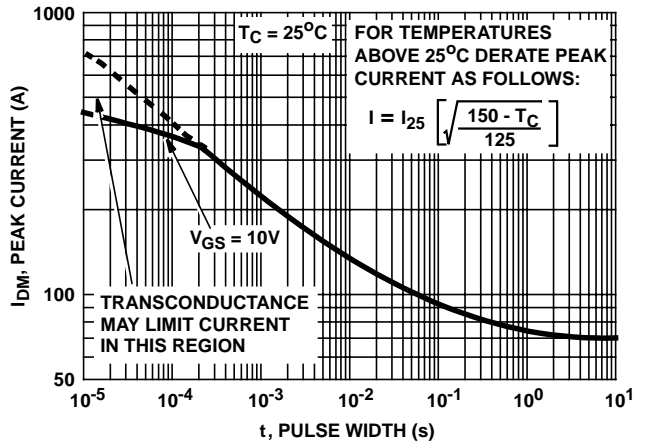
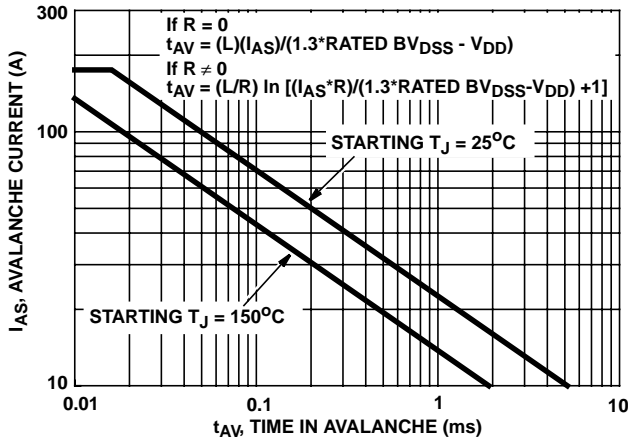


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.
FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

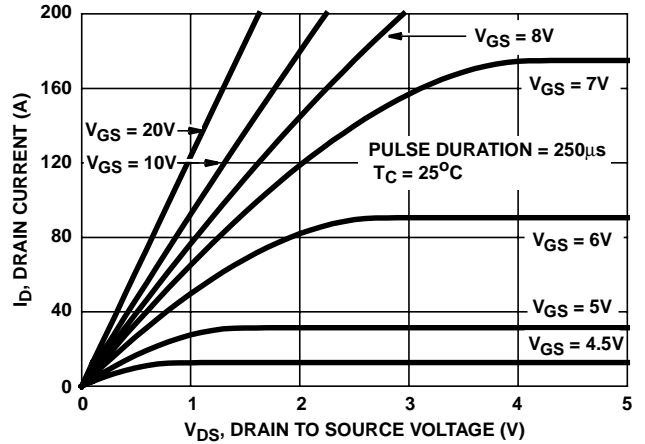


FIGURE 7. SATURATION CHARACTERISTICS

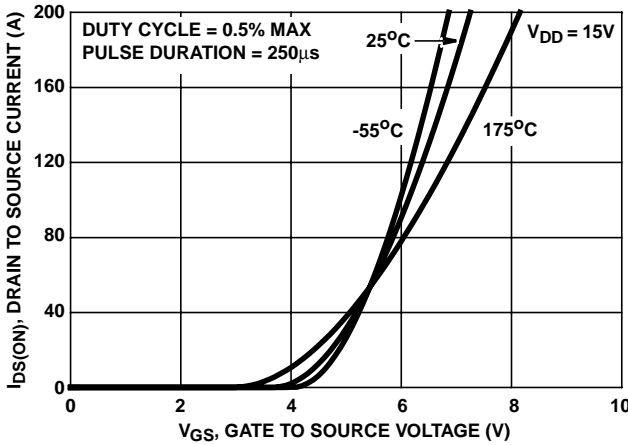


FIGURE 8. TRANSFER CHARACTERISTICS

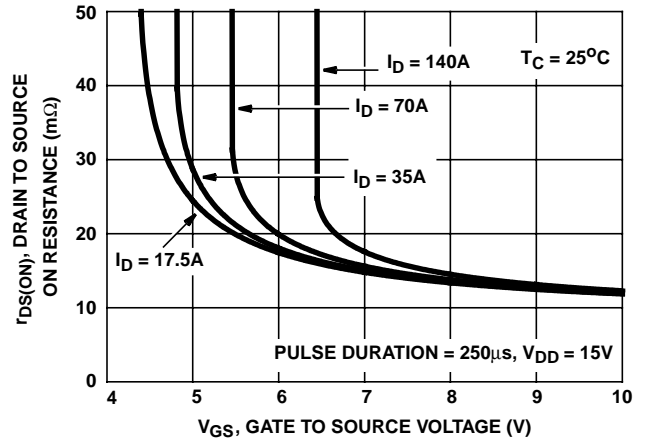


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

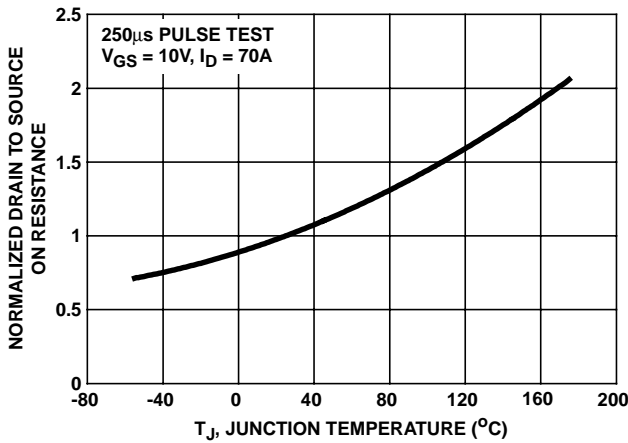


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

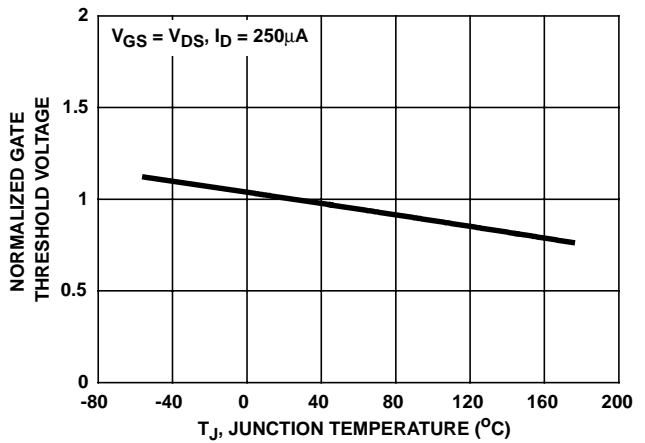


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

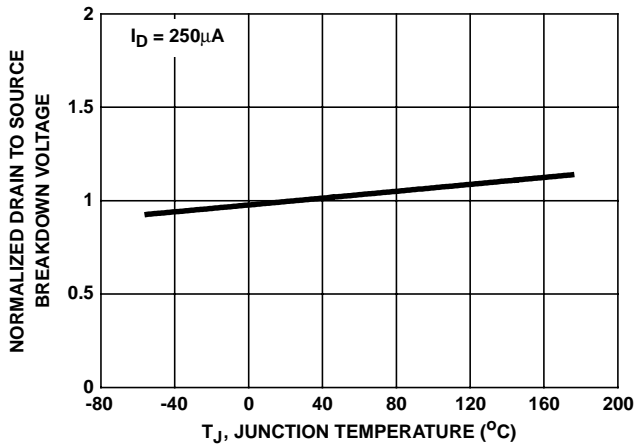


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

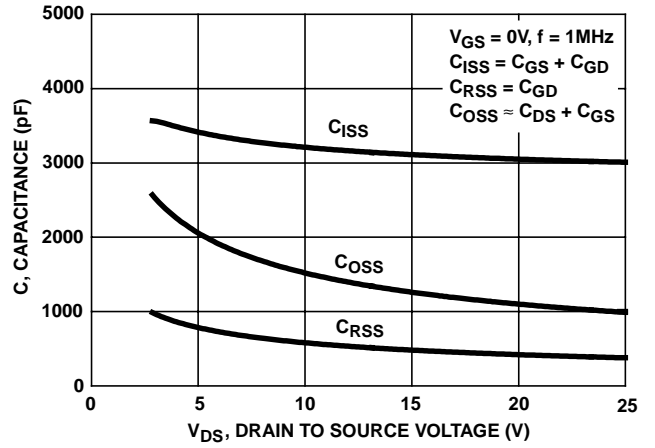
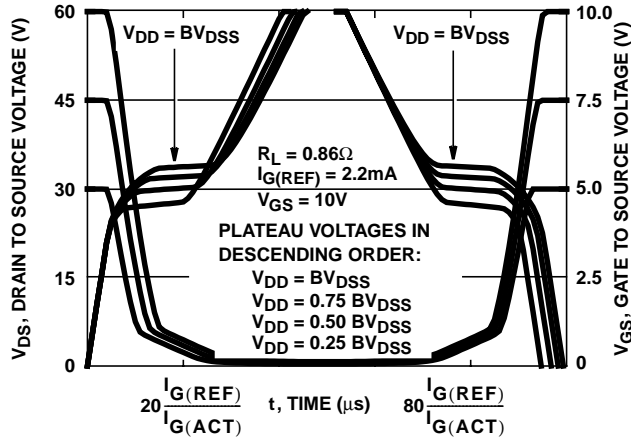


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

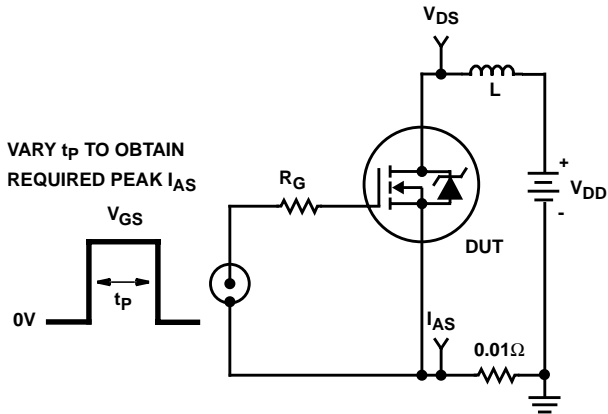


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

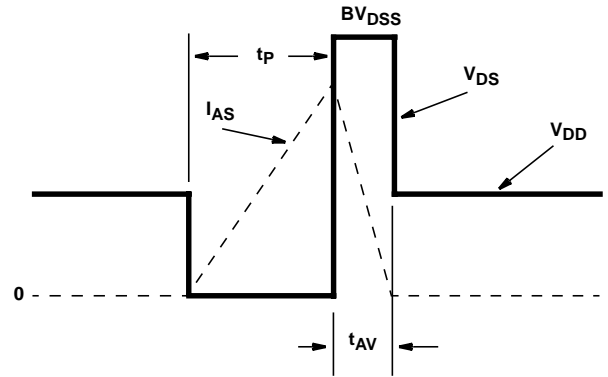


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

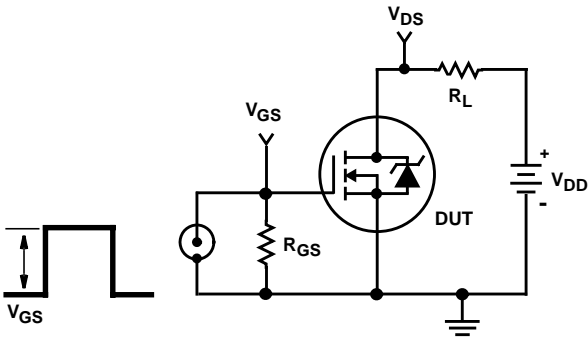


FIGURE 17. SWITCHING TIME TEST CIRCUIT

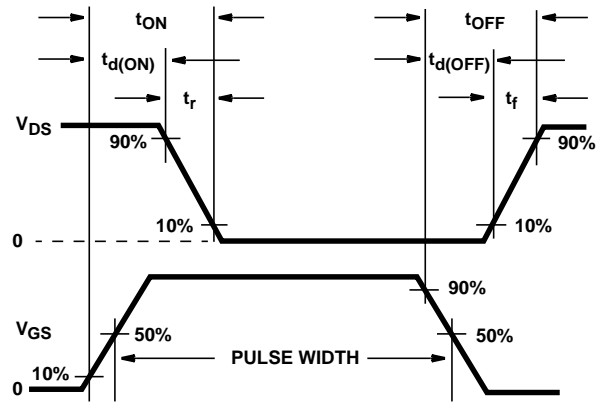


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

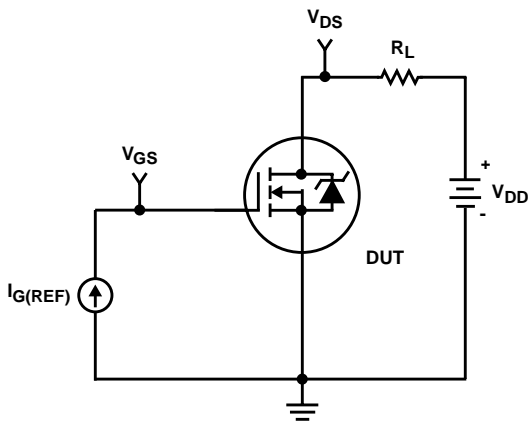


FIGURE 19. GATE CHARGE TEST CIRCUIT

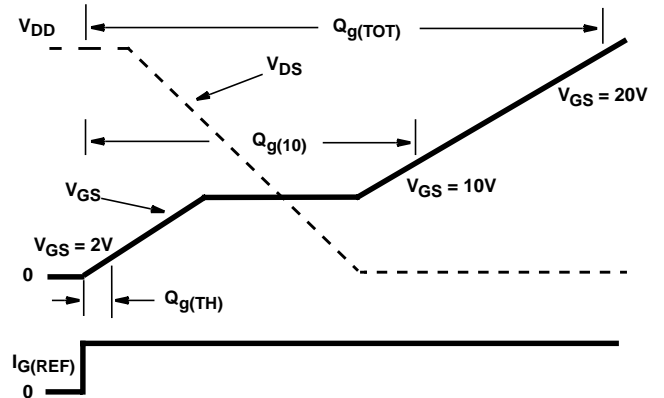


FIGURE 20. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029