LOW CURRENT LNA/MIXER

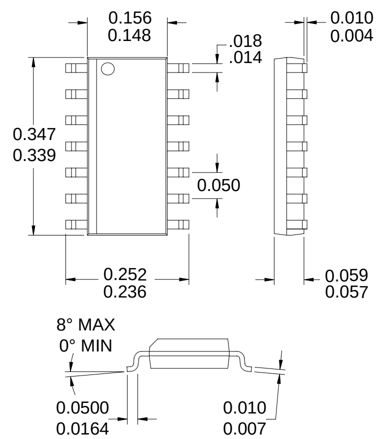
RoHS Compliant & Pb-Free Product

Typical Applications

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread-Spectrum Communication Systems
- Commercial and Consumer Systems
- 433MHz and 915MHz ISM Band Receivers
- General Purpose Frequency Conversion

Product Description

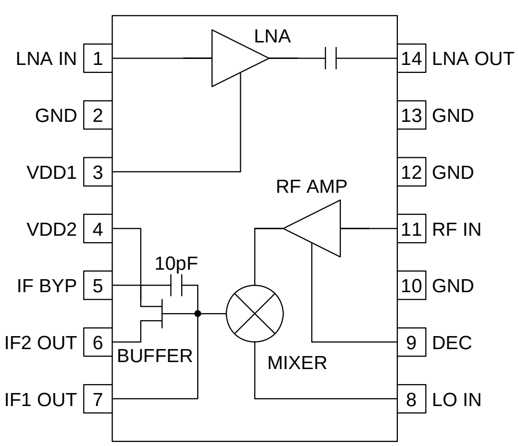
The RF2418 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, a dual-gate GaAs FET mixer, and an IF output buffer amplifier which will drive a 50Ω load. In addition, the IF buffer amplifier may be disabled and a high impedance output is provided for easy matching to IF filters with high impedances. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA section may be disabled by removing the VDD1 connection to the IC.



Package Style: SOIC-14

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- Single 3V to 6.5V Power Supply
- High Dynamic Range
- Low Current Drain
- High LO Isolation
- LNA Power Down Mode for Large Signals

Ordering Information

RF2418	Low Current LNA/Mixer
RF2418 PCBA	Fully Assembled Evaluation Board

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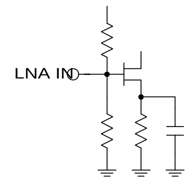
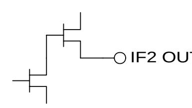
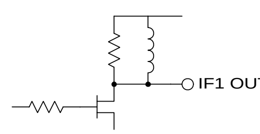
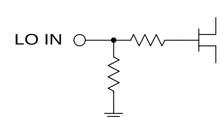
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

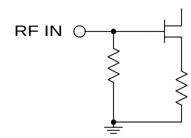
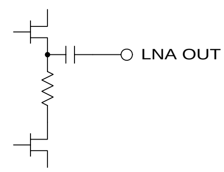
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

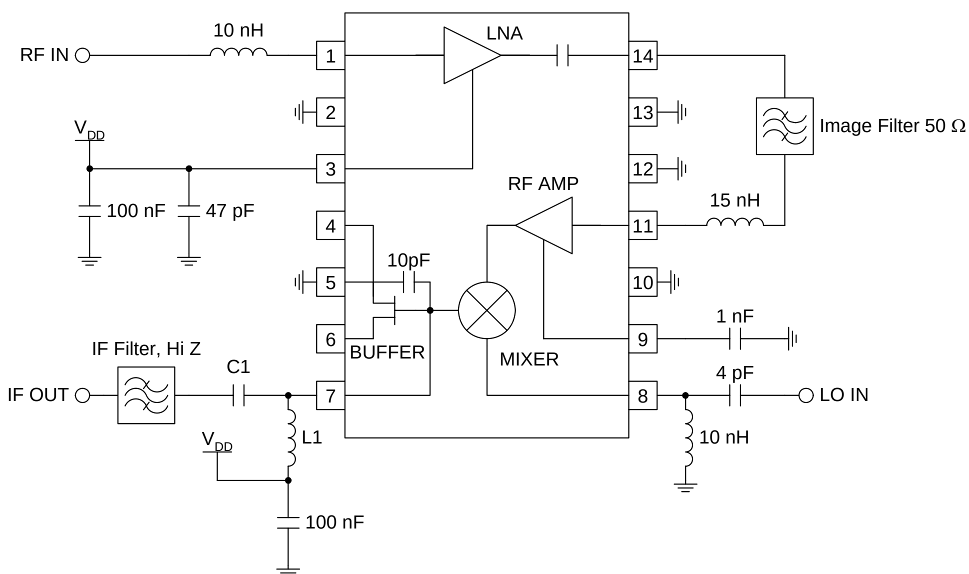
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=850MHz, LO=921MHz
RF Frequency Range		400 to 1100		MHz	
Cascade Power Gain		23		dB	High impedance output
Cascade IP_3		-13		dBm	Referenced to the input
Cascade Noise Figure		2.4		dB	Single sideband, includes image filter with 1.0dB insertion loss
First Section (LNA)					
Noise Figure		1.8	2.0	dB	
Input VSWR		1.5:1			With external series matching inductor
Input IP3	+3.0	+4.0		dBm	
Gain	13	14		dB	
Reverse Isolation		40		dB	
Output VSWR		1.5:1			
Second Section (RF Amp, Mixer, IF1)					High impedance output
Noise Figure		9.5		dB	Single Sideband
Input VSWR		1.5:1			With external series matching inductor
Input IP3		+1		dBm	
Conversion Power Gain	7	9		dB	
Output Impedance		4000‖10pF		Ω	Open Collector
Second Section (RF Amp, Mixer, IF2)					Buffered output, 50Ω load
Noise Figure		10		dB	Single Sideband
Input VSWR		1.5:1			With external series matching inductor
Input IP3	-0.5	0		dBm	
Conversion Gain	5	6		dB	
Output Impedance		30		Ω	
LO Input					
LO Frequency		300 to 1200		MHz	
LO Level		-6 to +6		dBm	
LO to RF Rejection		15		dB	
LO to IF Rejection		40		dB	With pin 5 connected to ground.
LO Input VSWR		1.3:1			In order to achieve a low VSWR match at this input, an 82Ω resistor to ground is placed in parallel with this port.
Power Supply					
Voltage	3.0		6.5	V	
Current Consumption		14		mA	V_{CC}=5.0V, LNA On, Mixer On, Buffer Off
	12	20	26	mA	V_{CC}=5.0V, LNA On, Mixer On, Buffer On
	6	9	20	mA	V_{CC}=5.0V, LNA Off, Mixer On, Buffer Off

Pin	Function	Description	Interface Schematic
1	LNA IN	A series 10nH matching inductor is necessary to achieve specified gain and noise figure at 900MHz. This pin is NOT internally DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
2	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VDD1	Supply Voltage for the LNA only. A 22pF external bypass capacitor is required and an additional 0.01μF is required if no other low frequency bypass capacitors are near by. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. For large input signals, VDD1 may be disconnected, resulting in the LNA's gain changing from +11dB to -26dB and current drain decreasing by 4mA. If the LNA is never required for use, then this pin can be left unconnected or grounded, and Pin 11 is used as the first input.	
4	VDD2	Power supply for the IF buffer amplifier. If the high impedance mixer output is being used, then this pin is not connected.	
5	IF BYP	If this pin is connected to ground, an internal 10pF capacitor is connected in parallel with the mixer output. This capacitor functions as an LO trap, which reduces the amount of LO to IF bleed-through and prevents high LO voltages at the mixer output from degrading the mixer's dynamic range. At higher IF frequencies, this capacitance, along with parasitic layout capacitance, should be parallel resonated out by the choice of the bias inductor value at pin 7. If the internal capacitor is not connected to ground, the buffer amplifier could become unstable. A ~10pF capacitor should be added at the output to maintain the buffer's stability, but the gain will not be significantly affected.	
6	IF2 OUT	50Ω buffered (open source) output port, one of two output options. Pin 7 must have a bias resistor to V_{DD} and pin 6 must have a bias resistor to ground (see Buffered Output Application Schematic) in order to turn the buffer amplifier on. Current drain will increase by approximately 8mA at 5V, and by approximately 5mA at 3V. It is recommended that these bias resistors be less than 1kΩ.	
7	IF1 OUT	High impedance (open drain) output port, one of two output options. This pin must be connected to V_{DD} through a resistor or inductor in order to bias the mixer, even when using IF2 Output. In addition, a 0.01μF bypass capacitor is required at the other end of the bias resistor or inductor. The ground side of the bypass capacitor should connect immediately to ground plane. This output is intended to drive high impedance IF filters. The recommended matching network is shunt L, series C (see the application schematic, high impedance output). This topology will provide matching, bias, and DC-blocking.	
8	LO IN	Mixer LO input. A high-pass matching network, such as a single shunt inductor (as shown in the application schematics), is the recommended topology because it also rejects IF noise at the mixer input. This filtering is required to achieve the specified noise figures. This pin is NOT internally DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.	
9	RF BYP	Connection for the external bypass capacitor for the mixer RF input preamp. 1000pF is recommended. The trace length between the pin and the capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	

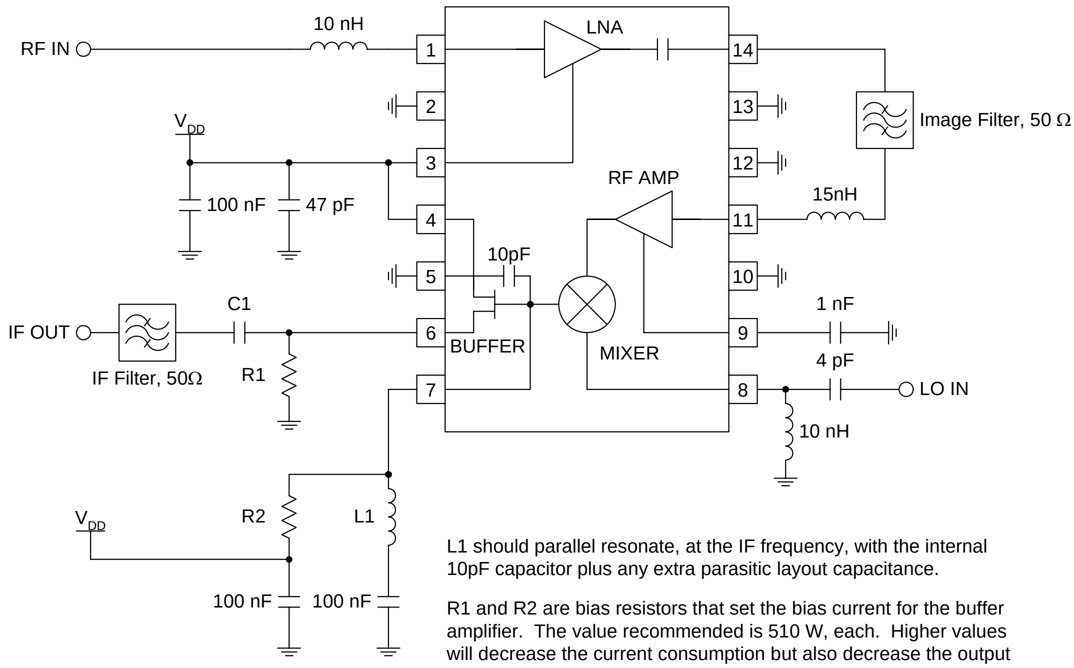
Pin	Function	Description	Interface Schematic
10	GND	Same as pin 2.	
11	RF IN	Mixer RF Input port. For a 50Ω match at 900MHz use a 15nH series inductor. This pin is NOT internally DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 22pF is recommended.To minimize the mixer's noise figure, it is recommended to have a RF bandpass filter before this input. This will prevent the noise at the image frequency from being converted to the IF.	
12	GND	Same as pin 2.	
13	GND	Same as pin 2.	
14	LNA OUT	50Ω output. Internally DC-blocked.	

Application Schematic
High Impedance Output Configuration
850MHz



L1 and C1 are picked to match the mixer's output impedance (4 kΩ II 10 pF) to the IF filter's impedance, at the IF frequency. C1 also serves as a DC block, in case the IF filter is not an open circuit at DC.

Application Schematic
Buffered Output Configuration
850 MHz



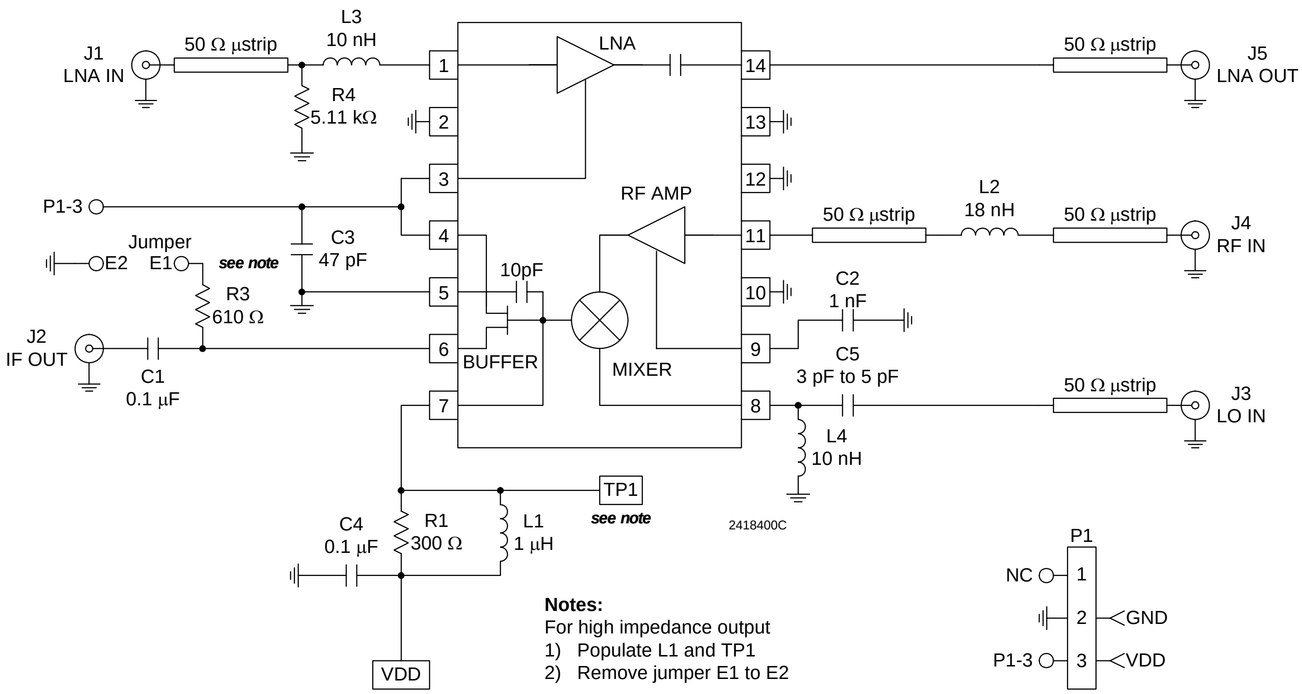
L1 should parallel resonate, at the IF frequency, with the internal 10pF capacitor plus any extra parasitic layout capacitance.

R1 and R2 are bias resistors that set the bias current for the buffer amplifier. The value recommended is 510 W, each. Higher values will decrease the current consumption but also decrease the output level at which voltage clipping begins to occur. At lower IF frequencies, where the internal 10 pF capacitor does not roll off the conversion gain, L1 may be eliminated.

C1 is a blocking capacitor, in case the IF filter's input is not an open circuit at DC.

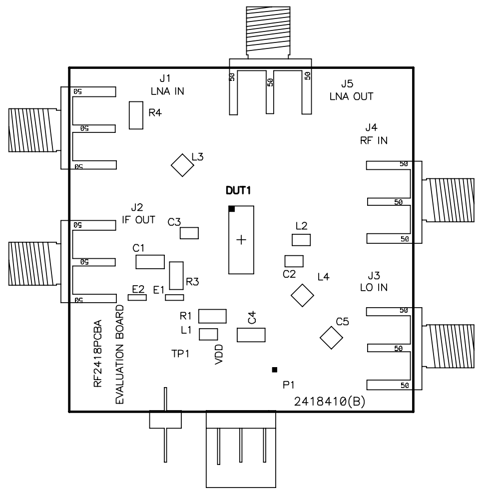
Evaluation Board Schematic
RF=850MHz, IF=71MHz

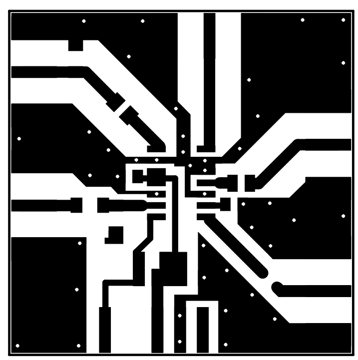
(Download Bill of Materials from www.rfmd.com.)



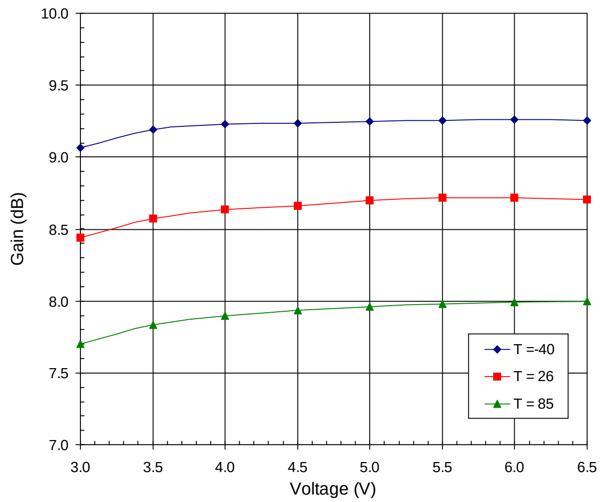
Notes:
For high impedance output
1) Populate L1 and TP1
2) Remove jumper E1 to E2

Evaluation Board Layout
Board Size 1.52” x 1.52”
Board Thickness 0.031”, Board Material FR-4

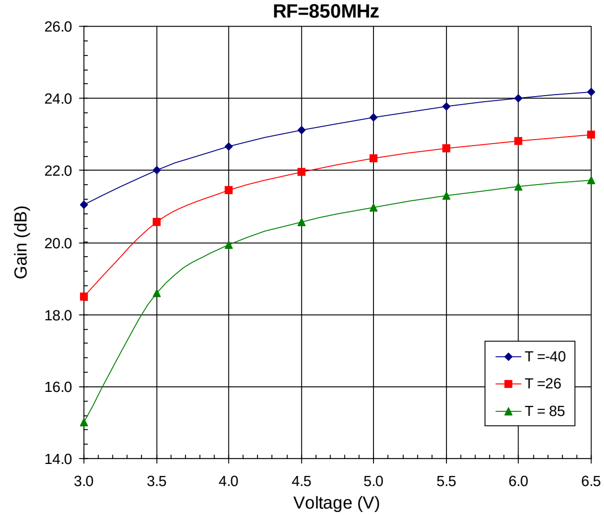




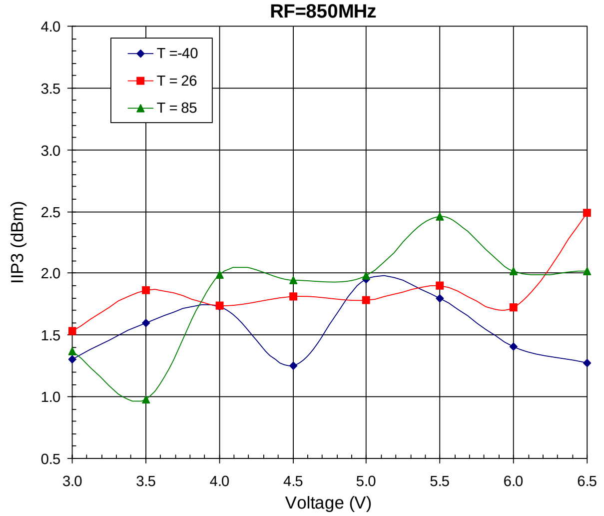
High Impedance Mixer Gain versus Voltage, RF=850MHz



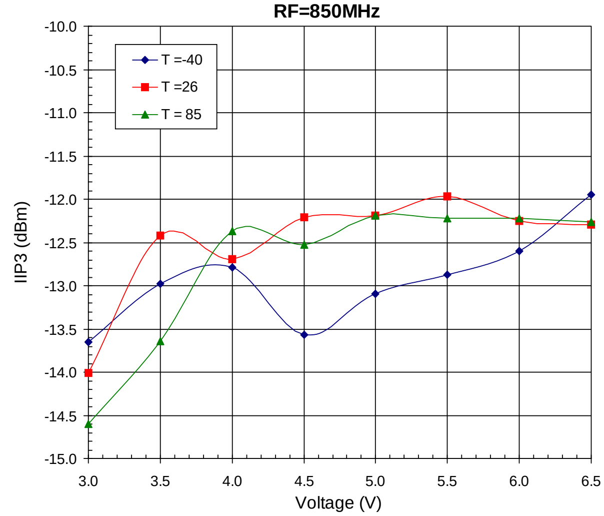
High Impedance Casc. Gain versus Voltage, RF=850MHz



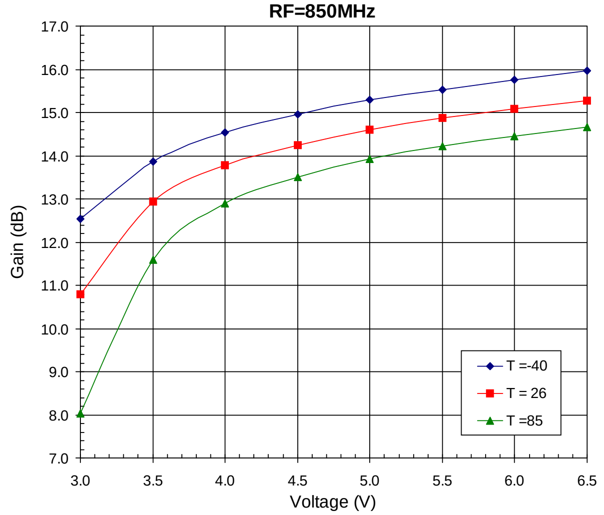
High Impedance Mixer Input IP3 versus Voltage, RF=850MHz



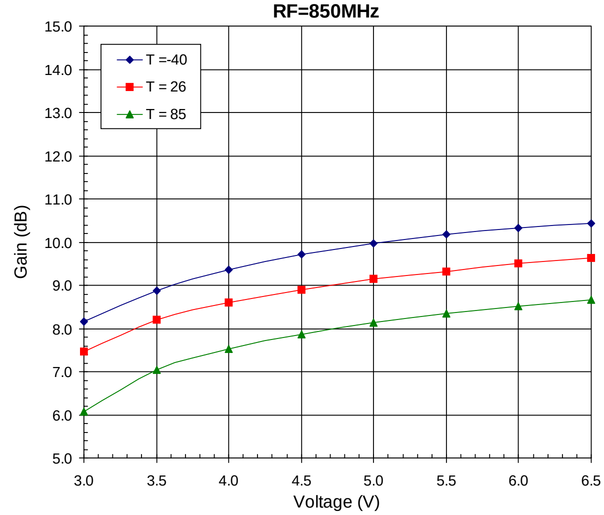
High Impedance Casc. Input IP3 versus Voltage, RF=850MHz



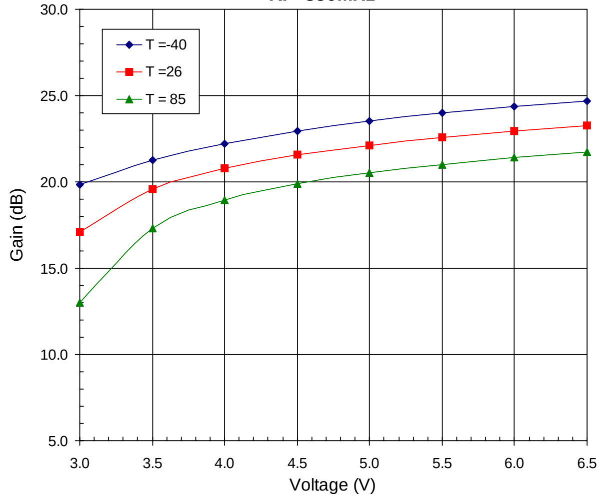
Buffered LNA Gain versus Voltage, RF=850MHz



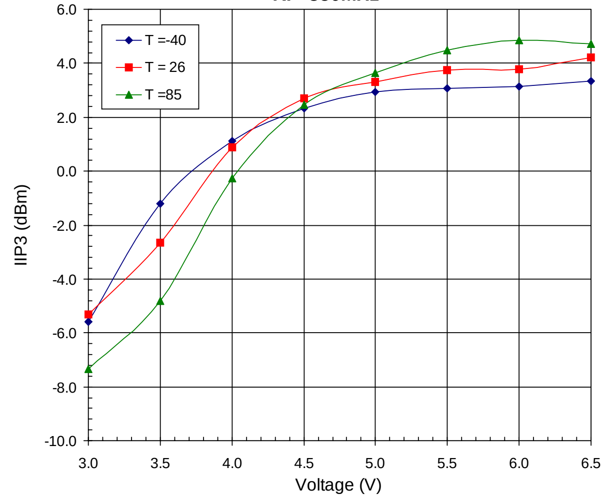
Buffered Mixer Gain versus Voltage, RF=850MHz



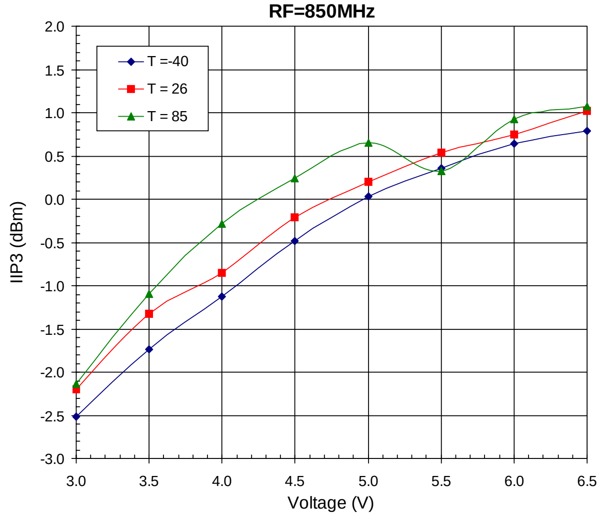
Buffered Casc. Gain versus Voltage, RF=850MHz



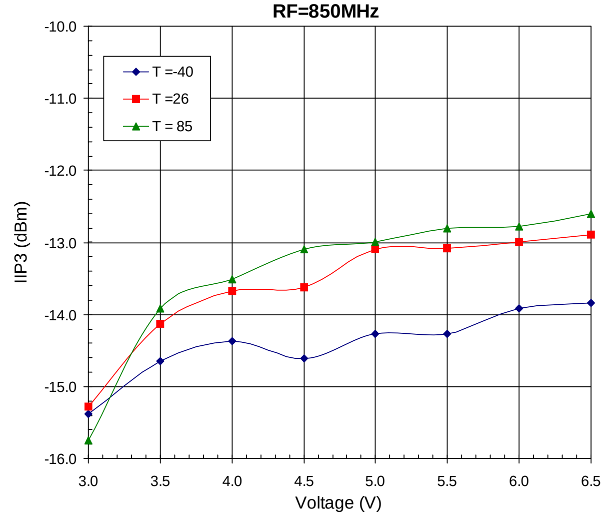
Buffered LNA Input versus Voltage, RF=850MHz



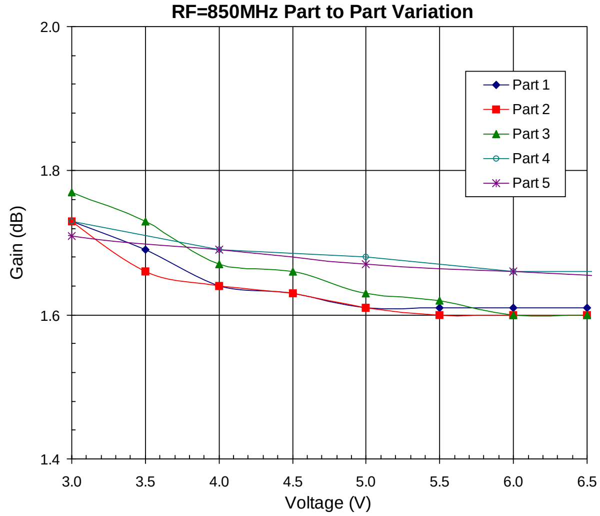
Buffered Mixer Input IP3 versus Voltage, RF=850MHz



Buffered Casc. Input IP3 versus Voltage, RF=850MHz



Buffered LNA Noise Figure versus Voltage, RF=850MHz Part to Part Variation



Buffered Mixer Noise Figure versus Voltage, RF=850MHz Part to Part Variation