General Description

The RA0512J is a full frame CCD sensor designed specifically for use in astronomy, spectroscopy and related scientific imaging applications. Its combination of very low noise and low dark current make it ideal for low light level, high dynamic range, and high resolution applications.

The imager is structured in a serial-parallel-serial configuration so charge packets (imaging data) in the vertical (parallel) registers can be shifted either up or down to two identical horizontal (serial) shift registers. One is at the top and another is at the bottom of the array. Three-phase clocks are needed to drive both vertical and horizontal shift registers.

The array is available in a 40-pin ceramic package as shown in Figure 1. Package dimensions are shown in Figure 7. It is available with a quartz window or unwindowed. The device is indifferent to its orientation in a circuit due to the symmetry of the pinout (see Table 1 for complete pinout description).

Note: While the RA0512J has been designed to be resistant to electro-static discharge, ESD, damage, it still can be damaged from such discharges. Standard electronic ESD precautions should be observed when handling and storing this device.

Key Features

- 262,144 picture elements (pixels) in a 512 x 512 configuration
- 27 µm square pixels
- 3-Phase buried channel process
- On-chip output amplifier for low noise and high speed readout
- High dynamic range: over 98 dB at -110°C (183°K)
- Serial-parallel-serial configuration for selectable bidirectional readout
- Usable spectral response from 450 nm to 1050 nm

MPP Operation

A major source of dark current in devices such as this originates in surface states at the Si-SiO_2 interface. A unique design and process enables the RA0512J to be run in the "Multi-Pinned Phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface of the sensing area is inverted. As a result, the surface will not be depleted and surface states will not generate dark current. Dark current densities of less than 50 pa/cm^2 have been achieved using the MPP mode of operation, resulting in integration times of more than 30 seconds at room temperature.

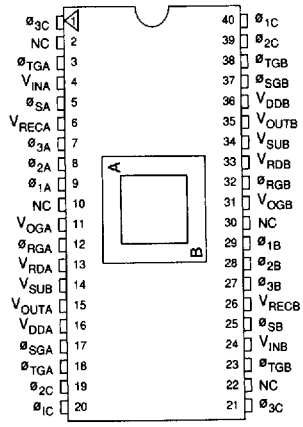

Figure 1A. Pinout Configuration, DIP

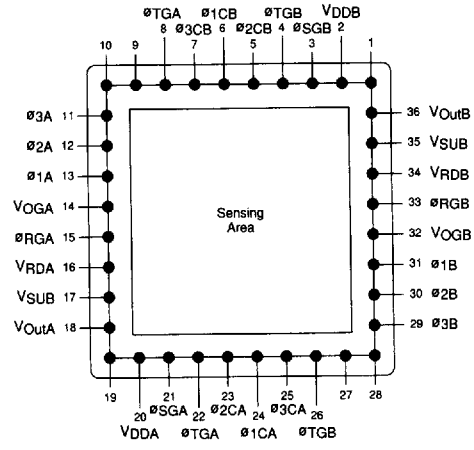

Figure 1B. Pinout Configuration, Metal Package

Functional Description

Imaging Area

The imaging area is an array of 512 columns (vertical CCD shift registers) which are isolated from each other by 5 µm channel-stop regions. Each column has 512 picture elements. The pixel size is 27 µm x 27 µm. The total imaging area is 13.8 mm x 13.8 mm. Typical spectral response as a function of wavelength is shown in Figure 2.

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three-electrode

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groups are driven by three-phase clocks ($ø_{1C}$ - $ø_{3C}$) brought in from both edges of the array to improve clock electrode response time.

Charge packets (imaging data) in the vertical registers can be shifted either up or down to the top or bottom horizontal registers by interchanging two of the three phases ($ø_{1C}$ and $ø_{2C}$). See Figure 3 for functional diagram.

A transfer gate ($ø_{TG}$) is provided at the interface of the vertical and horizontal registers for controlling charge flow. Charge flow is from $ø_{3C}$ gate of the vertical shift register into $ø_2$ and $ø_3$ gates of the horizontal shift register. The control function is performed by pulsing the transfer gate either high or low to permit or prevent the charge flow from the vertical register into the horizontal register for readout.

When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates ($ø_{1C}$ and $ø_{2C}$). When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full-frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From there, charge can be shifted serially to the output amplifier.

A mechanical shutter is needed to shield the array from incident light during the read out process. A strobe illumination could be used to simulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless such shuttering is provided.

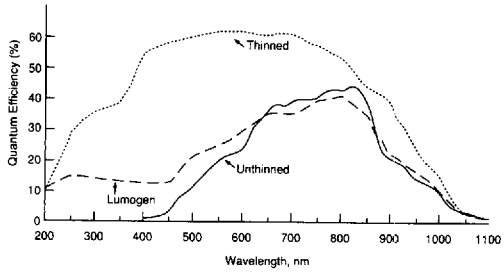

Figure 2. Typical Spectral Response

Horizontal Registers

There are two identical horizontal shift registers which are driven by three-phase clocks($ø_{1A}$-$ø_{3A}$, $ø_{1B}$-$ø_{3B}$), one at the top and one at the bottom of the imaging area. Each shift register has 512 stages plus an extension of 50 stages. As a result, amplifier power is dissipated more efficiently and dark current generated by localized heating is minimized.

Summing Mode

At the end of each serial register, there is an output summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 49th extra stage of the horizontal registers and prior to the DC biased gate (V_{OG}) as shown in Figure 5. The summing gate (SG) can be clocked with one of the serial clock phases or with its own clock generator (see Figure 6 for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2 x 2) contiguous pixels from the imaging section. It effectively reduces the 512 x 512 device to a 256 x 256 array and increases the pixel size by 4 times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast, or a low signal-to-noise ratio. There is, of course, a loss in resolution which accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier which is located at the end of each extended serial shift register. The amplifier is a single-stage buried-channel transistor (Figure 5) designed to operate in the source-follower configuration with an off-chip load resistor (1KΩ - 20KΩ). It has a bandwidth of approximately 5 MHz with a 10 pF load.

Timing Requirements

The timing recommended to run the RA0512J imager in the low speed and low noise mode of operation is shown in Figures 4A and 4B. Other types of three-phase clocks can also be used to drive both the vertical and horizontal registers. For example, 50% duty cycle, three-phase clocks can be used to drive the horizontal register for high-speed operation. However, the large full well capacity and low noise floor will be sacrificed.

Figure 4A shows the timing of the horizontal three-phase clocks, summing well clock, reset clock, and external clamping and sampling clocks. To achieve high charge transfer efficiency and high full well capacity, serial clocks must overlap by more than 1 µs. In addition, the rise and fall times of the three-phase clocks may be more than 300 ns to prevent possible injection of spurious charge into the CCD channel. After the three-phase clock transitions, the clocks are held steady to provide a quiet period for signal readout. During this quiet period, the output amplifier is clamped and the signal charge in the summing well is transferred into the output sensing node. The output signal is then sampled and the sensing node is reset.

This timing is repeated 562 (or more) times to allow the readout of one complete line of the image. The video signal from one pixel is also shown in Figure 4A.

Figure 4B shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks may be 300 ns or longer. All clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during an integration, all clocks must be held low for MPP mode. The clocks should repeat 562 times (or more) to read out the entire image.

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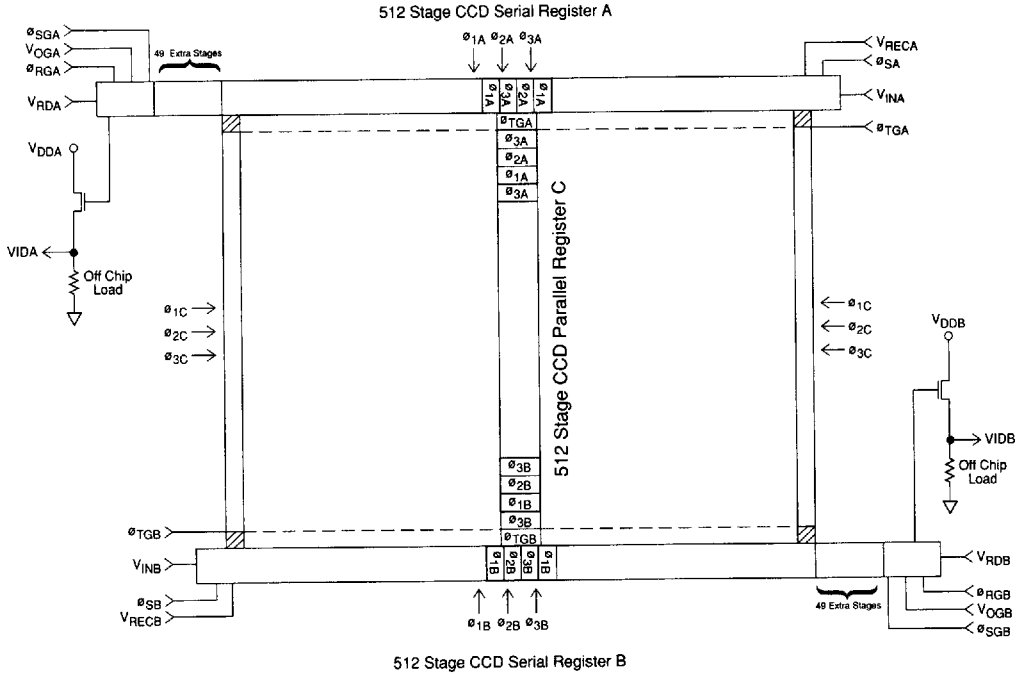

Figure 3. Functional Diagram

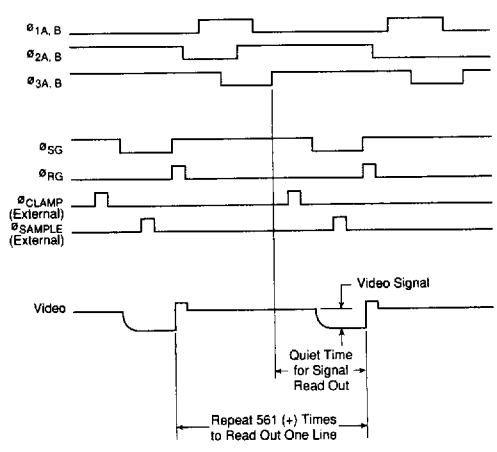

Figure 4A. Horizontal CCD Shift Register Timing Low Noise Operation

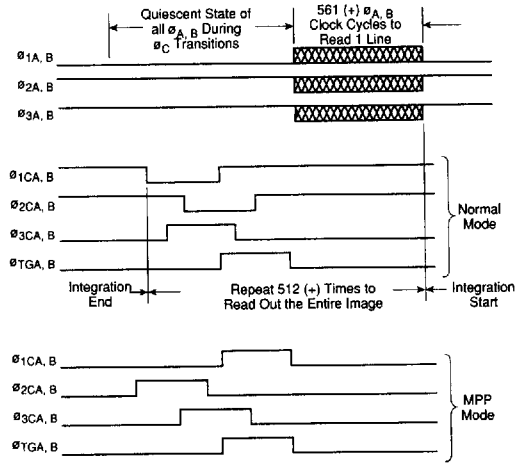

Figure 4B. Vertical CCD Shift Register Timing Diagram

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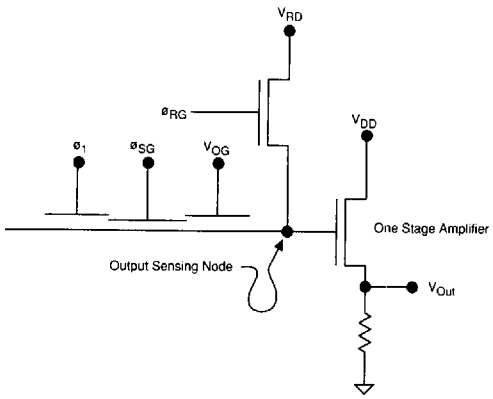

Figure 5. Output Structure

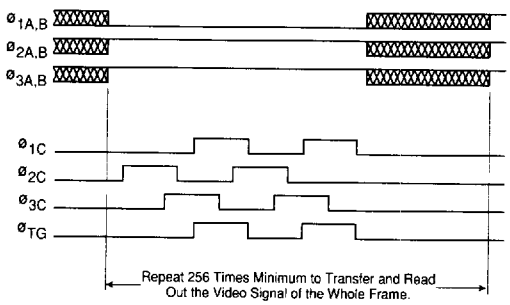

Figure 6A. Timing Comparison Between $\phi_{A,B}$ and ϕ_C

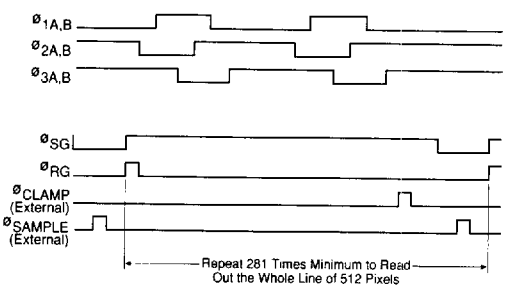

Figure 6B. Timing Comparison between $\phi_{A,B}$ and ϕ_{SG}

Array Cooling

Both the dark current and noise performance of the array can be improved by cooling. The dark current will be reduced 50% for every 7°C reduction in array temperature. The noise floor of the output amplifier is proportional to $\sqrt{kTC}$ where k is Boltzmann's constant, T is the array temperature in degrees Kelvin and C is the output node capacitance of approximately .17 pF. Cooling can be achieved via a thermo-electric, Joule-Thomson cooler, or liquid nitrogen dewar.

UV Coating

The RA0512JAU CCD is available with a special UV enhancement coating which extends the spectral response range to 120 nm. A thin layer of lumogen is deposited directly on the frontside illuminated arrays and will emit at 550 nm when excited by 120 nm - 450 nm light. The coating is transparent in the visible and near-infrared spectrums. UV coated devices are designed by the -3XX part number.

Backside Illumination - Thinning

The RA0512JAU is also available in a thinned version which greatly improves the quantum efficiency in the visible and near-infrared while also giving excellent performance in the 200 - 400 nm UV range. The imaging area of the device is thinned to 10 μ using a chemical etch procedure. Then a flash-oxide treatment is applied to the thinned area. To activate the flash oxide it is necessary to UV flood the array (expose the array to a UV light source for 5 - 10 minutes or longer, using a mercury lamp (eprom eraser)) to charge the device. Once the array is returned to room temperature, the charge will decrease requiring another charging. Thinned devices have pinouts which are mirror images of the frontside devices and are designated by the 2XX part number.

Specifications

Recommended operating conditions for the RA0512J are shown in Table 2. Typical device specifications are shown in Table 3, and Table 4 gives typical capacitance values.

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Table 1. Pin Descriptions

Pin No.	Sym	Function	Register
1	ϕ_{3C}	Parallel phase 3 clock	C
2	N/C		
3	ϕ_{TGA}	Parallel transfer gate to reg. A	A
4	VINA	Input diode	A
5	ϕ_{SA}	Input sample gate	A
6	VRECA	Input receiving gate	A
7	ϕ_{3A}	Serial phase 3 clock	A
8	ϕ_{2A}	Serial phase 2 clock	A
9	ϕ_{1A}	Serial phase 1 clock	A
10	N/C		
11	V_{OGA}	Output bias gate	A
12	ϕ_{RGA}	Reset gate	A
13	V_{RDA}	Reset drain	A
14	V_{SUB}	Substrate bias	
15	V_{OUTA}	Video amplifier output	A
16	V_{DDA}	Drain supply of amplifier	A
17	SGA	Summing well gate	A
18	ϕ_{TGA}	Parallel transfer gate to reg. A	C
19	ϕ_{2C}	Parallel phase 2 clock	C
20	ϕ_{1C}	Parallel phase 1 clock	C

Pin No.	Sym	Function	Register
21	ϕ_{3C}	Parallel phase 3 clock	C
22	N/C		
23	ϕ_{TGB}	Parallel transfer gate to reg. B	B
24	VINB	Input diode	B
25	ϕ_{SB}	Input sample gate	B
26	VRECB	Input receiving gate	B
27	ϕ_{3B}	Serial phase 3 clock	B
28	ϕ_{2B}	Serial phase 2 clock	B
29	ϕ_{1B}	Serial phase 1 clock	B
30	N/C		
31	VOGB	Output bias gate	B
32	ϕ_{RGB}	Reset gate	B
33	V_{RDB}	Reset drain	B
34	V_{SUB}	Substrate bias	
35	V_{OUTB}	Video amplifier output	B
36	V_{DDB}	Drain supply of amplifier	B
37	SGB	Summing well gate	B
38	ϕ_{TGB}	Parallel transfer gate to reg. B	C
39	ϕ_{2C}	Parallel phase 2 clock	C
40	ϕ_{1C}	Parallel phase 1 clock	C

Note: Pins 1, 19, 20 are internally connected to pins 21, 39, 40 respectively. This allows the vertical clocks to be driven from both sides of the sensor to improve clock response time.

Table 2. Recommended Operating Conditions

Definition		Symbol	Parameter						
			Normal Mode			MPP Mode			
			Low	Typ	High	Low	Typ	High	Units
DC supply		V_{DD}	20	21	25	20	21	25	V DC
Output gate bias		V_{OG}	3	6	8	1	2	5	V DC
Reset drain bias		V_{RD}	12	13	14	12	13	14	V DC
Substrate bias		V_{SUB}, V_{SS}	-5	0	0	-5	-0	0	V DC
Serial clocks	High	ϕ_A, ϕ_B		10			6		V
	Low			-2			-6		V
Vertical clocks	High	ϕ_{1C}, ϕ_{2C}, ϕ_{3C}		10			4		V
	Low			-2			-8		V
Transfer gate clock	High	ϕ_{TG}		10			4		V
	Low			-2			-8		V
Reset gate clock	High	ϕ_{RG}		10			12		V
	Low		0	5		0	6	1	V
Summing gate clock	High	ϕ_{SG}		10			6		V
	Low			-2			-6		V

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Table 3. Typical Device Specifications

Test Conditions: Temperature: 230°K (-43°C); Pixel Rate: 50 kHz; Integration time: 6 sec

Parameter	Sym	Min	Typ	Max	Units
Format			512 x 512 full frame		
Pixel size			27 x 27		µm
Imaging area			13.8 x 13.8		mm
Dynamic range [1]	DR				
Normal mode			83,333:1 (98 dB)		
MPP mode			58,333:1 (95 dB)		
Full well charge	Q_{sat}				
Normal mode			500		K electrons
MPP mode			350		K electrons
Saturation voltage [2]	V_{sat}				
Normal mode			350		mV
MPP mode			220		mV
Dark current [3,6,7]	DL				
Normal mode			1.0		na/cm^2
MPP mode			50		pa/cm^2
Saturation exposure	E_{sat}		5.7		µJ/cm^2
Responsivity	R		20		V/µJ/cm^2
Photo-response nonuniformity [4]	PRNU		5	10	±%
Dark signal nonuniformity [3]	DSNU		4		mV
Charge transfer efficiency	CTE		.99999		
Output amplifier gain			.5		µV/electron
Read noise [5]			6		electrons

Notes:

1. Full well/read noise
2. R_{Load} = 5.1K
3. Hot pixels are ignored.
4. Low pixels and traps are ignored.
5. Measured at -110°C.
6. Typical dark current for thinned version is 2 times higher than frontside illuminated device.
7. At 23°C.

Table 4. Typical Capacitance Values

Parameter	Sym	Pin No.	Typ Value	Units
Parallel clocks	$ø_{1C}$	20, 40	2100	pF
	$ø_{2C}$	19, 39	1550	pF
	$ø_{3C}$	1, 21	2150	pF
Serial clocks	$ø_{1A/B}$	9, 29	135	pF
	$ø_{2A/B}$	8, 28	90	pF
	$ø_{3A/B}$	7, 27	180	pF
Transfer clocks	$ø_{TGA/B}$	3, 18, 23, 38	71	pF
Video output	$V_{OutA/B}$	15, 35	10	pF
Reset gate clock	$ø_{RGA,B}$	12, 32	21	pF
Summing gate clock	$ø_{SGA,B}$	17, 37	9	pF

Absolute Maximum Ratings

Storage temperature: -150°C to +50°C

Voltages: measured with respect to substrate pins 14 & 34

Pin 1, 3, 7, 8, 9, 17, 18, 19, 20, 21, 23, 27, 28, 29, 37, 38, 39, 40	Max 20V swing
All other pins	0V to 25V

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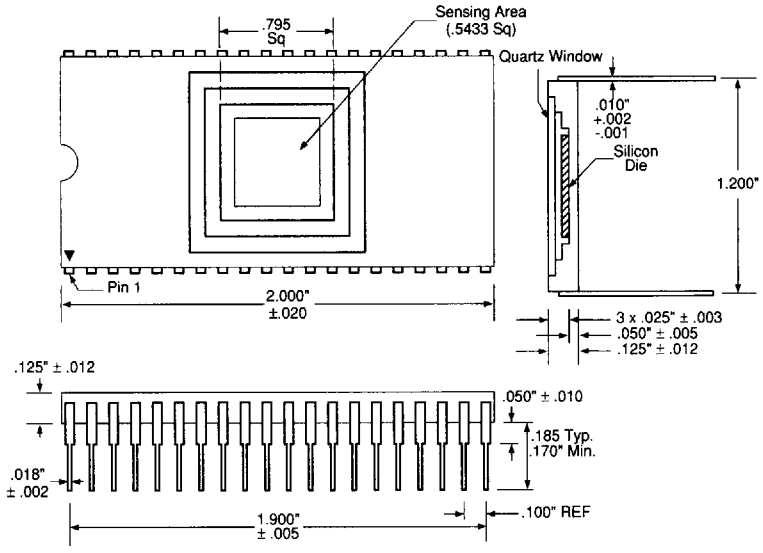

Figure 7. Package Dimensions

Ordering Information

Grade	Maximum Point Defects	Maximum Column Defects	Maximum Cluster Defects	Unsealed Part Number	Quartz Window
0	0	0	0	RA0512JAU-011	RA0512JAQ-011
1	10	0	1	RA0512JAU-020	RA0512JAQ-020
2	100	0	2	RA0512JAU-021	RA0512JAQ-021

Defect Definition

A. Point defects - Hot, low or trap
   1. Hot pixel - a pixel with an output signal 10 times greater than average dark current.
   2. Low pixel - a pixel with an output signal 50% lower than average background near full-well
   3. Charge trap - defect greater than 0.7% of full-well

B. Other
   1. Column defect - Ten or more contiguous point defects in a single column
   2. Cluster defect - Two to nine contiguous point defects

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