PT Pericom Technology Inc.

Bluetooth Digital Audio Streaming IC

Features

- Compliant to Bluetooth Specification v1.2
- Seamless interface to PT8R1002 (BlueRF™ RF transceiver)
- High speed UART, USB 1.1 interface with hub/devices and host function, up to four channels 8KHz PCM / CVSD codec, 16/18/20/24-bit I^2S audio input/output and SPDIF input/output interface, 2 channel digital AMP interface
- Integrated 128MHz PTI own hybrid RISC and DSP PiCOII embedded processor with 24-bit multiplication and 48-bit accumulation and 128KByte on-chip SRAM enough to support several digital audio and speech codecs
- On-chip implementation of BT qualified Link Controller, Link Manager, HCI, L2CAP, RFCOMM and several profiles such as Headset, SPP, OBEX, AV profiles, etc.
- Software development kit and source code licenses available for qualified embedded stacks and DSP firmware for popular digital audio and speech codecs
- Single reference clock for system, USB, audio sub system
- 0.18um CMOS technology

Application

- Bluetooth portable audio players
- Stereo audio headset with HSP/HFP function
- Multi-functions USB dongle such as Bluetooth, USB audio device, USB Flash storage, etc.
- Wireless high quality digital audio streaming system for DVD/PC speaker

General Descriptions

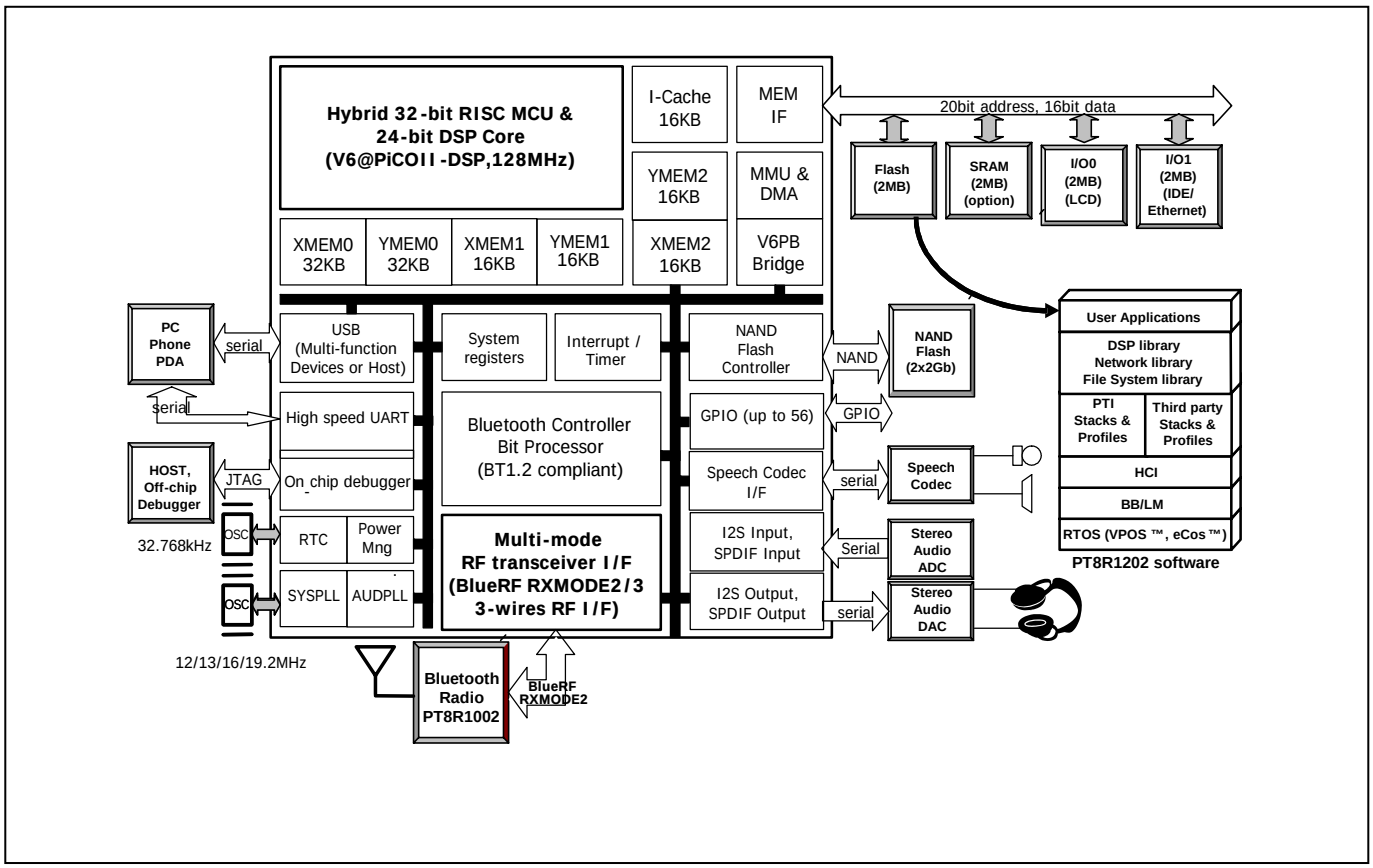
The PT8R1202 is a part of the PTI Bluetooth product family. It is a DSP processor with the functionality of both baseband controller providing the Bluetooth™ functionality for high data rate, short-distance wireless communication in the free 2.4GHz ISM band and digital audio decoder such as MP3 or AC3. Together with PT8R100X 2.4GHz radio transceiver IC and an external flash memory, it provides a fully compliant Bluetooth system for data and voice communications. PT8R1202 consists of BlueRF™ RXMODE2/3, 3-wires radio interface, Bluetooth™ baseband and bit processor, PTI proprietary 32-bit hybrid RISC/DSP embedded processor with 48bit resolution, and USB / UART / PCM / DAC / I2S / SPDIF / SMC standard interfaces.

The on-chip 32-bit hybrid RISC/DSP embedded processor is powerful enough to support full rate Bluetooth data communications as well as full rate digital audio decoding and includes large enough embedded SRAM up to 128KByte to support several applications without external memory, which results in cost-effective and low-power consumption systems. In combination with PTI own optimized Bluetooth™ baseband, embedded protocol stacks and audio decoder firmware, it provides a complete cost-effective SOC embedded solutions such as portable MP3 decoder, wireless high quality speaker system or headset.

Ordering Information

Device	Package				Order Number
	Type		Size	Shipment Method	
PT8R1202	LQFP144	Normal	20 x 20 x 1.4mm	Tray	PT8R1202F
				T&R	PT8R1202FX
		Pb(Lead) free		Tray	PT8R1202FE
				T&R	PT8R1202FEX
	fpBGA144	Normal	10 x 10 x 1.4mm	Tray	PT8R1202ND
				T&R	PT8R1202NDX
		Pb(Lead) free		Tray	PT8R1202NDE
				T&R	PT8R1202NDEX

Block Diagram



Product Description

Bluetooth is an open specification for short-range data communications. It operates in the globally available 2.4 GHz to 2.5 GHz ISM free band. Fast frequency hopping (1600 hop/s), 79 available channels (2.402 to 2.480 GHz), and a maximum 1 Mbit/s GFSK modem are allowed.

The PT8R1202 consists of a Bluetooth baseband hardware, on-chip 128MHz hybrid embedded RISC / DSP processor and peripheral interface block. The PT8R1202 focuses on audio streaming to distribute audio content of high-quality in mono or stereo on ACL channels of Bluetooth. Since PT8R1202 is highly integrated SOC solution to support the Advanced Audio Distribution Profile(A2DP) defined in Bluetooth as audio streaming application with minimum BOM, the minimum required external devices are just PT8R100X 2.4GHz radio transceiver IC, external antenna, crystal, and minimum 256KB flash memory for program code.

Bluetooth baseband hardware

Bluetooth baseband hardware consists of modem control, packet processing hardware, and on-chip microcontroller interface.

Modem control part generates the control signal for modem and RF block and transmits or receives data with modem. PT8R1202 supports BlueRF™ RXMODE2/3 Bluetooth radio interface with uni/bi-directional and JTAG/DBUS serial interface like PT8R1000 or PT8R1001 PTI Bluetooth radio transceiver. In RXMODE3, SYNCWORD correlator is located in radio transceiver, SYNCWORD detect signal feeds from external radio transceiver. In RXMODE2, SYNCWORD correlation is processed in PT8R1202, SYNCWORD detect signal feed to external radio transceiver to timing adjustment of modem. In additional to BlueRF™ interface, PT8R1202 supports BlueQ™ interface with SBI serial interface.

Packet processing for Bluetooth is implemented by a dedicated hardware for a low power solution whilst providing the required data throughput. The function implemented in hardware include : forward error correction, header error control, cyclic redundancy check, encryption, and data whitening. On-chip microcontroller interface generates interrupt signal to on-chip interrupt handler and processes DMA operation with 16KB internal memory(XMEM2) which is shared with on-chip microcontroller. During radio transmission this block constructs a packet from header information and payload data/voice taken from a ring buffer in XMEM2 which is previously loaded by software. For radio reception, this block stores the packet header and the payload data in the appropriate ring buffer in XMEM2, which is indicated by software. After the completion of reception, this block generates interrupt signal to on-chip interrupt handler. This architecture minimizes the interventions required by the processor during packet transmission and reception.

Hybrid embedded RISC / DSP processor

To satisfy multimedia data streaming through wireless connectivity like Bluetooth, the embedded processor used in portable system must provide highly energy-efficient operations, due to the importance of battery weight and size without compromising high performance when the user requires it. The functions required in this application are classified into two computations such as MCU operation and DSP operation. The former performs all functions associated with user interface as well as real-time communication protocols and the latter performs all signal-processing and multimedia functions.

The on-chip embedded processor in the PT8R1202 is based on PTI proprietary V6 processor(PiCOII-RISC/DSP), which is optimized to accelerate both two computations for low power and high performance embedded processing. Its instruction set is optimized not only for general embedded processing but also DSP signal processing specially used in audio and speech code. This hybrid embedded RISC/DSP processor supports 24-bit multiplication and 48-bit accumulator with DSP functionality such as saturation and rounding. Also, it supports SIMD features, which results in high performance in 16-bit speech applications.

To support low power consumption, on-chip processor adopts programmable dynamic clock control, reduces the complexity of embedded RTOS optimizing for both Bluetooth connectivity and audio streaming, and minimizes external I/O access with several techniques. Default operation frequency is 96MHz at boot and it can be increased to 128MHz entering into turbo mode. There are four global power states provided in PT8R1202 such as active state, sleep state, deep sleep state and power-off state. In active state, processor can change the processor clock between normal operation clock, a half of one, and a third of one. For example, if processor operates in turbo mode, it can change processor clock between 128MHz, 64MHz and 42MHz. Also, during the execution of “idle” instruction, it cuts down the processor clock without interrupting I/O device operation. In sleep state, the clock of all processor and I/O device except RTC is disabled. In sleep state, processor can be waked up quickly by RTC time-out event or external trigger signal since on-chip PLL is still working in order to fast response. Deep sleep state is the same of sleep state except on-chip PLL is off also. Since on-chip PLL is off in deep sleep state, the power consumption is reduced very much but requires more latency during wake-up.

To minimize the access of external flash memory for code, PT8R1202 includes on-chip 16KB instruction cache. In addition to instruction cache, frequent access code or time critical code is dynamically located on scratch-pad memory of internal X/YMEM region. It is possible to allocate up to 96KB as scratch-pad memory in order to reduce external memory access for low power and high performance Bluetooth digital audio streaming system.

Total 128KB internal SRAM is integrated large enough to support both on-chip Bluetooth stack and audio application without external memory, which results in cost-effective and low-power consumption systems. Internal SRAM

consists of six types memories : XMEM0, XMEM1, XMEM2, YMEM0, YMEM1, and YMEM2. All memories can be byte accessible as general purpose data memory. Some memories such as XMEM2 and YMEM2 have special usage. XMEM2 is used as 16KB memory for communication with Bluetooth baseband hardware or USB, and YMEM2 is used as 16KB memory for communication with audio data buffer for stereo PCM output.

PT8R1202 can boot from NOR type flash and NAND type flash memory. With NOR type flash memory, code can be cached into internal instruction cache in order to execute code at high frequency and reduce power consumption of frequent memory fetch. With NAND type flash memory, both code and data are stored same memory, which results in the reduction of system BOM and form factor. If PT8R1202 boots from NAND flash, the configuration of the internal instruction cache is optimized to support NAND flash efficiently.

Software development environment

The PT8R1202 supports high-level programming development with our optimized C compiler based on GCC and intrinsic library functions to maximize the software development productivity. The system software to support application software development includes C-compiler, multi-level instruction set simulator, performance analyzing profiler, memory configuration optimizer and power monitor. Specially, our C compiler supports automatically collaboration mechanism between compiled general code and hand-written DSP libraries to maximize the utilization of V6 advanced features.

To reduce the system developing cost, PTI provides performance optimized DSP library for enabling several multimedia standards with our own developing skill for multimedia application. This library supports several standards such as MPEG-1/2 layer I, II, III audio decompression, Dolby Digital decompression, WMA, SBC codec, G.723.1/G.728 speech codec, etc.

Advanced audio streaming on Bluetooth

PT8R1202 supports advanced audio streaming using the advanced audio distribution profile(A2DP) defined in Bluetooth. This profile is used by devices to distribute audio content of high-quality in mono or stereo on ACL channels, as well as Bluetooth audio which indicates distribution of narrow band voice on SCO channel. PT8R1202 support several codecs in A2DP such as low complexity subband codec(SBC), MPEG-1,2 audio, or WMA. This advanced audio streaming feature of PT8R1202 can be used several audio system with Bluetooth connectivity between portable audio player and headphone, high-quality audio system and surround speaker, or portable speech recorder and microphone.

For supporting A2DP, PT8R1202 embeds all Bluetooth stack such as baseband, LMP, L2CAP, SDP, AVDTP(A/V Distribution Transport Protocol) and AVCTP(A/V Control Transport Protocol). As well as A2DP, PT8R1202 supports cordless phone or dial-up networking using RFCOMM, TCS/BIN protocol and profiles.

Peripheral Interface block

PT8R1202 has several peripheral interface such as off-chip memory interface, USB interface, UART interface, PCM interface, I2S and SPDIF interface, JTAG interface, Flash Memory/Card interface, and up-to 59-general purpose programmable I/O(GPIO) interface. All peripheral devices are connected to on-chip microcontroller via internal peripheral bus(V6PB), which is compatible with Advanced Peripheral Bus(APB) from ARM™

Off-chip memory interface supports 4 devices concurrently such as flash memory, SRAM, and I/O for code and data. It supports 2MB address space and 16bit data with byte access functionality. The access timing for each device can be programmable by software. Also, PT8R1202 supports external I/O with explicit wait signal such as PCMCIA card.

USB interface supports both 12Mbps and 1.5Mbps serial data communication conforming to universal serial bus standard version 1.1. It supports both device and host side operation and all operation modes such as bulk, interrupt, control and isochronous mode. It consists of one control end-point, four receiver end-points and four transmit end-points, each of which has dual 64bytes FIFO except control end-point and supports bulk, interrupt, and control, and two pair of end-points which supports isochronous mode up to 1023bytes.

On-chip UART supports programmable baud rate up to maximum 1.84MBaud serial communication and fully programmable serial interface such as flow control and bit format. It includes separate 16-byte transmit and receiver FIFOs to reduce CPU interrupts.

PCM interface supports the external PCM codec with CVSD Bluetooth codec functionality. For the external PCM codec, it support 8-bit A/u-law PCM and 13- or 14-bit 8KHz linear PCM in both master or slave mode. For 8-bit A/u-law format, it supports one, two and four channels simultaneously.

Audio output interface supports I2S digital audio interface, SPDIF digital audio interface. For external DAC, it supports 32, 44.1, or 48KHz sampling frequencies with the programmable bit resolution up to 24bit. All sampling frequency can be generated both from on-chip audio PLL or external clock source.

Audio input interface supports both I2S interface and SPDIF interface with 32, 44.1, or 48kHz sampling frequencies. For slave mode in which all control signals come from external, I2S interface can support up to 192kHz sampling frequency.

PT8R1202 supports the dedicated hardware interface to SmartMedia™ flash memory(NAND type) or card. Without the occupation of the CPU resource, it supports DMA transfer for SmartMedia™ interface to achieve fast read/write operation. At SMC boot mode, PT8R1202 can boot from SMC without normal parallel flash of NOR type.

PT8R1202 provides 59-bit programmable, bi-directional IO(GPIO) which are shared with dedicated pins in order to reduce pins. GPIO signal can be used as key-pad input, MMC/SDCard/Memory Stick™ interface, or LCD interface.

PT8R1202 supports standard JTAG interface for both boundary scan and communication channel with PTI enhanced on-chip hardware debugger controller. Using on-chip debugger controller, off-chip debug handler or external host can access internal peripheral device registers, external memory interface, and executes real-timing hardware debugging and monitoring of on-chip embedded RISC processor. Also, external host can communicate on-chip processor through JTAG with on-chip hardware managed channel buffer.

Pin Descriptions

Pin Name	PIN	I/O	TYPE	Description
DI(Digital Input, 3.3V), DO(Digital Output, 3.3V), DB(Digital Bidirectional, 3.3V), DP(Digital Programmable, 3.3V) DCP(Digital Core Power, 1.8V), DPP(Digital Peripheral Power, 3.3V) DCG(Digital Core Ground), DPG(Digital Peripheral Ground) AAI(Analog Audio Input, 3.3V), AAO(Analog Audio Output, 3.3V), AAB(Analog Audio Bidirectional, 3.3V) ACI(Analog Core Input, 1.8V), ACO(Analog Core Output, 1.8V), ACB(Analog Core Bidirectional, 1.8V) AAP(Analog Audio Power, 3.3V), AAG(Analog Audio Ground) ACP(Analog Core Power, 1.8V), ACG(Analog Core Ground)				
BLUETOOTH INTERFACE : 12				
TXACTIVE / GPA[0]	D4	DO/ DP	active high	transmitter enable
RXACTIVE / GPA[1]	C1	DO / DP	active high	receiver enable
TXDATA_EN / GPA[2]	E2	DO / DP	active high	timing reference of valid data
TXDATA / GPA[3]	D1	DB / DP	serial data	transmit data
RXDATA / GPA[4]	E3	DI / DP	serial data	receive data
SYNCDECTECT / GPA[5]	E1	DB / DP	active high	indication of SYNC word detection
DATACLK / GPA[6]	F1	DI / DP	clock	Phy reference data clock
RFRESET / GPA[7]	F3	DO / DP	active high	Reset signal for external radio transceiver
BLUERF_TCK / GPA[8]	F2	DO / DP	clock	a serial register interface clock
BLUERF_TMS / GPA[9]	G3	DO / DP	serial data	control signal of Phy's TAP controller
BLUERF_TDI / GPA[10]	G1	DB / DP	serial data	Phy control register serial data output
BLUERF_TDO / GPA[11]	G2	DI / DP	serial data	Phy control register serial data input
CLOCK SIGNAL INTERFACE : 6				
XTALIN	J8	DI	clock	Crystal input for on-chip PLL (see note1)
XTALOUT	L9	DO	clock	Crystal output
PLL_MD1	M10	DI	control	PLL mode control (see note1) External, test clock input (see note1, 2)
PLL_MD0	M11	DI / DO	control	PLL mode control (see note1) Manufacturing test mode (see note2)
PLLSEL	L10	DI	control pin	External clock source select signal (see note1,2)
CLKOUT / GPB[0]	L7	DO / DP	clock	clock out divided by a third of internal system clock (see note1)
TEST & DEBUG INTERFACE : 9				
RESET	K8	DI	active low	reset signal
BTMD[1:0]	M7, J7	DI / DP	control pin	boot mode (see note2)
SCAN_EN	C5	DI	control pin	manufacturing test (see note3)
JTAG_TCK / GPC[4]	M8	DI / DP	clock	JTAG clock signal
JTAG_TMS / GPC[5]	K7	DI / DP	serial data	JTAG test mode signal
JTAG_RST / GPC[6]	L8	DI / DP	active low	JTAG reset signal
JTAG_TDI / GPC[7]	K9	DI / DP	serial data	JTAG serial input data
JTAG_TDO / GPC[8]	M9	DO / DP	serial data	JTAG serial output data
EXTERNAL MEMORY INTERFACE : 45				
MEMA[19:0]	(see note4)	DO	bus	address bus for external memory
MEMD[15:0]	(see note5)	DB	bus	data bus for external memory
WEB	C10	DO	active low	write enable signal for external memory
REB	C12	DO	active low	read enable signal for external memory
UBE / GPB[1]	D11	DO / DP	active low	upper byte enable (see note6)
LBE / GPB[2]	D10	DO / DP	active low	lower byte enable (see note6)
FLASHCSB / GPB[3]	D12	DO	active low	chip select for external flash memory
SRAMCSB / GPB[4]	E10	DO / DP	active low	chip select for external SRAM memory
IOCSB0 / GPB[5]	E11	DO / DP	active low	chip select for external I/O device0
IOCSB1 / SM_CSB1 / GPB[6]	E12	DO / DP	active low	chip select for external I/O device1 (see note7)
IOWAIT / GPB[7]	F10	DI / DP	control pin	IO wait cycle extension indication signal
UART & USB INTERFACE : 6				
UARTTX / GPC[0]	H3	DO / DP	serial data	UART serial transmit data / USBOE
UARTRX / GPC[1]	H1	DI / DP	serial data	UART serial receive data / USBSPEED
DIGAMP_L / UARTRTS / AUDISCLK / GPC[2]	H2	DO / DP	active low	UART RTS(Ready To Send) signal / USBVPO AUDISCLK / DIGAMP_L (see note8)
DIGAMP_R / UARTCTS / AUDILRCLK / GPC[3]	J4	DO / DP	active low	UART CTS(Clear To Send) signal / USBVMO AUDILRCLK / DIGAMP_R(see note8)
D+	B4	DB	serial data	USB D+
D-	A4	DB	serial data	USB D-

Pin Name	PIN	I/O	TYPE	Description
DIGITAL AUDIO INTERFACE : 9				
PCMOUT / GPD[0]	J3	DO / DP	serial data	PCM 8kbps data out
PCMIN / GPD[1]	J1	DI / DP	serial data	PCM 8kbps data input
PCMSYNC / GPD[2]	J2	DP	clock	PCM 8KHz frame synchronization signal
PCMCLK / GPD[3]	K1	DP	clock	PCM bit data clock (128/256)
AUDSCLK / GPD[4]	K2	DP	clock	audio serial data bit clock(64*fs)
AUDLRCLK / GPD[5]	L1	DP	clock/	audio left/right sync clock(fs)
AUDOUT / GPD[6]	L2	DO / DP	serial data	audio serial data output
AUDMCLK / GPD[7]	M1	DP	clock	audio oversampled clock(256/384*fs)
AUDIN / SPDIFIN/GPD[8]	K3	DI / DP	serial data	audio serial data input
ANALOG AUDIO INTERFACE : 6 (see note9)				
MIC_IN	B2	AAI	analog	Reserved
MICGS	A1	AAO	analog	Reserved
VMID	C3	AAO	analog	Reserved
VREF	C2	AAO	analog	Reserved
EARA	C4	AAO	analog	Sleep crystal(32.768kHz) XTALIN
EARB	B1	AAO	analog	Sleep crystal(32.768kHz) XTALOUT
SMARTMEDIA INTERFACE : 14				
SM_CSB / GPE[0]	L3	DO / DP	active low	Smartmedia chip select
SM_CLE / GPE[1]	M2	DO / DP	active low	Smartmedia command latch enable
SM_ALE / GPE[2]	M3	DO / DP	active low	Smartmedia address latch enable
SM_WE / GPE[3]	K4	DO / DP	active low	Smartmedia write enable
SM_OE / GPE[4]	M4	DO / DP	active low	Smartmedia read enable
SM_RB / GPE[5]	L4	DI / DP	control pin	Smartmedia ready signal
SM_DATA[7:0] /GPF[7:0]	(see note10)	DB	bus	Smartmedia data/address bus
GPIO INTERFACE : 7				
GPG[0] / IRQ0 / SSM1	D6	DI / DP	active high	external interrupt request0 (see note11)
GPG[1] / IRQ1	B6	DI / DP	active high	external interrupt request1 / USBVPI
GPG[2] / WAKEUP	C6	DI / DP	active high	external wake up signal (see note12) / USBRCV
GPG[3] / SSM0	A5	DO / DP	clock	Size indicator at Smartmedia boot (see note11) / USBVMI
GPG[4] / CLK32K	D5	DB / DP	signal	External RTC clock(32kHz) input (see note13)
SPDIFO / GPG[5]	B5	DO / DP	signal	SPDIF output / USBSUSPND (see note14)
POWER SUPPLIES : 31				
SPLL_VCC(1)	L11	ACP	power	supply for system PLL (1.8V)
SPLL_GND(1)	M12	ACG	ground	ground for system PLL
APLL_VCC(1)	D3	ACP	power	supply for audio PLL (1.8V)
APLL_GND(1)	D2	ACG	ground	ground for audio PLL
ACODEC_VCC(1)	A2	AAP	power	supply for combo audio codec (3.0V)
ACODEC_GND(2)	A3, B3	AAG	ground	ground for combo audio codec
VCC(6)	(see note15)	DCP	power	power for digital core block (1.8V)
VCC_GND(6)	(see note16)	DCG	ground	ground for digital core block
VPP(6)	(see note17)	DPP	power	supply for digital peripheral blocks (3.3V)
VPP_GND(6)	(see note18)	DPG	ground	ground for digital peripheral blocks

Note :

1. PT8R1202 use two main clocks for core operation and peripheral operation. Both clocks can be generated from on-chip PLL or individually pumped from external clock source. The clock for processor operation, named CLKSYS, can be variable by application requirement or dynamic power management, but the clock for peripheral operation must be fixed as 48MHz for USB and audio interface and 32MHz for others. The PLL in the PT8R1202 supports 12MHz, 13MHz, 16MHz, or 19.2MHz as reference clock. Following table shows the configuration of PT8R1202 clock generation block. For using internal clock from on-chip PLL, PLLSEL must be set “0”. When using internal clock from on-chip PLL, PT8R1202 can change the operating frequency of on-chip processor up to 128MHz turbo mode. The default operation mode is normal execution at 96MHz operating frequency and it can be changed into turbo mode by software. However, in the case of using external clock source, it does not support turbo mode.

Table 1. PLL mode set value for setting core frequency

XTALIN	PLL_MD1	PLL_MD0	PLLSEL	CLKOUT	CLKSYS	Comment
12MHz	Low	Low	Low	32MHz	96MHz	Normal mode
				42.7MHz	128MHz	Turbo mode
13MHz	Low	High	Low	32MHz	96MHz	Normal mode
				42.7MHz	128MHz	Turbo mode
16MHz	High	Low	Low	32MHz	96MHz	Normal mode
				42.7MHz	128MHz	Turbo mode
19.2MHz	High	High	Low	32MHz	96MHz	Normal mode
				42.7MHz	128MHz	Turbo mode
Don't use	96MHz	Low	High	32MHz	96MHz	Normal mode
Don't use	TESTCLK	High	High	TESTCLK	TESTCLK	TEST mode

2. If both PLL_MD0 and PLLSEL are high, the operation mode of PT8R1202 changes into TEST mode. This mode is used only for manufacturing test purpose. In TEST mode, the boot mode will be used as indication of specific test mode. In normal mode, the boot mode indicates the source of boot code to be fetched first PC.

Table 2. Boot mode set value for indicating the source of boot code fetch in normal mode

BTMD[1:0]	Name	Comment
0	Flash	Boot from external memory using FLASHCSB[0] signal
1	Debug	Wait for debug command through JTAG
2	reserved	
3	NandFlash	Bood from NandFlash using smart media interface The size of NandFlash is indicated by SSM pin. See note7 for more information.

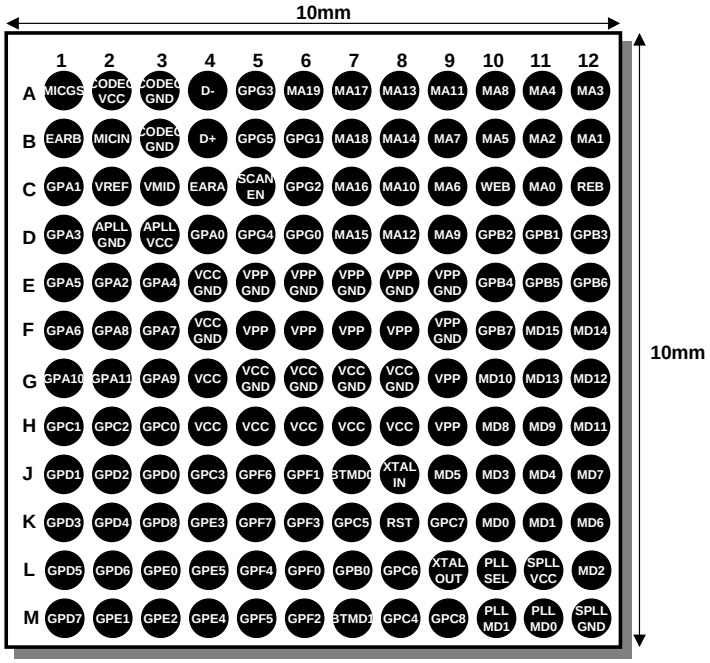
Table 3. Boot mode set value for indicating the source of boot code fetch in test mode

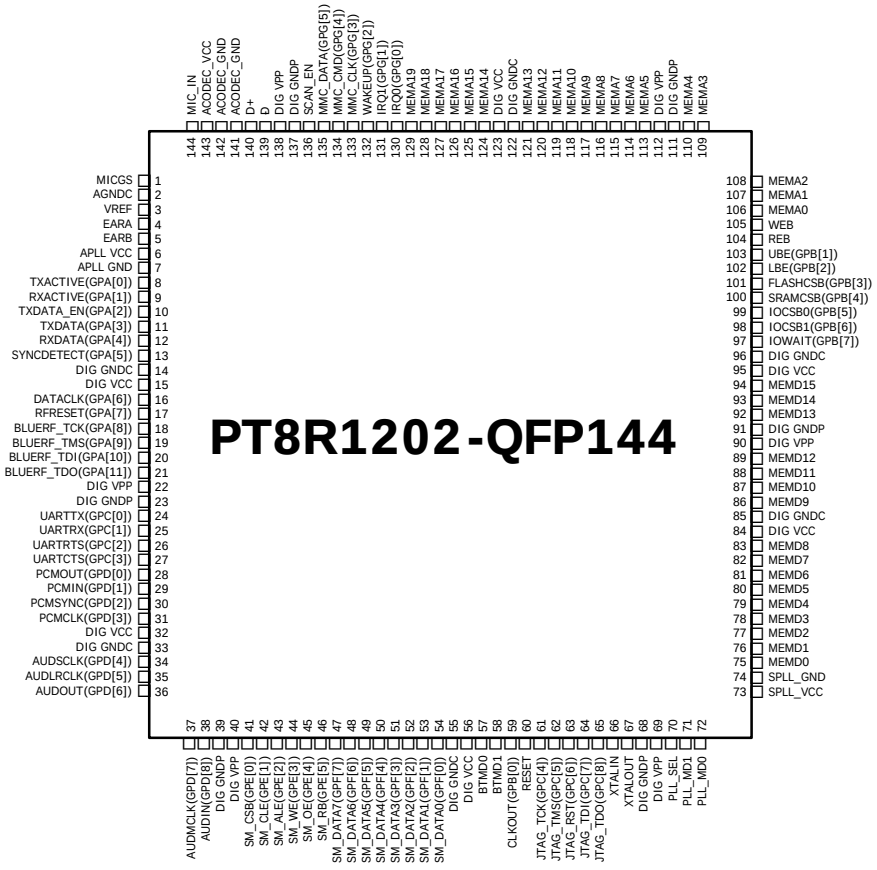
BTMD[1:0]	Name	Comment
0	SCAN test	Full scan test mode (manufacturing test purpose)
1	Codec test	Analog audio external test mode (debugging purpose)
2	Codec0 test	Audio left DAC and ADC test mode (manufacturing test purpose)
3	Codec1 test	Audio right DAC and ADC test mode (manufacturing test purpose)

3. This pin should be low for normal operation. It is used only in manufacturing test.
4. PIN of MEMA[19:0] : A6, B7, A7, C7, D7, B8, A8, D8, A9, C8, D9, A10, B9, C9, B10, A11, A12, B11, B12, C11
5. PIN of MEMD[15:0] : F11, F12, G11, G12, H12, G10, H11, H10, J12, K12, J9, J11, J10, L12, K11, K10
6. In non byte access device such as flash memory(x16), these pin will be not connected.
7. This pin can be programmed to access the second NAND flash chip in addition to SM_CSB signal. With this pin, PT8R1202 can support up to 4 Gb(512MB) NAND flash directly.
8. These pins can be used as multiple purposes by programming such as digital AMP output, UART flow control signal and alternative I2S input. From R2.4, the default direction and signal usage is changed. The default configuration is the output of internal digital amplifier. For the case of alternative I2S input mode, the sampling frequency of I2S input can be different to that of I2S output.
9. Internal audio codec is not recommended to use for both voice and audio. Instead of internal stereo sigma-delta DAC, we recommend to use external voice and audio codec. From R2.6, EARA and EARB PAD are only dedicated to oscillator PAD for external sleep crystal.
10. PIN of SM_DATA[7:0] : K5, J5, M5, L5, K6, M6, J6, L6
11. These pins is only used at NandFlash boot mode. If BTMD is "11" which means on-chip processor boots from NandFlash, these pins are used as size indication of external NandFlash. After the completion of boot, it is used as GPIO. Otherwise, it is always used as GPIO.
12. This signal can be programmed for embedded processor to be waked up from sleep or deep sleep power state.
13. Instead of dividing clock from XTALIN, this pin can be used as the low oscillator clock source as programming for extremely low power consumption in stand-by state.
14. From R2.4, the default direction of this pin is output as SPDIF output signal.
15. PIN of VCC : G4, H4, H5, H6, H7, H8
16. PIN of VPP : F5, F6, F7, F8, G9, H9
17. PIN of VCC_GND : E4, F4, G5, G6, G7, G8
18. PIN of VPP_GND : E5, E6, E7, E8, E9, F9

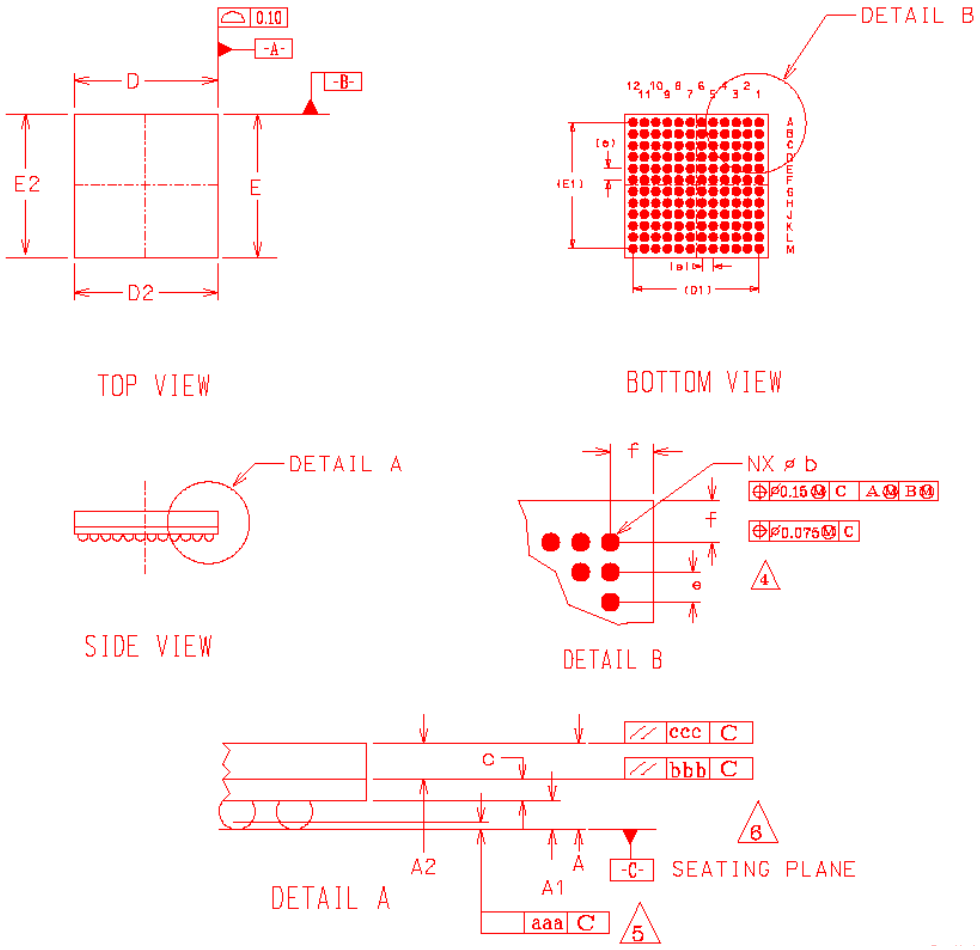
Package Diagram

The circuits is packaged with 144pin **FPBGA** and **LQFP** package. The body size of FPBGA is 10x10mm and the body size of LQFP is 20x20mm. Following figure shows the top view of the package.





Package Diagram of FPBGA

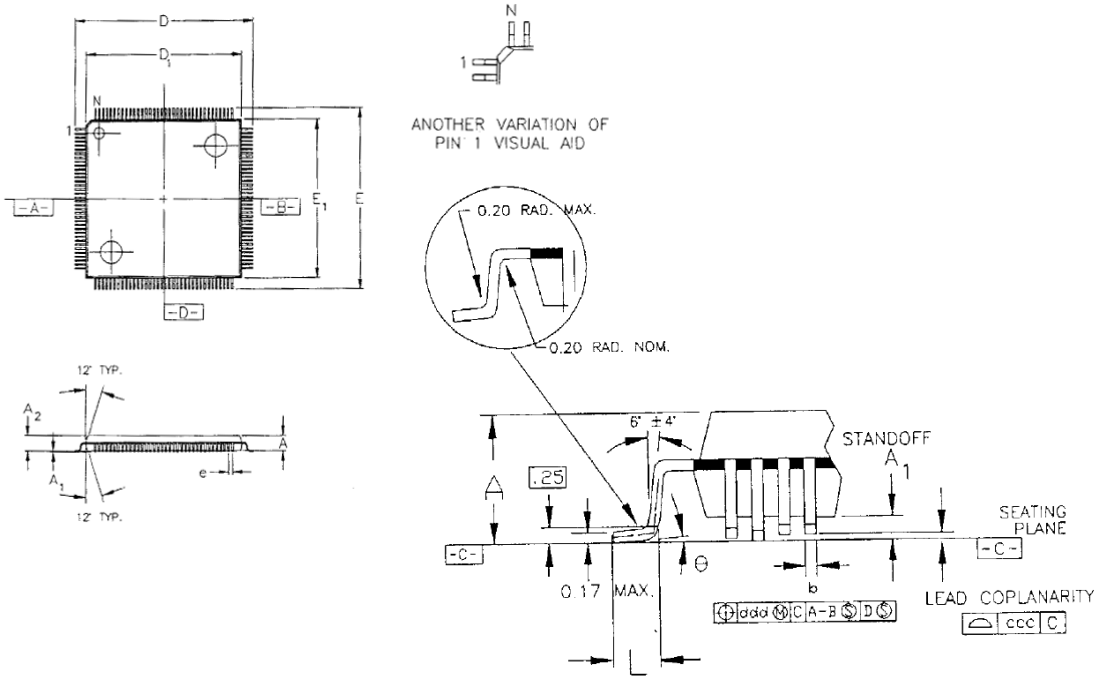


Notes :

1. All dimension are in millimeters.
2. 'e' represents the basic solder ball grid pitch.
3. 'M' represents the basic solder ball matrix size.
   And, symbol 'N' is the number of balls after depopulating.
4. 'b' is measurable at the maximum solder ball diameter after reflow parallel to primary datum -c-.
5. Dimension 'aaa' is measured parallel to primary datum –c-.
6. Primary datum –c- and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be matte finish charmilles 24 to 27.
8. Package centering to substrate shall be 0.0760 mm maximum for both X and Y direction respectively.
9. Package warp shall be 0.050mm maximum.
10. Substrate material base is bt resin.
11. The overall package thickness "A" already considers collapse balls.
12. Dimension and tolerancing per ASME Y14.5-1994.

DIMENSIONAL REFERENCES			
REF.	MIN.	NOR.	MAX.
A	1.25	1.40	1.55
A1	0.35	0.40	0.45
A2	0.65	0.70	0.75
D	9.80	10.00	10.20
D1		8.80 BSC.	
D2	9.80	10.00	10.20
E	9.80	10.00	10.20
E1		8.80 BSC	
E2	9.80	10.00	10.20
b	0.49	0.54	0.59
c	0.25	0.30	0.35
aaa			0.12
bbb			0.10
ccc			0.10
e		0.80 BSC	
f	0.50	0.60	0.70
M		12	
N		144	

Package Diagram for TQFP



Notes :

1. All dimension are in millimeters.
2. Dimention shown are nominal with TOL. As indicated.
3. L/F : EFTEC 64T copper or equivalent 0.127mm (.005") thick
4. Foot length "L" is measured at gage plane. At 0.25mm, above the seating plane.

BODY + 2.00 mm FOOTPRINT				
DIMS.	TOLS. \ LEADS	112L	144L	176L
A	MAX.	1.60		
A_1		.05 MIN./.15 MAX.		
A_2	±.05	1.40		
D	±.20	22.00		
D_1	±.10	20.00		
E	±.20	22.00		
E_1	±.10	20.00		
L	+.15/−.10	.60		
e	BASIC	.65	.50	.40
b	±.05	.30	.22	.18
θ		0°−5°		
ddd	MAX.	.13	.08	.07
ccc	MAX.	.10	.08	

I/O Description

Off-chip memory interface

The external memory port comprises a 16bit data bus(MEMD[15:0]) and an 20bit address bus(MEMA[19:0]), thus addressing up to 2Mbytes of off-chip code or data. Control signal WEB, REB, and multiple CSB(FLAHSCSB, SRAMCSB, IOCSB0 and IOCSB1) are provided, which make it possible to use a variety of different memories, including flash memory, SRAM and ROM. For SRAM access, UBE and LBE signal support byte access and memory interface block automatically handles control signals for 32bit word, 16bit half-word and 8bit byte access of on-chip microcontroller memory operations. In standard Bluetooth application, only external 256KB flash memory is required in PT8R1202. For additional Bluetooth application including several Bluetooth protocol stack which requires more data memory than internal SRAM of PT8R1202, external SRAM is used for extended data memory of PT8R1202 on-chip microcontroller. The access time of each device can be programmed and the wait cycle ranges 0 to 63 based on system clock, which is normally processor clock, that is CLKSYS. External flash can be programmed via host interface by external host or self update by PT8R1202 on-chip RISC/DSP processor.

Because PT8R1202 on-chip RISC/DSP processor is based on harvard architecture, the address map of instruction and data access is difference. Following table 1. shows the instruction address map and table 2. shows the data address map.

Table 4. Instruction address map

Address(24bit)*	Device	Attribute	Description
0x000000~0x1FFFFF	FLASH	read only	cacheable, scratch-pad memory or non-cacheable
0x200000~0x3FFFFF	-	-	reserved
0x400000~0x5FFFFF	SRAM	read only	cacheable, scratch-pad memory or non-cacheable
0x600000~0x7FFFFF	IO0	read only	cacheable, scratch-pad memory or non-cacheable
0x800000~0x9FFFFF	IO1	read only	cacheable, scratch-pad memory or non-cacheable

* This address space is based on byte addressing. There are addition extended two bits in the most significant bits(25th and 24th), and they are used for the indication of section attribute. All instructions are checked whether they are cached in the scratch-pad memory first. Then, those two bits are used to check the source of that instruction fetch. “00” indicates those section can be loaded only through on-chip instruction cache with conventional two-way set associate policy. “01” indicates those section can be loaded only set0 region of on-chip instruction cache. “10” indicates those section can be loaded only set1 region of on-chip instruction cache. “11” indicates those section can be loaded directly from external memory without passing instruction cache. The address space of this internal scratch-pad memory is 0xA00000~0xA0BFFF for XMEM and 0xC00000~0xC0BFFF for YMEM. The scratch memory is divided into four pages each size of which is 32KB with 9-bit instruction tag which consists of 3-bit section attribute and the most significant 6-bit section address. On-chip RISC processor will check the match by full associative comparison with four tag registers of internal scratch-pad memory first. Then, if that tag comparison is matched, instruction will be fetched from internal scratch-pad memory. Otherwise, instruction will be fetch through on-chip instruction cache from external flash memory region.

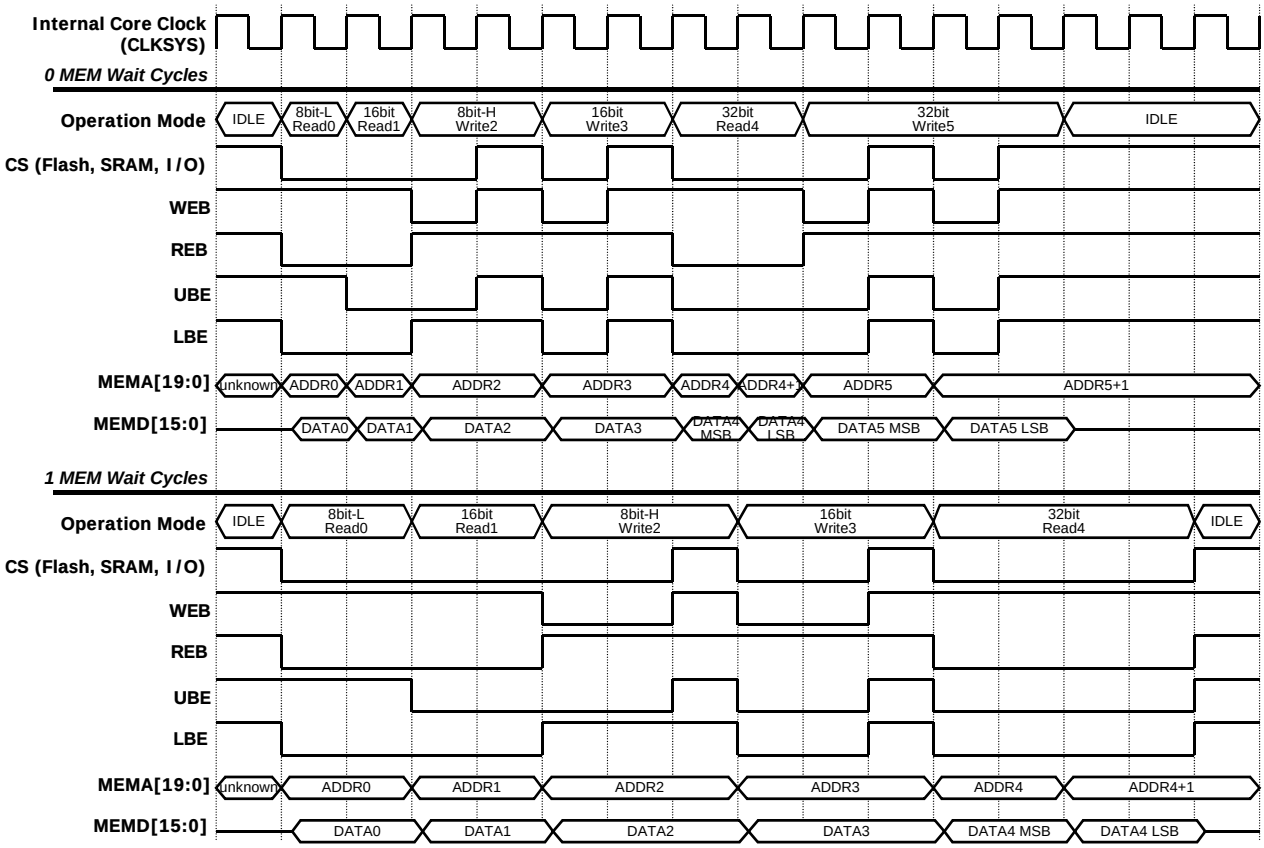
Table 5. Data address map

Address(23bit)*	Device	Attribute	Description
0x000000~0x1FFFFF	FLASH	read/write half-word, word	● instruction code memory ● constant data memory ● accessible by on-chip DMA
0x200000~0x3FFFFF	-	-	reserved
0x400000~0x5FFFFF	SRAM	read/write byte, half-word, word	● data memory ● fast fetch instruction code memory ● accessible by on-chip DMA
0x600000~0x7FFFFF	IO0	read/write byte, half-word, word	● I/O access ● accessible by on-chip DMA
0x800000~0x9FFFFF	IO1	read/write byte, half-word, word	● I/O access ● accessible by on-chip DMA
0xA00000~0xA07FFF	XMEM0 (32KB)	read/write byte, half-word, word DSP memory (14M)	● data memory ● scratch-pad instruction memory ● SmartMedia™ FIFO ● accessible by DMA
0xA08000~0xA0BFFF	XMEM1 (16KB)	read/wrtie byte, half-word, word DSP memory (14M)	● data memory ● scratch-pad instruction memory ● SmartMedia™ FIFO ● accessible by on-chip DMA
0xA0C000~0xA0FFFF	XMEM2 (16KB)	read/write byte, half-word, word	● data memory ● Bluetooth baseband FIFO, ● USB FIFO(0x20C000~0x20FFFF) ● accessible by on-chip DMA
0xC00000~0xC07FFF	YMEM0 (32KB)	read/write byte, half-word, word	● data memory ● scratch-pad instruction memory

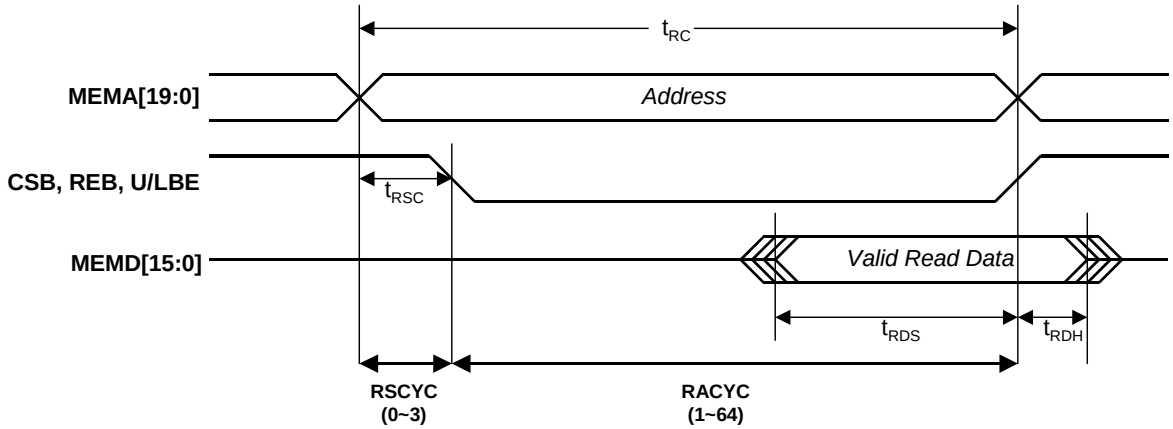
		DSP memory (14M)	● SmartMedia™ FIFO ● accessible by on-chip DMA
0xC08000~0xC0BFFF	YMEM1 (16KB)	read/write byte, half-word, word DSP memory (14M)	● data memory ● scatch-pad instruction memory ● SmartMedia™ FIFO ● accessible by on-chip DMA
0xC0C000~0xC0FFFF	YMEM2 (16KB)	read/write byte, half-word, word DSP memory(14M)	● data memory ● digital stereo audio output FIFO ● accessible by on-chip DMA

* This address space is based on byte addressing.

Off-chip memory interface waveform diagram



Off-chip memory interface read access timing without wait signal



Off-chip memory interface read access timing with wait signal

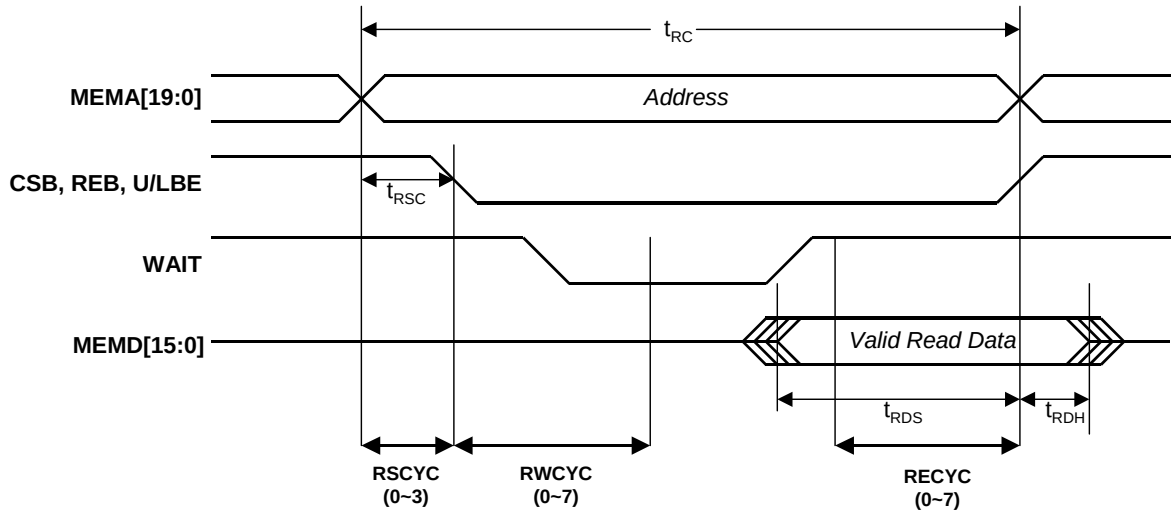
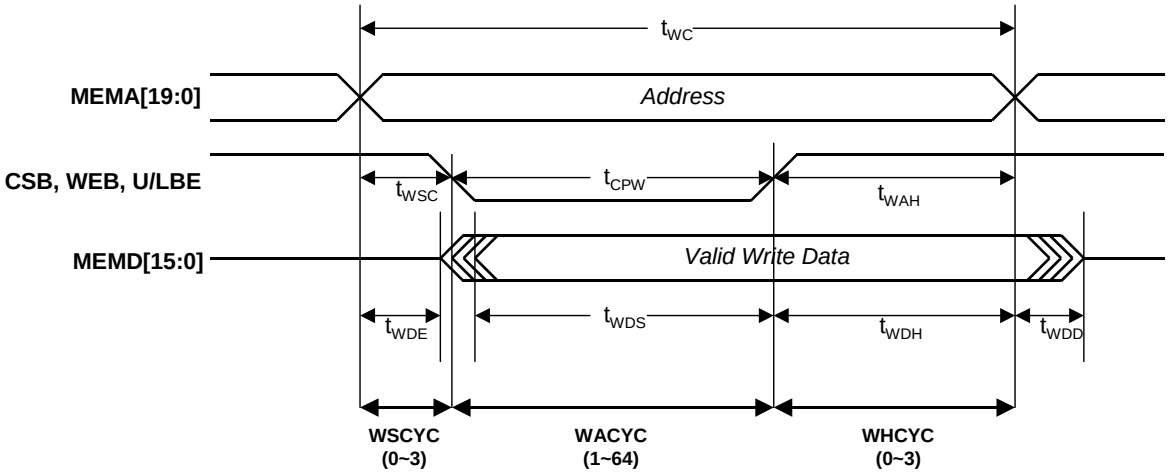


Table 6. Read access timing

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	1 (7.8ns)	64 (500ns)	CLKSYS clock cycles (128MHz)
Read data setup time	t_{RDS}	3		ns
Read data hold time	t_{RDH}	1		ns

* RSCYC, RACYC, RWCYC, RECYC based on cycle number of CLKSYS

Off-chip memory interface write access timing without wait signal



Off-chip memory interface write access timing with wait signal

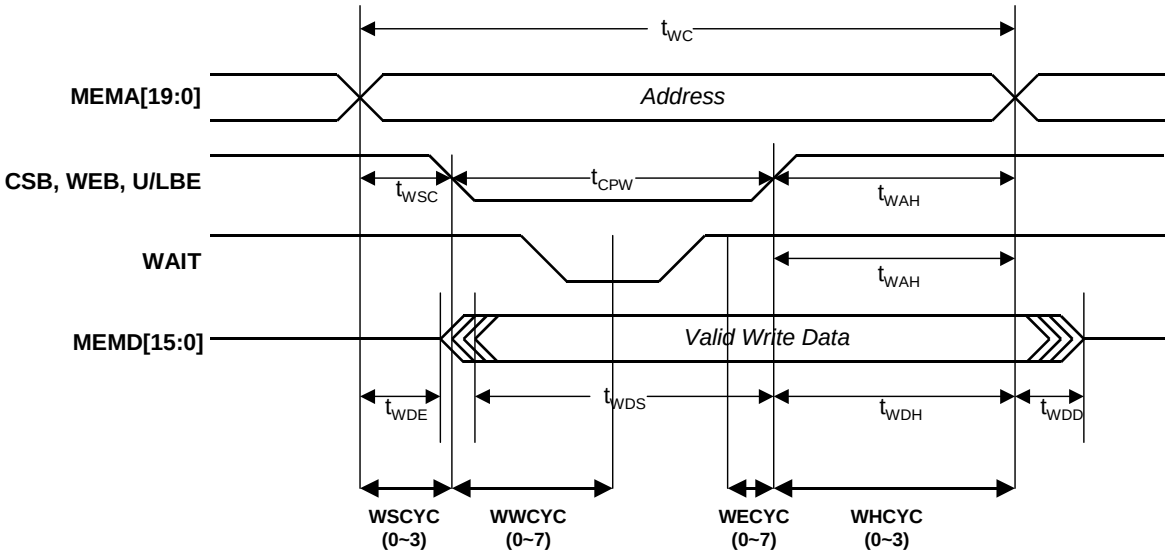
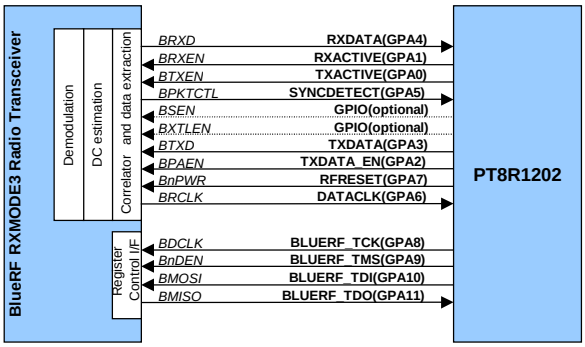


Table 7. Write access timing

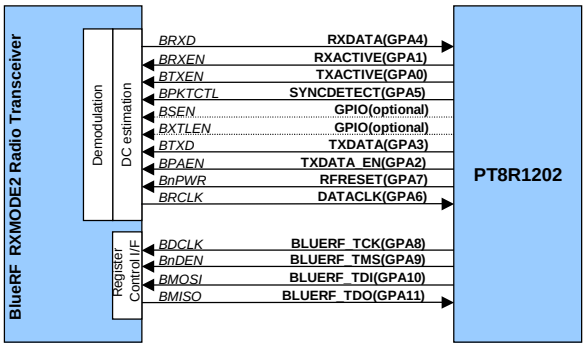
Parameter	Symbol	Min	Max	Unit
Write cycle time	t_{WC}	2 (15.6ns)	65 (507.8ns)	CLKSYS clock cycles (128MHz)
Write control signal pulse width	t_{CPW}	1 (7.8ns)	64 (500ns)	CLKSYS clock cycles (128MHz)
Write address hold time from control signal	t_{WAH}	1 (7.8ns)	1 (7.8ns)	CLKSYS clock cycles (128MHz)
Write data output enable time	t_{WDE}	0		ns
Write data setup time to control signal	t_{WDS}	4		ns (CLKSYS=128MHz)
Write data hold time from control signal	t_{WDH}	1 (7.8ns)	1 (7.8ns)	CLKSYS clock cycles (128MHz)
Write data output disable time	t_{WDD}	0		ns

Bluetooth radio interface

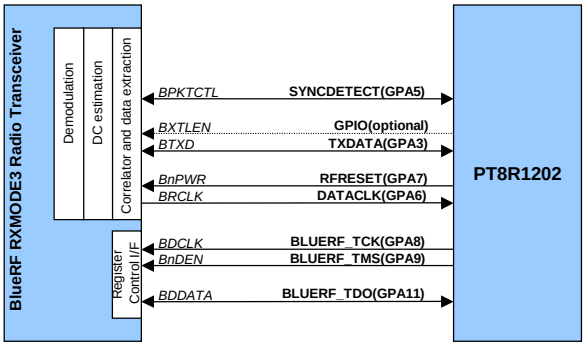
PT8R1202 supports BlueRF™ RXMODE2/3 Bluetooth radio interface with uni/bi-directional and JTAG/DBUS serial interface .PTI Bluetooth radio transceiver. In RXMODE3, SYNCWORD correlator is located in radio transceiver, SYNCWORD detect signal feeds from external radio transceiver. In RXMODE2, SYNCWORD correlation is processed in PT8R1202, SYNCWORD detect signal feed to external radio transceiver to timing adjustment of modem. In additional to BlueRF™ interface, PT8R1202 supports BlueQ™ interface with SBI serial interface.



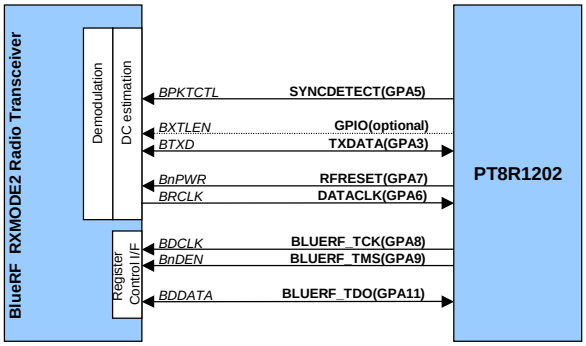
BlueRF RXMODE3 – Uni-directional I/F



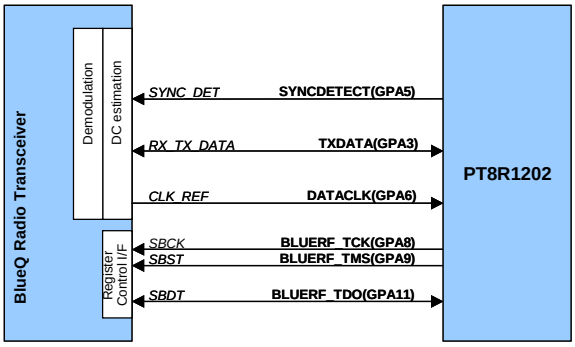
BlueRF RXMODE2 – Uni-directional I/F



BlueRF RXMODE3 – Bi-directional I/F



BlueRF RXMODE2 – Bi-directional I/F



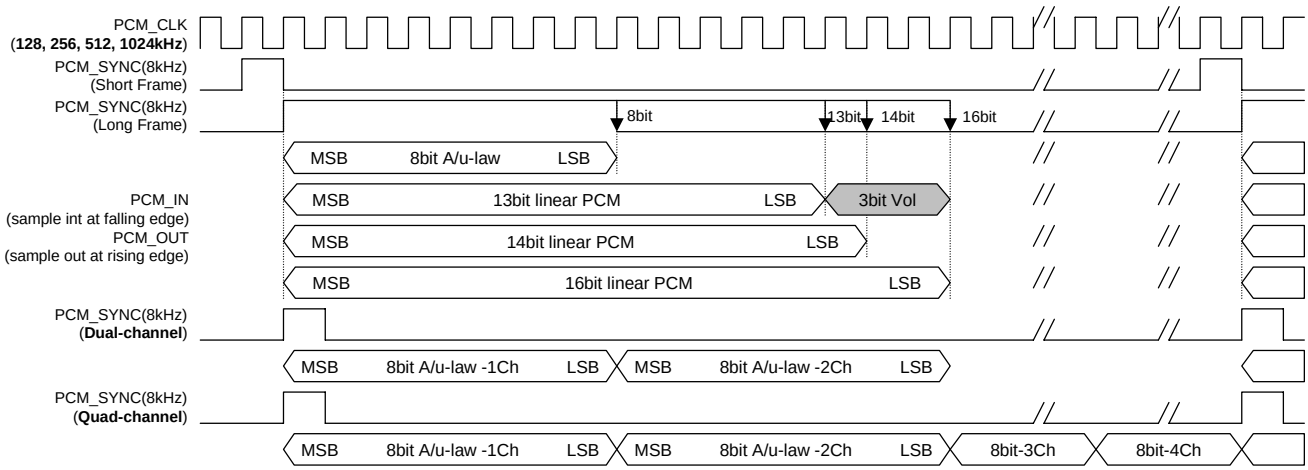
BlueQ

External PCM interface

PCMIN, PCMOUT, PCMCLK, PCMSYNC carry one channel of voice data using 8-bit A/u-law, 13-bit /14-bit/16-bit linear PCM at 8kbps. PT8R1202 generates PCMCLK and PCMSYNC as both outputs or input, which can be programmed, and interfaces directly to PCM audio devices. PCMSYNC operates at fixed clock frequency of 8KHz. PCMCLK operates at one of two fixed clock frequencies such as 128 and 256kHz. PCM interface supports both long frame sync signal and short frame sync signal. Additionally, PT8R1202 supports two or four channels of 8-bit A/u-law PCM interfacing with external multi-channel codec.

Table 8. Configuration of external PCM interface

Configuration	Supporting device	PCM type	Frame type	Bit length	PCMCLK clock	Channel number
8bit A/u-law codec	Qualcomm MSM	A, u-law	L	8bit	128kHz	1
	Motorola MC145481	A, U-law	S/L	8bit	128/256kHz	1
	Oki MSM7717	A, U-law	L	8bit	128/256kHz	1
	Oki MSM7704	A, U-law	L	8bit	128/256kHz	2(dual)
	Oki MSM7705	A, U-law	L	8bit	256KHz	4(quad)
13bit linear PCM	Motorola MC145483	Linear	S/L	13bit	128/256kHz	1, 2(volume)
14bit linear PCM	Oki MSM7716	Linear	L	14bit	128/256kHz	1
16bit linear PCM	TBD	Linear	S/L	16bit	128/256kHz	1



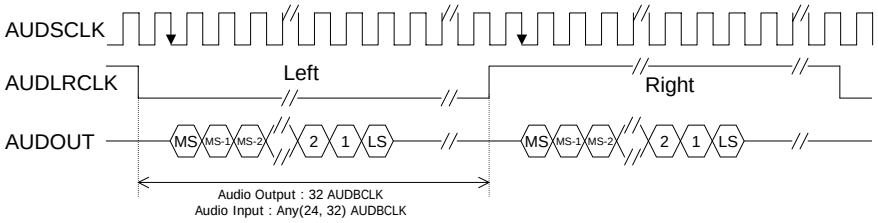
External Audio ADC/DAC, SPDIF input interface

Audio ADC/DAC interface provides a high quality multi resolution(16/18/20/24-bit) digital audio connection to external audio devices. ADI interface supports I2S audio format as well as optional left-justified or right-justified audio format. ADI interface produces one 64-bit frame at the audio sample frequency using a bit clock and frame sync signal in master mode. In slave mode, ADI accepts one 64-bit frame in audio DAC or one 64/48-bit frame at the audio sample frequency using external generated control signal. ADI interface supports several audio sampling frequency up to 96-kHz such as 32, 44.1, 48, 64, 88.2, or 96-kHz, of which 256 or 384 times main clock can be generated from on-chip audio PLL or external clock signal by interface mode programming. ADI interface contains dual on-chip FIFO which size contains maximally 2048 samples with 16-bit or 1024 samples with above 16-bit stereo audio data through YMEM2 shared with RISC/DSP processor.

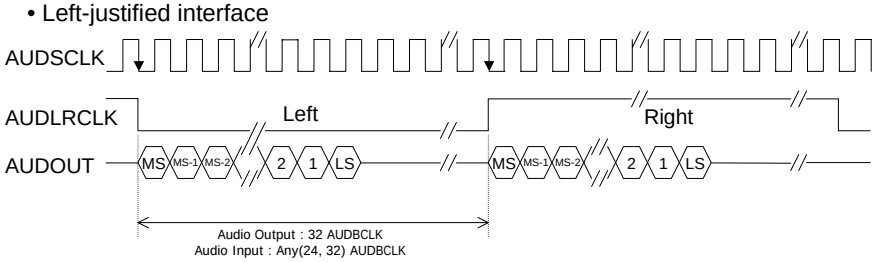
Table 9. Audio interface pin description

Pin Name	I/O	Type	Description
AUDMCLK	programmable	clock	audio oversampled clock This clock can be programmed 256 or 384 times AUDLRCLK
AUDSCLK	programmable	clock	audio serial data bit clock This clock is fixed at 64 times AUDLRCLK in output, but can be programmed at 64 or 48 times AUDLRCLK or UARTRTS in input
AUDLRCLK	programmable	clock	audio frame synchronization clock This clock can be programmed up to 96kHz
AUDOUT	output	serial data	audio serial data used for sending playback data to DAC
AUDIN	input	serial data	audio serial data used for receiving recording data from ADC SPDIF serial data input
UARTRTS	programmable	clock	audio input serial data bit clock This pin can be programmed as alternative audio serial data bit clock for audio input interface
UARTCTS	programmable	clock	audio input frame synchronization clock This pin can be programmed as alternative audio frame synchronization for audio input interface

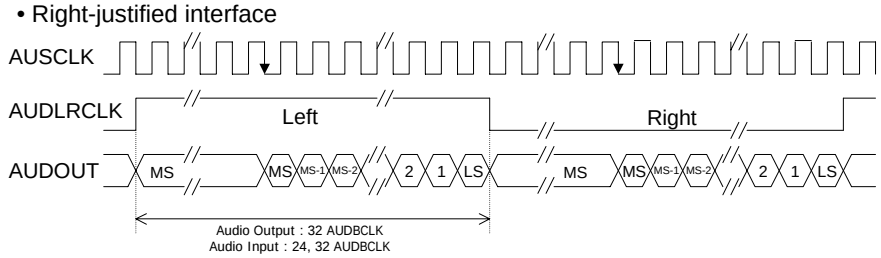
• I²S interface



• Left-justified interface

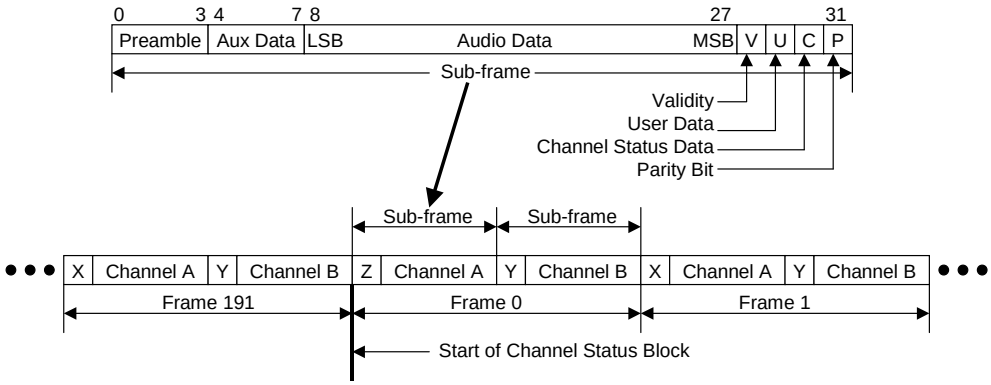


• Right-justified interface



SPDIF interface

The PT8R1202 supports IEC-958 or SPDIF serial digital input or output data directly. Through SPDIF interface, uncompressed audio PCM or compressed PCM can be transferred into or from the PT8R1202 in order to do wireless audio streaming solution. The function of SPDIF and I2S input shall be executed in the time share way. The function of SPDIF and I2S output can be executed in the same time. Following figure shows the supported data format in the PT8R1202.



USB interface

USB controller in PT8R1202 is compliant USB 1.1 version. The USB functionality is executed by an USB hardware block and firmware running on V6 RISC processor. This configuration allows acceleration of the intensive function processing while allowing flexibility in the implementation of higher level protocols over USB. USB controller in PT8R1202 supports both 12Mbps high speed mode and 1.5Mbps low speed mode and host and device mode programmed by firmware.

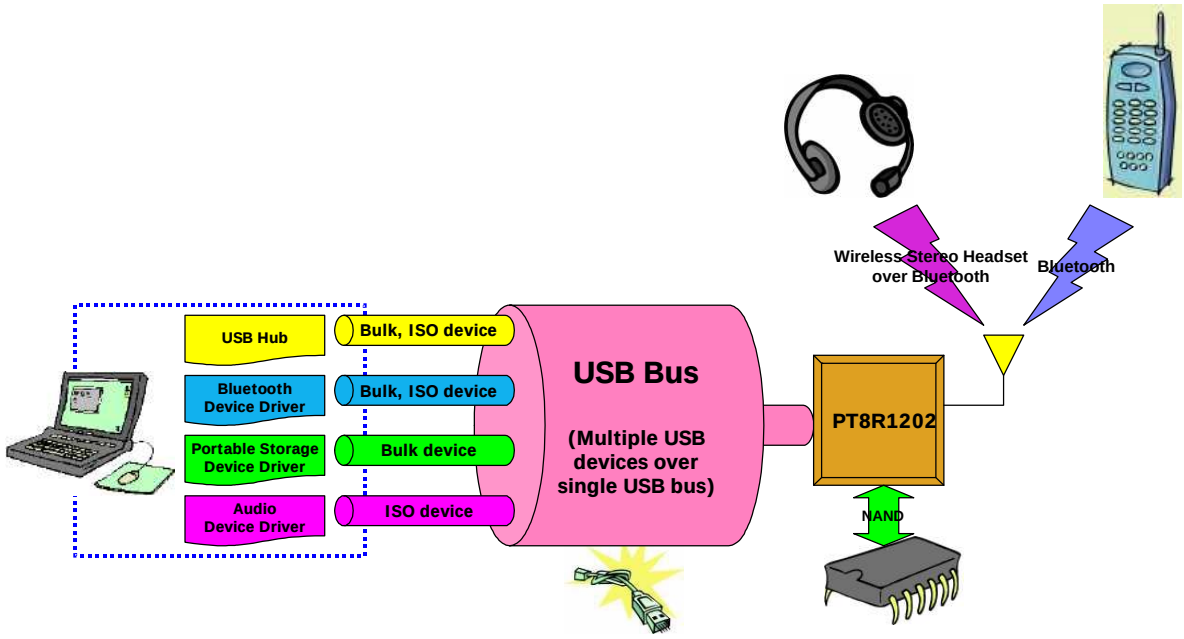
The USB hardware block consists of a serial interface engine(SIE), a serial bus controller(SBC) and a V6PB bus interface. The SIE performs the clock/data separation, NRZI encoding and decoding, bit stuffing and unstuffing, CRC generation and checking and the serial-parallel data conversion. The SBC consists of protocol engine and a USB device with nine endpoints including endpoint0 for control, each with single or double buffered scheme. Control endpoint consists of single 16-byte FIFO for transmit and receive, and eight endpoints consist of dual 64-byte FIFOs in each side, which is shared through XMEM2 with on-chip RISC processor. Four of eight endpoints are for transmit and others for receiving. Additionally, there are four endpoints dedicated to isochronous operation with 1023-byte FIFO located in XMEM2. The SBC manages the device address, monitors the status of the transactions, manage the FIFOs and communicates to the processor through a set of status and control registers. The V6PB bus interface connects the serial bus controller to the processor.

- Endpoint 0 (EP0) : Control Endpoint equipped with 16bytes single-buffered FIFO
- Endpoint 1 (EP1) : OUT Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 2 (EP2) : IN Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 3 (EP3) : OUT Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 4 (EP4) : IN Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 5 (EP5) : OUT Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 6 (EP6) : IN Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 7 (EP7) : OUT Endpoint (isochronous) with 1023bytes single-buffered FIFO
- Endpoint 8 (EP8) : IN Endpoint (isochronous) with 1023bytes single-buffered FIFO
- Endpoint 9 (EP9) : OUT Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 10 (EP10) : IN Endpoint (control, interrupt, bulk) with 64bytes double-buffered FIFO
- Endpoint 11 (EP11) : OUT Endpoint (isochronous) with 1023bytes single-buffered FIFO
- Endpoint 12 (EP12) : IN Endpoint (isochronous) with 1023bytes single-buffered FIFO

PT8R1202 supports device function, Hub function and host function in USB 1.1 version. Specially, PT8R1202 emulates the multiple device operations simultaneously with supporting Hub function. Together with on-chip Nand flash controller and audio DSP, PT8R1202 supports multiple function in USB dongle which integrates Bluetooth, USB storage device and USB sound card. Following list is possible configuration for multiple USB device system on a chip.

Table 10. Recommend Endpoint mapping in USB

End point	Bluetooth USB dongle	Bluetooth USB dongle + USB storage device	Bluetooth USB dongle + USB storage device + USB sound device
EP0	Common control	Common control	Common control
EP1(Out)	BT Event (interrupt)	BT Event (interrupt)	BT Event (interrupt)
EP2(In)	BT Command (control)	BT Command (control)	BT Command (control)
EP3(Out)	BT ACL data (Bulk)	BT ACL data (Bulk)	BT ACL data (Bulk)
EP4(In)	BT ACL data (Bulk)	BT ACL data (Bulk)	BT ACL data (Bulk)
EP5(Out)	reserved	HUB	HUB
EP6(In)	reserved	reserved	USB audio control
EP7(Out)	BT SCO data (Isoch)	BT SCO data (Isoch)	BT SCO data (Isoch)
EP8(In)	BT SCO data (Isoch)	BT SCO data (Isoch)	BT SCO data (Isoch)
EP9(Out)		USB storage (Bulk)	USB storage (Bulk)
EP10(In)		USB storage (Bulk)	USB storage (Bulk)
EP11(Out)	reserved	reserved	USB audio stream (Isoch)
EP12(In)	reserved	reserved	USB audio stream (Isoch)



UART interface

UARTTX, UARTRX, UARTRTS, and UARTCTS form a conventional asynchronous data serial port. The interface is designed to operate correctly when connected to other UART devices such as NS16550A. The signaling levels are 0V and 3.3V. The interface is programmable over a variety of bit rates. It supports many configurations such as no, even or odd parity, one or two stop bit, number of bit in a frame, break conditions, and hardware flow control on or off. The maximum UART data rates is 1.8Mb/s. Two-way hardware control is implemented by UARTRTS and UARTCTS. If input UARTCTS signal becomes high, transmission will be stopped, else it will be continued. If internal UART FIFO will be full, output UARTRTS signal becomes high, else becomes low.

Flash Card interface

PT8R1202 supports two types of flash card such as SmartMedia™ flash devices and MMC or SDCard flash devices. This flash card devices are small removable cards that contain one or two NAND Flash devices. Alternatively, the system designer can use non-removable NAND flash chips. PT8R1202 supports hardware interface logic for SmartMedia™ devices, but only supports software firmware using GPIO for MMC or SDCard. The SmartMedia™ electrical interface uses an 8-bit data/address bus and 6-bit control lines. PT8R1202 supports up to 4GB SmartMedia™ devices.

JTAG interface

PT8R1202 supports IEEE1149.1 standard specification compliant interface. This interface supports basic test commands such as EXTEST, SMAPLE, BYPASS, and IDCODE. Beside of this, JTAG interface can be used communication channel with PTI enhanced on-chip hardware debugger controller. Using on-chip debugger controller, off-chip debug handler or external host can access internal peripheral device registers, external memory interface, and executes real-timing hardware debugging and monitoring of on-chip embedded RISC processor. Also, external host can communicate on-chip RISC processor through JTAG with on-chip hardware managed channel buffer. There are sixteen debug registers specified and these will be used in PTI own development chip manager software, named as V6EMU™. The length of instruction register in JTAG interface is 6bit and that of debug data register is 32bit. Table 11. shows the summary of TAP instructions supported in PT8R1202 and Table 12. shows the summary of debugger registers in JTAG interface.

Table 11. TAP instructions

Instruction	Opcode	Description
EXTEST	0x000000	EXTEST initiates testing of external circuitry, typically board-level interconnects and off chip circuitry. EXTEST connects the Boundary-Scan register between TDI and TDO in the SHIFT_DR state only. When EXTEXT is selected, all output signal pin values are driven by values shifted into the Boundary-Scan register and may change only on the falling-edge of TCK in the Update_DR state. Also, when EXTEST is selected, all system input pin states must be loaded into the Boundary-Scan register on the rising-edge of TCK in the Capture_DR state. Values shifted into input latches in the Boundary-Scan register are never used by the processor's internal logic.
SAMPLE	0x000001	SAMPLE / PRELOAD performs two functions: • When the TAP controller is in the Capture-DR state, the SAMPLE instruction occurs on the rising edge of TCK and provides a snapshot of the component's normal operation without interfering with that normal operation. The instruction causes Boundary-Scan register cells associated with outputs to SAMPLE the value being driven by or to the processor. • When the TAP controller is in the Update-DR state, the PRELOAD instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in the Boundary-Scan cells to the slave register cells. Typically the slave latched data is then applied to the system outputs by means of the EXTEST instruction.
IDCODE	0x011111	IDCODE is used in conjunction with the device identification register. It connects the identification register between TDI and TDO in the Shift_DR state. When selected, IDCODE parallel-loads the hard-wired identification code (32 bits) on TDO into the identification register on the rising edge of TCK in the Capture_DR state. NOTE: The device identification register is not altered by data being shifted in on TDI.
DEBUG (Private Instruction)	0x10SSSS	DEBUG instruction select the DEBUGReg with address indicator SSSS. • When the TAP controller is in the Capture-DR state, the DEBUG instruction occurs on the rising edge of TCK and executes a snapshot of DEBUG register addressed SSSS into DEBUGReg. • When the TAP controller is in the Update-DR state, the DEBUG instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in DEBUGReg to DEBUG register addressed SSSS.
BYPASS	0x111111	BYPASS instruction selects the Bypass register between TDI and TDO pins while in SHIFT_DR state, effectively bypassing the processor's test logic. 0 is captured in the CAPTURE_DR state. While this instruction is in effect, all other test data registers have no effect on the operation of the system. Test data registers with both test and system functionality perform their system functions when this instruction is selected

Table 12. Debug interface register address map

Address	Name	Attribute	Description
0x0	DEBUG_CMD	Write	debugger control register
0x1	DEBUG_CTRL	Read	debug handler control register
0x2	DEBUG_TX	Read	debug handler transmit register
0x3	DEBUG_RX	Write	debug handler receive register
0x4	DEBUG_ADDR	Write	debugger address register
0x5	DEBUG_WDATA0 (DEBUG_CYC_CNT)	Write	debugger write data register0(31:0) debugger instruction step count
0x7	DEBUG_RDATA0	Read	debugger read data register0(31:0)
0x9	DEBUG_INST_ACNT	Read	debugger instruction cycle accumulator
0xA	DEBUG_INST_SCNT	Read	debugger instruction step cycle count
0xB	DEBUG_BREAK_PC	Write	debugger breakpoint PC register

Electrical specifications

Absolute Maximum Rating

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TA	Storage Temperature		-40		150	°C
	Supply Voltages : SPLL_VCC, APLL_VCC, VCC	TA= +25°C	-0.4		2.1	V
	Supply Voltage : ACODEC_VCC		-0.4		3.6	V
	Supply Voltage : VPP		-0.4		3.6	V
	Other Terminal Voltage		-0.4		3.6	V

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TA	Ambient Temperature		-40	25	105	°C
VCC	Supply Voltage VCC (to VCC_GND)*	TA= +25°C	1.62	1.8	1.98	V
VPP	Supply Voltage VPP (to VPP_GND)*	TA=+25°C	2.7	3.0	3.6**	V
SPVCC	Supply Voltage SPLL_VCC (to SPLL_GND)*	TA=+25°C	1.62	1.8	1.98	V
APVCC	Supply Voltage APLL_VCC (to APLL_GND)*	TA=+25°C	1.62	1.8	1.98	V
ACVCC	Supply Voltage ACODEC_VCC(to ACODEC_GND)*	TA=+25°C	2.7	3.0	3.6	V
	Difference between any two VCC, SPLL_VCC, APLL_VCC terminals	TA=+25°C			0.3	V

* An external regulator is required for reliability

DC/AC Specification

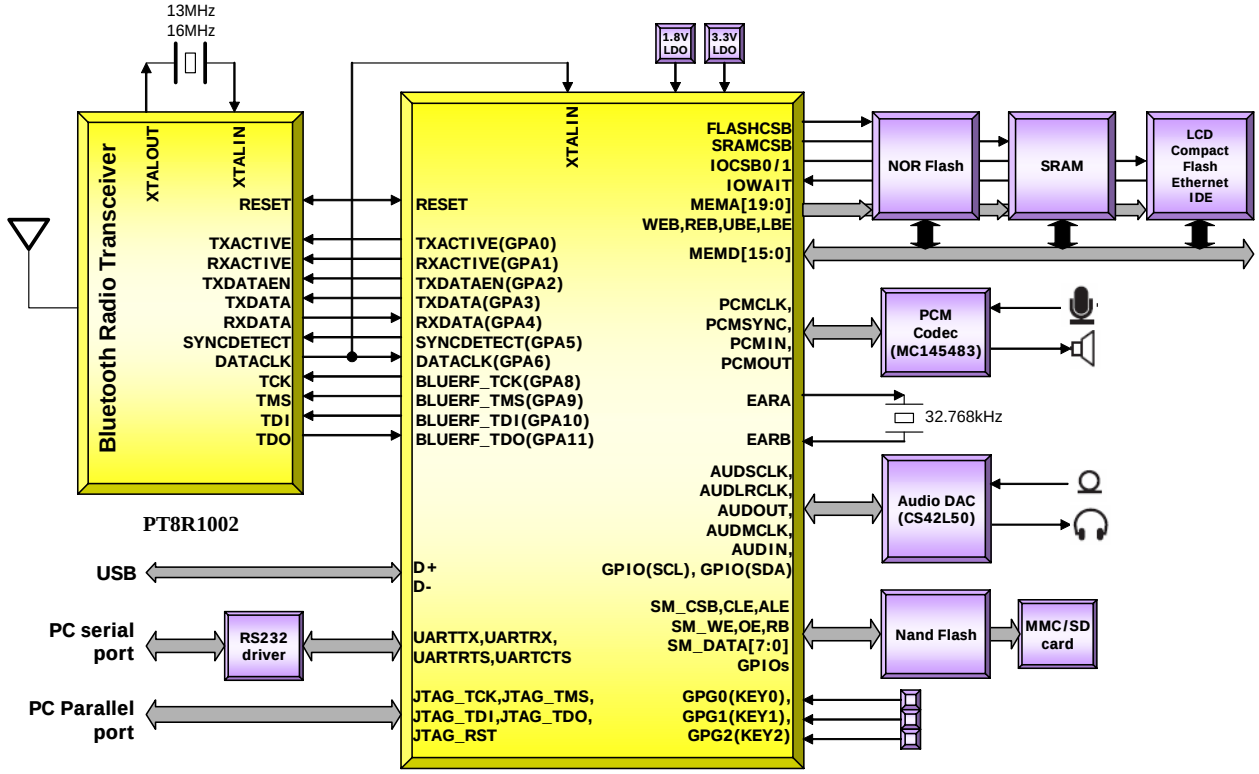
Unless otherwise noted, the specification applies for: TA=+25°C, Typical conditions

Sym	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs						
VIH	Logical input High		2.0		VPP	V
VIL	Logical input Low		-0.3		0.8	V
ILEAK	Input leakage current	0.5 < VIN < V_{CC}-0.5	-1		1	μA
Digital Outputs						
VOH	Logical output High		2.4			V
VOL	Logical output Low				0.4	V
	Tri-state output leakage current		-1		1	μA
	Low level max output current for MEMA, MEMD, REB, WEB			13.2		mA
	High level max output current for MEMA, MEMD, REB, WEB			24.8		mA
	Low level max output current for others			6.6		mA
	High level max output current for others			12.4		mA
USB Signals (D+, D-)						
VDI	Differential input sensitivity	(D+) – (D-)	-0.2		0.2	V
VCM	Differential common mode range		0.8		2.5	V
VSE	Single ended receiver threshold		0.7		1.7	V
VUOL	Output low voltage	RL=1.5K			0.3	V
VUOH	Output high voltage	RL=1.5K	2.8			V
IUOZ	Tri-state date line leakage	O < VIN < 3.3	-10		10	μA
Current Consumption						
	Operating supply current of VCC	under 96MHz operation		100		mA
	Low power mode supply current of VCC	under IDLE operation		3.5		mA
	Sleep mode supply current of VCC			0.55		mA
	Operating supply current of VPP			10		mA
	Sleep mode supply current of VPP	under oscillator operation		0.5		mA
	Operating supply current of SPLL_VCC			3.5		mA
	Sleep mode supply current of SPLL_VCC			0.35		mA
	Operating supply current of APLL_VCC			1.6		mA
	Sleep mode supply current of APLL_VCC			0.2		mA
	Operating supply current of ACODEC_VCC			11.8		mA
	Sleep mode supply current of ACODEC_VCC			0.12		mA
System Power Consumption						
	Deep sleep with RTC timer operation	VPP, ACODEC_VCC =3.0V, others all 1.8V		4.7		mW
	Sleep with RTC timer operation	VPP, ACODEC_VCC =3.0V, others all 1.8V		18.2		mW
	BT data transfer (DM5)*	VPP, ACODEC_VCC =3.0V, others all 1.8V		41		mW
	BT voice connection (HV1)*	VPP, ACODEC_VCC =3.0V, others all 1.8V		45		mW
	MP3 decoding from NAND flash*	VPP, ACODEC_VCC =3.0V, others all 1.8V		111		mW
	MP3(128kbps) streaming from Bluetooth link*	VPP, ACODEC_VCC =3.0V, others all 1.8V		139		mW
	SBC(384kbps) streaming from Bluetooth link*	VPP, ACODEC_VCC =3.0V, others all 1.8V		91		mW
	VOIP(G.723.1) call with Bluetooth link*	VPP, ACODEC_VCC =3.0V, others all 1.8V		136		mW

* The actual power consumption depends on real situation.

Application Note

PT8R1202 reference configuration



Applications

- Wireless speaker for DVD / PC surround speaker with CD quality, low-latency audio transmission
- Portable digital audio player with Bluetooth streaming and storage function
- Bluetooth stereo headset with combining A/V profile and headset profile
- 3-in-one multi-functions(Bluetooth, USB audio, USB flash storage) USB dongle
- Bluetooth USB printer adaptor with USB host function
- Bluetooth handsfree with on-chip echo cancellation function
- Bluetooth VOIP phone with on-chip speech compression function

Notes

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