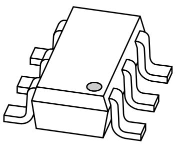


PMN50XP

P-channel TrenchMOS extremely low level FET

Rev. 01 — 23 January 2006 **Product data sheet**

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low threshold voltage
- Low on-state losses

1.3 Applications

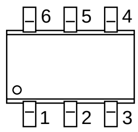
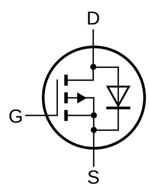
- Low power DC-to-DC converters
- Load switching
- Battery management
- Battery powered portable equipment

1.4 Quick reference data

- $V_{DS} \leq -20$ V
- $R_{DSon} \leq 60$ mΩ
- $I_D \leq -4.8$ A
- $Q_{GD} = 1.3$ nC (typ)

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 5, 6	drain (D)	 SOT457 (TSOP6)	
3	gate (G)		
4	source (S)		

3. Ordering information

Table 2: Ordering information

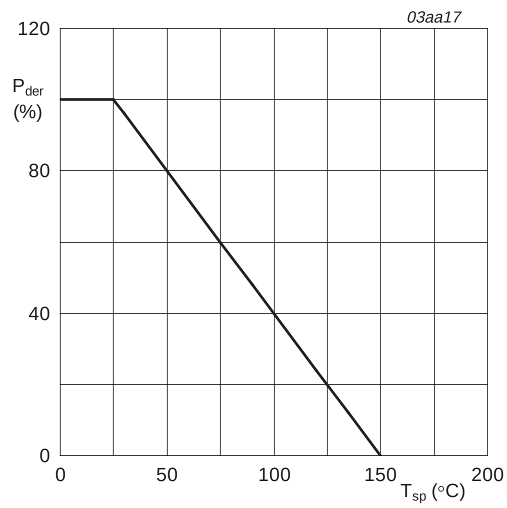
Type number	Package		
	Name	Description	Version
PMN50XP	TSOP6	plastic surface mounted package (TSOP6); 6 leads	SOT457

4. Limiting values

Table 3: Limiting values

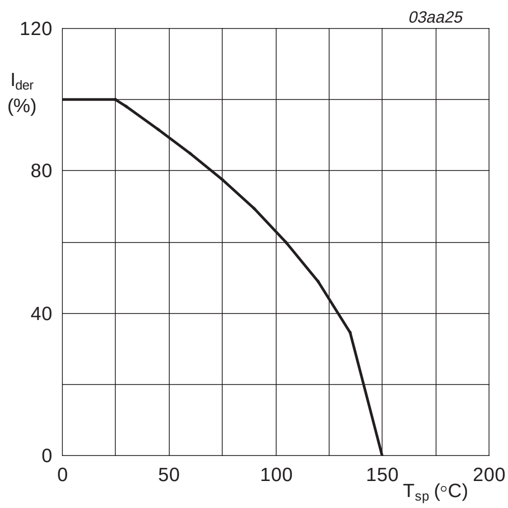
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	–20	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	–20	V
V_{GS}	gate-source voltage		-	±12	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = –4.5 V; see Figure 2 and 3	-	–4.8	A
		T_{sp} = 100 °C; V_{GS} = –4.5 V; see Figure 2	-	–3	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	–19.4	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1	-	2.2	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	–1.9	A
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	–7.5	A



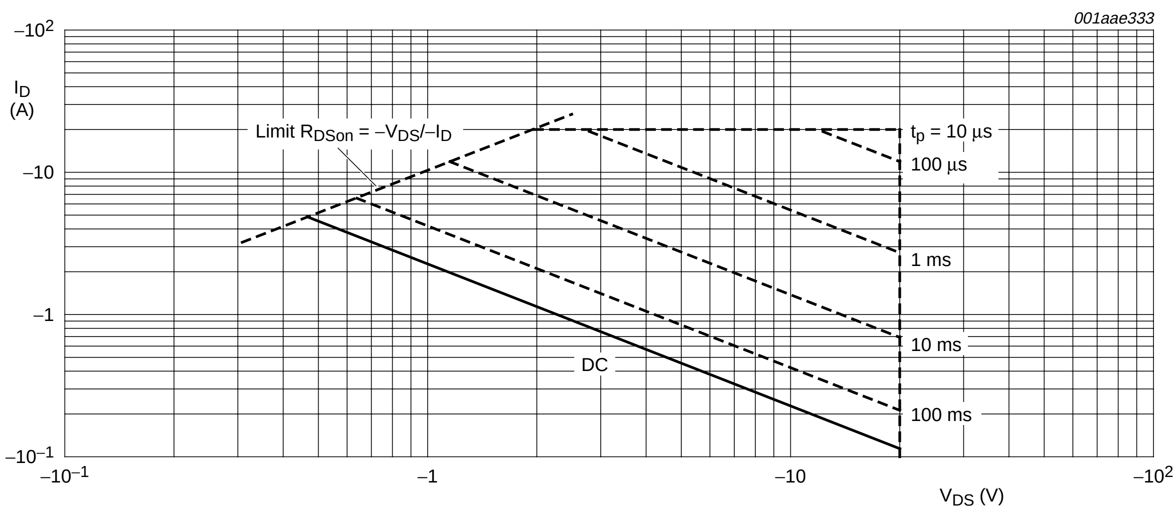
$$P_{der} = \frac{P_{tot}}{P_{tot(25\ ^{\circ}C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\ ^{\circ}C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	55	K/W

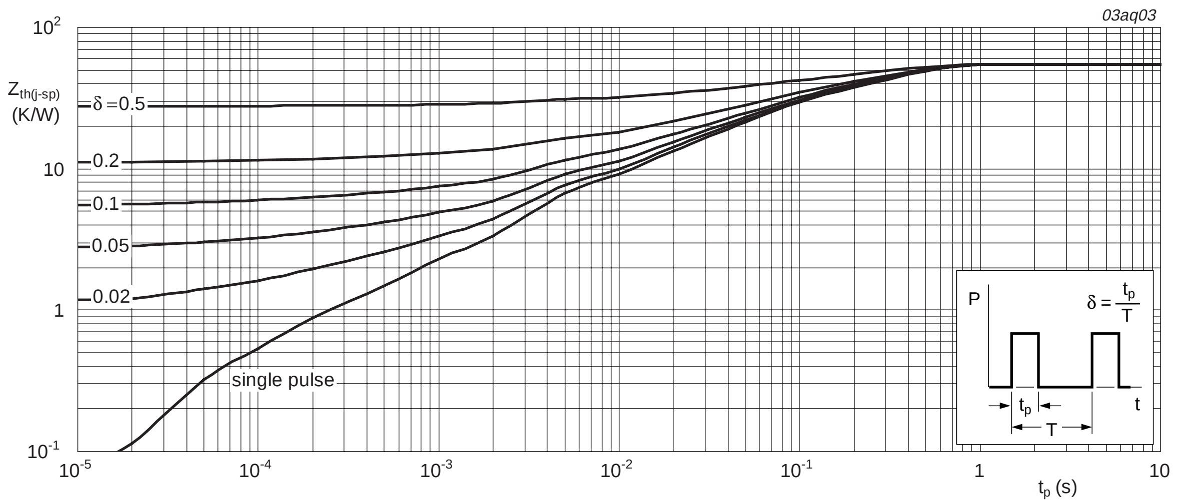


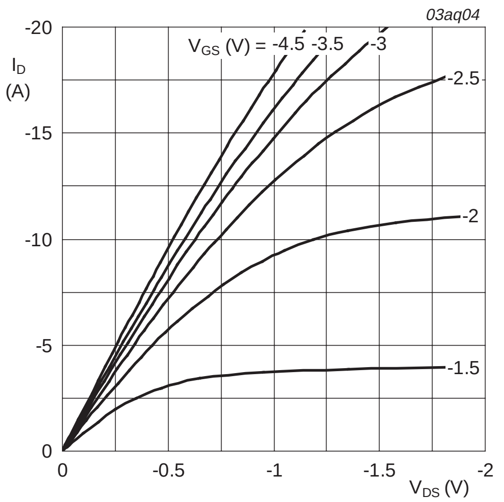
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

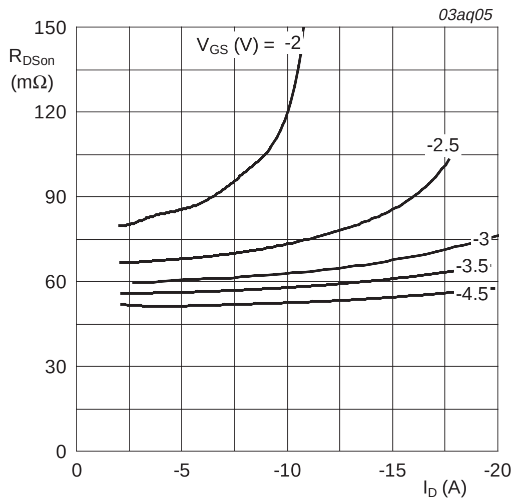
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = –250 µA; V_{GS} = 0 V				
		T_j = 25 °C	–20	-	-	V
		T_j = –55 °C	–18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = –0.25 mA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	–0.55	–0.75	–0.95	V
		T_j = 150 °C	–0.35	-	-	V
		T_j = –55 °C	-	-	–1.1	V
I_{DSS}	drain leakage current	V_{DS} = –20 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	–1	µA
		T_j = 70 °C	-	-	–5	µA
I_{GSS}	gate leakage current	V_{GS} = ±12 V; V_{DS} = 0 V	-	–10	–100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –2.8 A; see Figure 6 and 8				
		T_j = 25 °C	-	48	60	mΩ
		T_j = 150 °C	-	77	96	mΩ
		V_{GS} = –2.5 V; I_D = –2.3 A; see Figure 6 and 8	-	65	80	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = –4.7 A; V_{DS} = –10 V; V_{GS} = –4.5 V; see Figure 11 and 12	-	10	-	nC
Q_{GS}	gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	1.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	–1.6	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = –20 V; f = 1 MHz; see Figure 14	-	1020	-	pF
C_{oss}	output capacitance		-	140	-	pF
C_{rss}	reverse transfer capacitance		-	100	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = –10 V; R_L = 10 Ω; V_{GS} = –4.5 V; R_G = 6 Ω	-	8.5	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
t_f	fall time		-	35	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = –1.7 A; V_{GS} = 0 V; see Figure 13	-	–0.77	–1.2	V



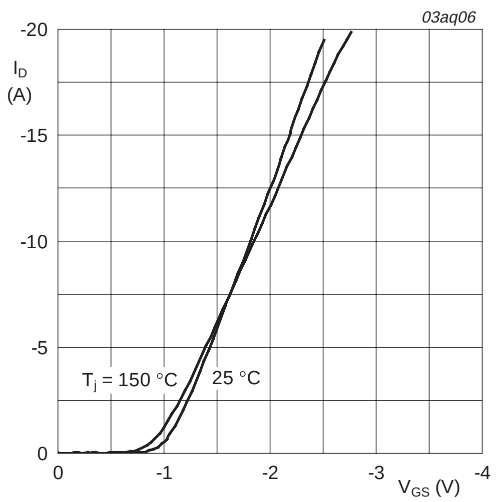
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



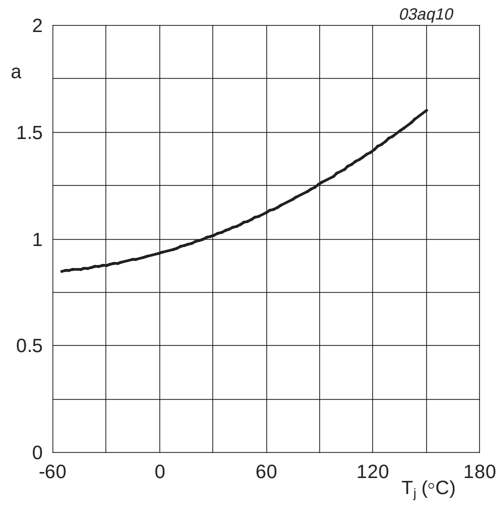
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



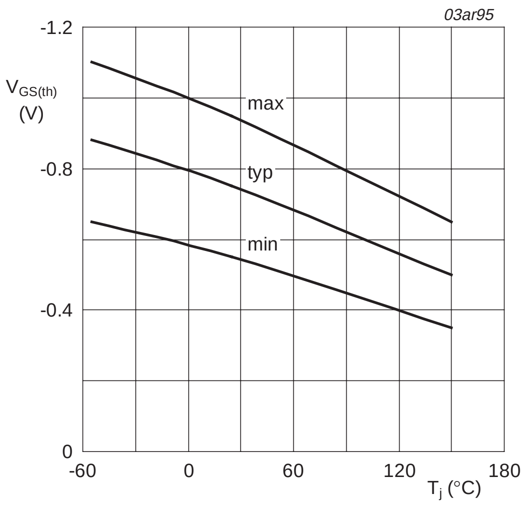
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



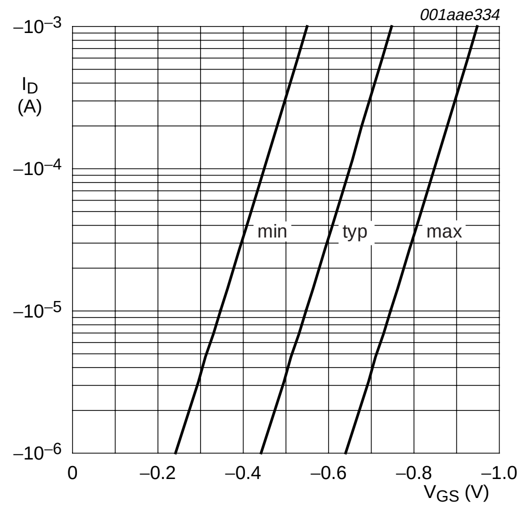
$$a = \frac{R_{DSon}}{R_{DSon(25\ ^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



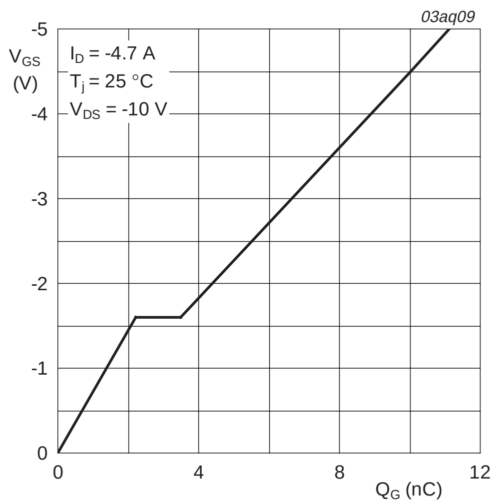
I_D = –0.25 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = –5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = –4.7 A; V_{DS} = –10 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

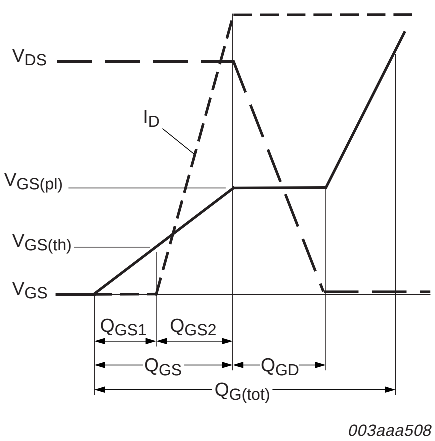
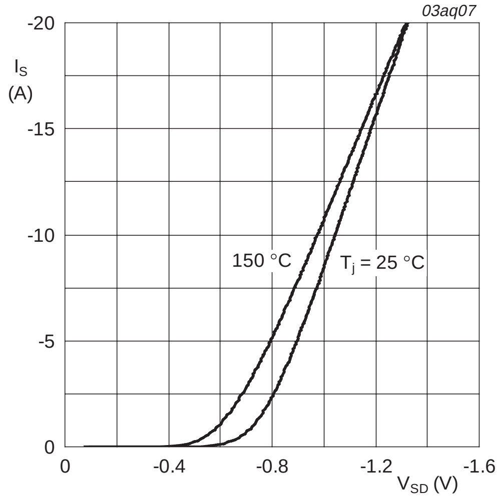
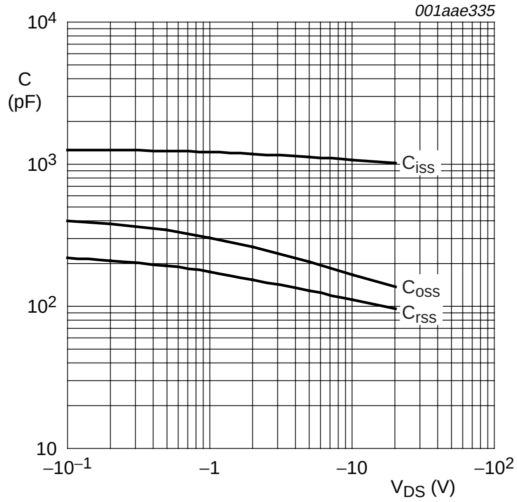


Fig 12. Gate charge waveform definitions



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source current as a function of source-drain voltage; typical values

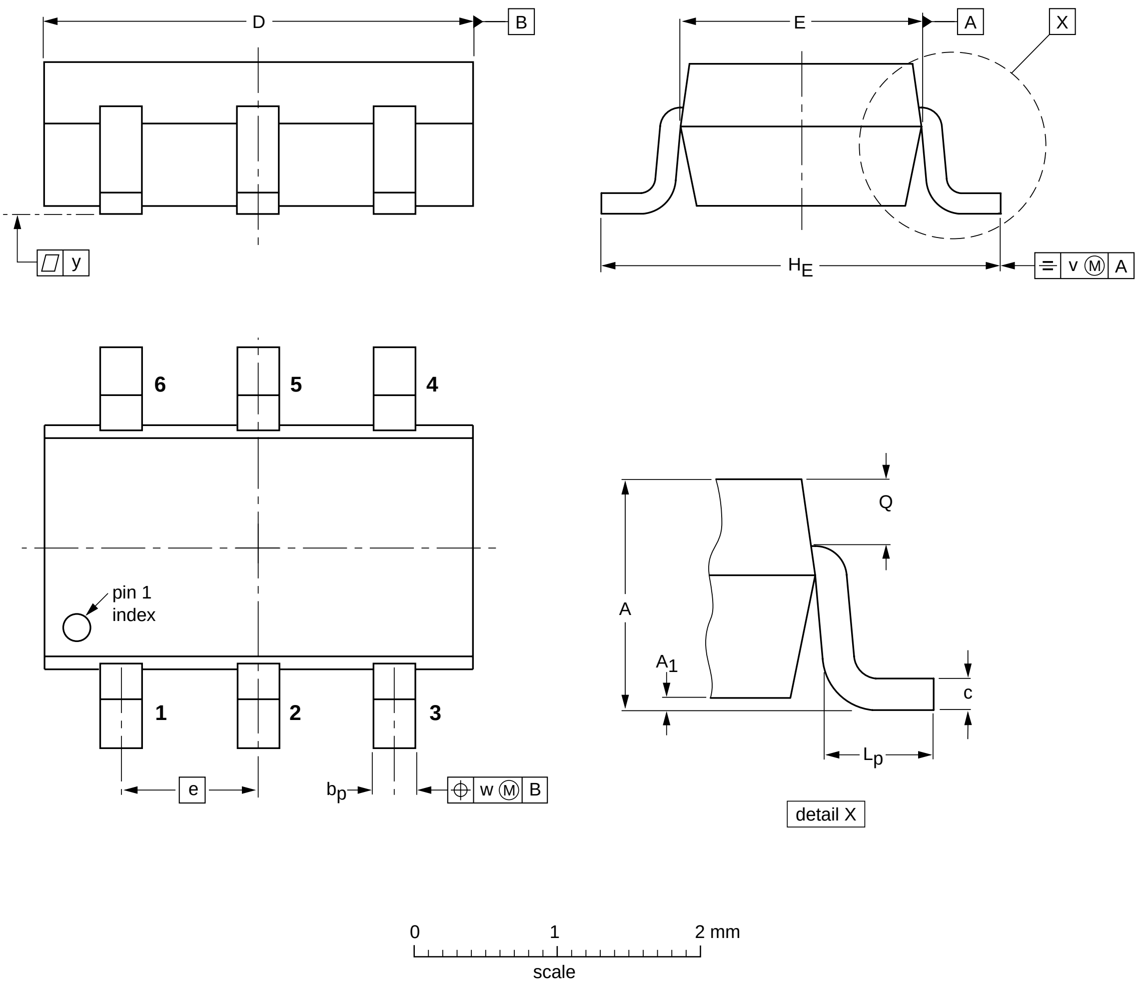


V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~04-11-08~~ 05-11-07

Fig 15. Package outline SOT457 (TSOP6)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMN50XP_1	20060123	Product data sheet	-	-	-

9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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14. Contents

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