ATM Layer Solution

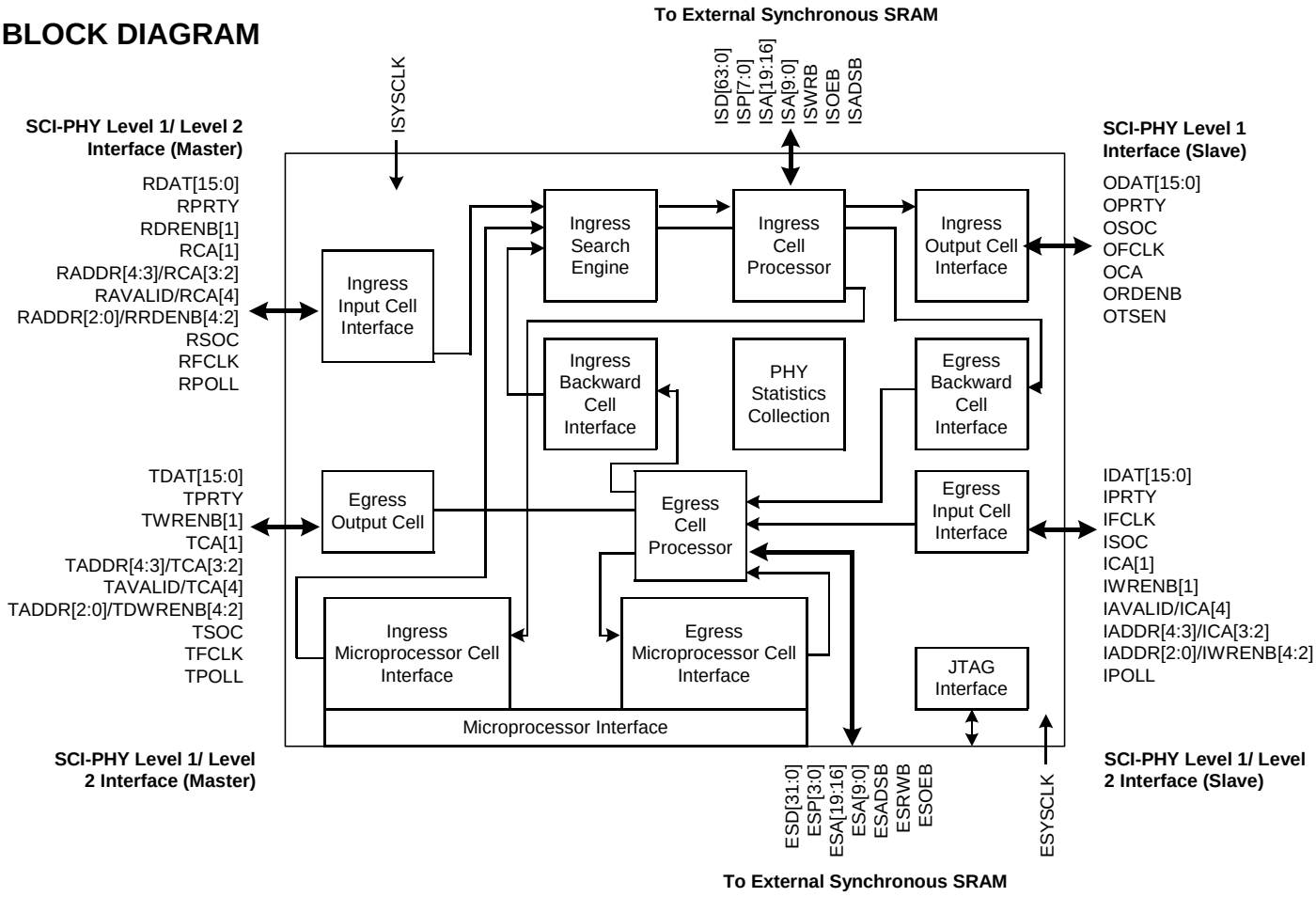
FEATURES

- Monolithic single chip device which handles bi-directional ATM Layer functions including VPI/VCI address translation, cell appending, policing (ingress only), cell counting and OAM requirements for 1024 VCs (virtual connections).
- Instantaneous bi-directional transfer rate of 800 Mbit/s supports a bi-directional cell transfer rate of $1.42x10^6$ cell/s.
- Ingress input interface supports an 8 or 16 bit PHY interface using direct addressing for up to 4 PHY devices (Utopia Level 1) and Multi-PHY addressing for up to 32 PHY devices (Utopia Level 2).
- Ingress output interface supports an 8 or 16 bit SCI-PHY (52 - 64 byte cell) interface (Utopia Level 1) to a switch fabric.
- Egress input and output interfaces support an 8 or 16 bit SCI-PHY (52 - 64 byte cell) interface using direct addressing for up to 4 PHY devices (Utopia Level 1) and Multi-PHY addressing for up to 32 PHY devices (Utopia Level 2).
- Compatible with the PM7329 S/UNI-APEX-1K800 Traffic Manager, and PMC-Sierra's VORTEX Architecture.
- Ingress functionality includes a highly flexible search engine that covers the entire PHYID/VPI/VCI address range, dual leaky bucket policing, per-VC cell counts, OAM-FM and OAM-PM processing.
- Egress functionality includes direct address lookup, per-VC cell counts, OAM-FM and OAM-PM processing. Per-PHY output buffering scheme resolves the head-of-line blocking issue.
- Includes a FIFO buffered 16-bit microprocessor bus interface for cell insertion and extraction, deterministic VC Table access, status monitoring and configuration of the device.
- Supports DMA access for cell extraction.
- The UTOPIA and external SRAM interfaces are 52 MHz max.

POLICING

- ITU-I.371, ATM Forum TM4.0 compliant, per-VC programmable dual leaky bucket policing with a programmable action (tag, discard, or count only) for each bucket, each with 3 programmable 16 bit non-compliant cell counts.
- Per-PHY single leaky bucket policing with a programmable action (tag, discard, or count only).

BLOCK DIAGRAM



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- Guaranteed Frame Rate (GFR) Policing with Minimum Cell Rate Frame Tagging.

OAM

- ITU-I.610 compliant OAM on both Ingress and Egress directions.
- Complete Fault Management (AIS, RDI, CC) processing, for VP/VC, Segment/End-to-end flows on all VCs.
- Complete Performance Monitoring processing, for VP/VC, Segment/End-to-end, Forward/Backward flows, on 256 Bi-directional VCs.

CELL COUNTING

- Per-VC counts include CLP0 cells, CLP1 cells, policing violations.
- Per-PHY counts include CLP0 cells, CLP1 cells, OAM cells, errored OAM cells, unassigned/invalid cells and policing violations.
- Per-device counts include total cells received/transmitted, and physical layer cells.

PACKAGING

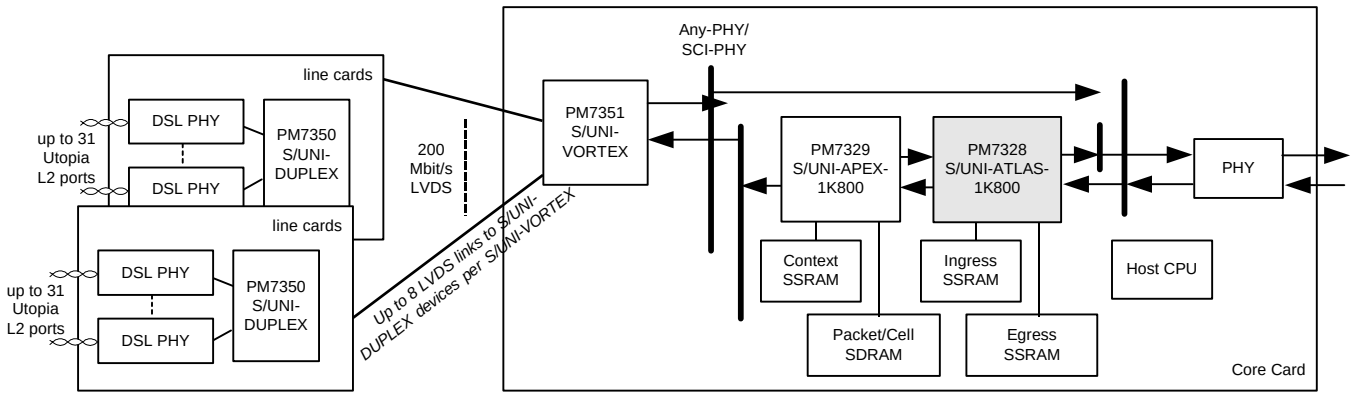
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 0.35 micron, 3.3V CMOS technology with a 3.3V UTOPIA (SCI-PHY), 3.3/5V Microprocessor I/O interfaces and 3.3V external synchronous SRAM interfaces.
- Packaged in 432-pin ball grid array (BGA) package.

APPLICATIONS

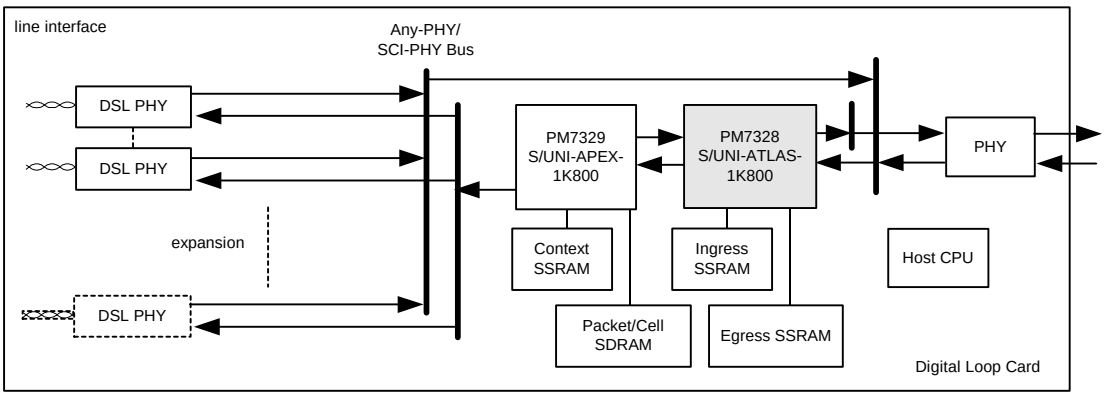
- Mini Digital Subscriber Loop Access Multiplexer (Mini-DSLAM).
- Subscriber Access Equipment.
- Digital Loop Card Traffic Aggregation.

TYPICAL APPLICATION

S/UNI-ATLAS-1K800 IN OC3 MINI-DSLAM APPLICATION



S/UNI-ATLAS-1K800 IN OC3 DIGITAL LOOP CARD APPLICATION



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

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