1.8V-3.3V PicoTreo™, 3-PLL, 200MHz, 5 Output Clock IC

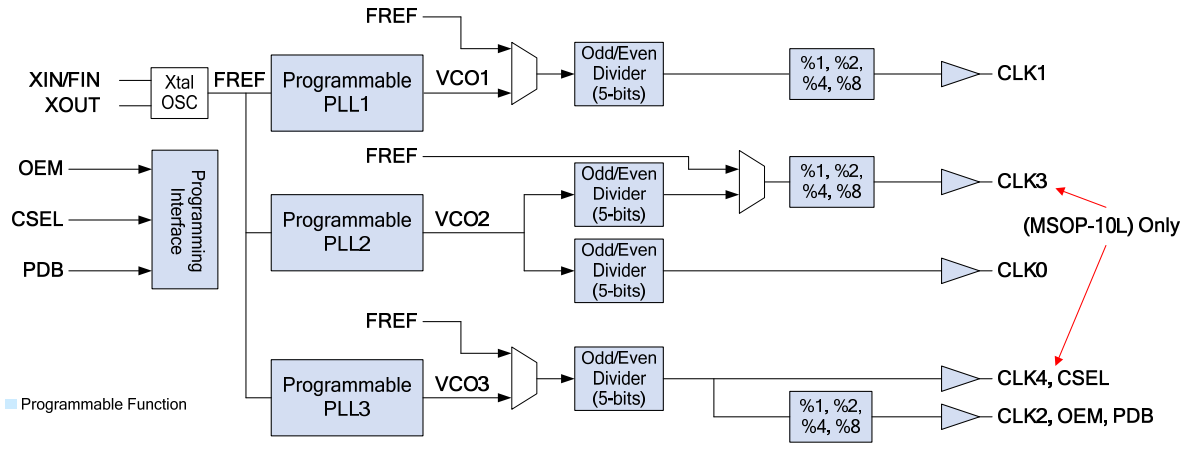
FEATURES

- Designed for PCB space savings with 3 low-power Programmable PLLs and up to 5 clock outputs.
- Low-power consumption (<10µA when PDB is activated)
- Output Frequency:
  - o ≤133MHz @ 1.8V operation
  - o ≤166MHz @ 2.5V operation
  - o ≤200MHz @ 3.3V operation
- Input Frequency:
  - o Fundamental Crystal: 10MHz - 50MHz
  - o Reference Input: 1MHz - 200MHz
- Programmable I/O pins can be configured as Output Enable (OE), Power Down (PDB) inputs, Configuration Select (CSEL) or Clock outputs.
- Disabled outputs programmable as HiZ or Active Low
- Two distinct configurations selectable with CSEL (MSOP-10L Only)
- Single 1.8V ~ 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in GREEN/RoHS compliant 8-pin SOP or 10-pin MSOP packages.

DESCRIPTION

The PL613-05 is an advanced triple PLL design based on PhaseLink's PicoPLL™, world's smallest programmable clock, technology. This flexible programmable architecture is ideal for high performance, low-power, low-cost applications. When using the power down (PDB) feature the PL613-05 consumes less than 10 µA of power, while its Configuration Select (CSEL) function allows switching of 2 programmable configurations. Besides its small form factor and 3 or 5 outputs that can reduce overall system costs, the PL613-05 offers superior phase noise, jitter and power consumption performance.

BLOCK DIAGRAM



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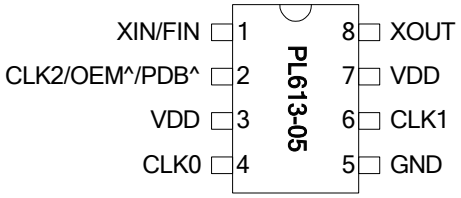
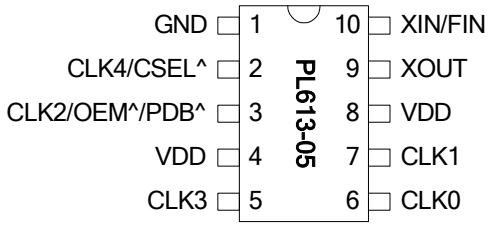
PIN CONFIGURATION



SOP-8L



MSOP-10L

^ Denotes internal pull up

PACKAGE PIN ASSIGNMENT

Name	Package Pin #		Type	Description
	MSOP-10L	SOP-8L		
GND	1	5	P	GND connection
CLK4/CSEL	2	-	B*	- Programmable Clock (CLK4) output or - Configuration Switching input
CLK2/OEM/PDB	3	2	B*	- Programmable Clock (CLK2) output, or - Output Enable Master (OEM) for all clock outputs, or - Power Down mode (PDB) input
VDD	4, 8	3, 7	P	VDD connection
CLK3	5	-	O	Programmable Clock (CLK3) output
CLK0	6	4	B*	Programmable Clock (CLK0) output
CLK1	7	6	O	Programmable Clock (CLK1) output
XOUT	9	8	O	Crystal output pin. Do Not Connect when using FIN
XIN/FIN	10	1	I	Crystal or Reference Clock input

*** Note**: All bidirectional buffers (I/Os) incorporate an internal 60KΩ pull up resistor except when PDB mode is used. In configurations that use PDB, the PDB pin will have a 10MΩ pull up resistor.

KEY PROGRAMMING PARAMETERS

CLK[0:4] Output Frequency	Output Drive Strength	Programmable Input/Output
CLK[0] F_{VCO2} / P CLK[1,2] F_{VCOx} / (P*(1,2,4,8)) or F_{REF} / (P*(1,2,4,8)) CLK[3] F_{VCO2} / (P*(1,2,4,8)) or F_{REF} / (P*(1,2,4,8)) CLK[4] F_{VCO3} / P or F_{REF} / P Where $F_{VCO} = F_{REF} * M / R$ M = 11 bit R = 8 bit P = 5 bit (Odd/Even Divider)	Each output has three optional drive strengths to choose from. They are: • Low: 4mA • Std: 8mA (default) • High:16mA	Most pins are multi-function I/Os and can be configured as: • OEM – (Master OE controlling all outputs) • CSEL – (Device Configuration Switching) • PDB – (Power Down) • CLK[0:4] – (Output) • HiZ or Active Low disabled state

FUNCTIONAL DESCRIPTION

The PL613-05 is a highly featured, very flexible, advanced triple PLL design for high performance, low-power applications. The device accepts a low-cost fundamental crystal input of 10MHz to 50MHz or a reference clock input of 1MHz to 200MHz and is capable of producing 3 (SOP-8L) or 5 (MSOP-10L) distinct output frequencies up to 200MHz. All 3-PLLs are fully programmable, with a total of four, 5-bit Post VCO, Odd/Even (patent pending) 'P-counter' dividers with additional 1, 2, 4 or 8 'Post P-counter' dividers to allow generating the most demanding frequencies easily. The outputs can be programmed to deliver the generated frequencies from the PLLs, or the reference input. Each bidirectional feature pin (I/O) on the PL613-05 incorporates a 60KΩ pull up resistor (10MΩ for PDB function) and can be configured to perform various functions. Usage of various design features of these products is mentioned in the following paragraphs.

PLL Programming

The three PLLs in PL613-05 are fully programmable. Each PLL is equipped with an 8-bit input frequency divider (R-Counter) and an 11-bit VCO frequency feedback loop (M-Counter) divider. The three PLL outputs are transferred to four 5-bit post VCO, Odd/Even (patent pending) dividers (P-Counter), as shown in the above diagrams. In addition, there are three optional (÷1, ÷2, ÷4 or ÷8) post P-Counter dividers, that can further divide the VCO frequencies. In general, the PLL output frequency is determined by the following formula

$$F_{OUT} = (F_{REF} * M) / (R * P)$$

For output calculations, please note that 'P' includes the 'P' counter bits plus the additional optional (÷1, ÷2, ÷4 or ÷8) dividers, if used.

CLKx (Clock Outputs)

There are a maximum of 3 (SOP-8L) or 5 (MSOP-10L) outputs available on the PL613-05. Clock output frequencies can be configured as follows:

CLK[0]
F_{VCO2} / P

CLK[1,2]
F_{VCOx} / (P*(1,2,4,8)) or F_{REF} / (P*(1,2,4,8))

CLK[3]
F_{VCO2} / (P*(1,2,4,8)) or F_{REF} / (P*(1,2,4,8))

CLK[4]
F_{VCO3} / P or F_{REF} / P

Each output can be programmed with a 4mA, 8mA, or 16mA drive strength. The maximum output frequency is 200MHz @ 3.3V, 166MHz @ 2.5V or 133MHz @ 1.8V.

OEM (Master Output Enable)

One pin can be configured to be a single Master OE (OEM) input pin that controls all the outputs of the PL613-05. In addition the state of the disabled outputs can be programmed to float (Hi Z) or Active '0'. The OEM pin incorporates a 60kΩ pull up resistor for normal operating condition. The logic for OEM is shown below:

OEM Pin	OE Type (Programmable)	Osc	PLL	Output
0	0 (Default)	On	On	Hi Z
	1	On	On	Active '0'
1	Normal Operation (Default)			

Note: Typical enable time is 10ns.

Power-Down Control (PDB)

When activated, PDB 'Disables all the PLLs, the oscillator circuitry, counters, and all other active circuitry. PDB activation disables all outputs and the IC consumes <10µA of power. The PDB input incorporates a 10MΩ pull up resistor for normal operating condition.

The PDB feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode. The logic for PDB is shown below:

PDB Pin	PDB Type Program	Osc	PLL	Output
0	0 (Default)	Off	Off	Hi Z
	1	Off	Off	Active '0'
1	Normal Operation (Default)			

Note: Typical enable time is <2ms.

On-The-Fly Configuration Switching (CSEL)

The PL613-05 can be programmed to allow switching between 2 different configurations, allowing for changes in the output frequency and other feature changes. Many applications (i.e. video/audio) can use the same design footprint, but allow for configuration switching, adhering to various standards. CSEL is used to make the switching selection. This pin incorporates a 60kΩ pull up resistor for normal operating condition. The logic for configuration switching of the programmed parts is shown below:

CSEL	Programmed Configuration
0	0
1	1(Default)

Note: Typical enable time is 100µs.

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

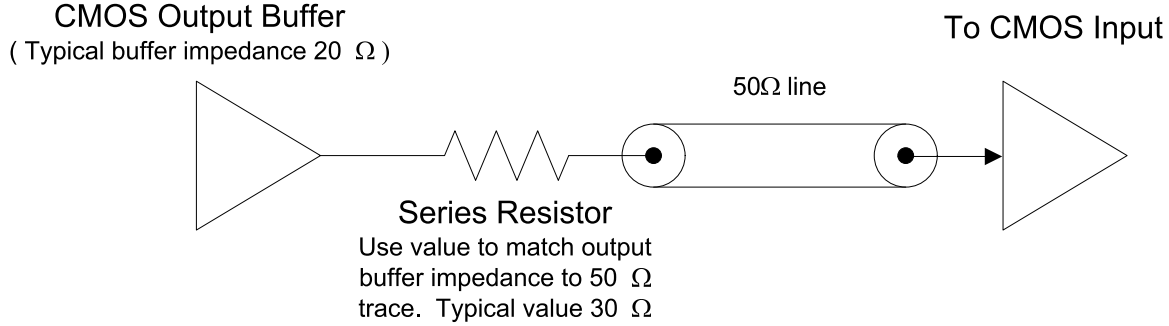
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1µF for designs using crystals < 50MHz and 0.01µF for designs using crystals > 50MHz.

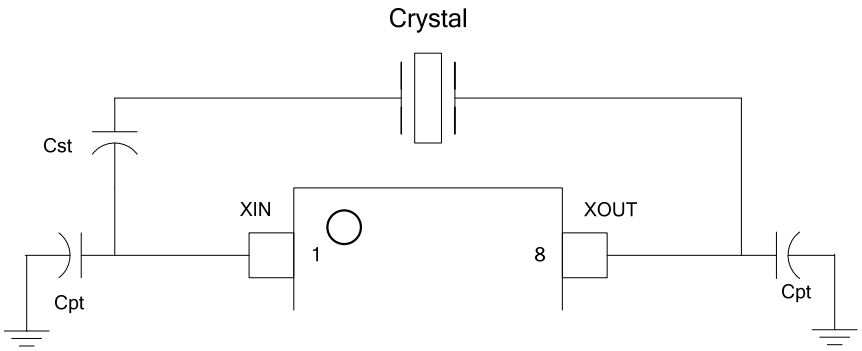
Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		50	MHz
Input (FIN) Frequency	@ V_{DD} =3.3V	1		200	MHz
	@ V_{DD} =2.5V			166	
	@ V_{DD} =1.8V			133	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			200	MHz
	@ V_{DD} =2.5V			166	
	@ V_{DD} =1.8V			133	
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
VDD Sensitivity	Frequency vs. V_{DD} +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	PLL Enabled, @ V_{DD} /2	45	50	55	%
Period Jitter, Pk-to-Pk* (10,000 samples)	Input 16MHz fundamental mode crystal, all outputs at 40MHz, 10pF Load, with capacitive decoupling between V_{DD} and GND.		100	120	ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, Loaded CMOS Outputs	I_{DD}	All outputs @ 20MHz 10pF Load		15	21	mA
Supply Current, Dynamic, Loaded CMOS Outputs	I_{DD}	All outputs @ 20MHz 10pF Load		11	16	mA
Supply Current, Dynamic, Loaded CMOS Outputs	I_{DD}	All outputs @ 20MHz 10pF Load		8.5	11	mA
Supply Current	I_{DD}	When PDB=0 All outputs @ 20MHz 10pF Load, V_{DD} = 3.3V			<10	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Std Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Std Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

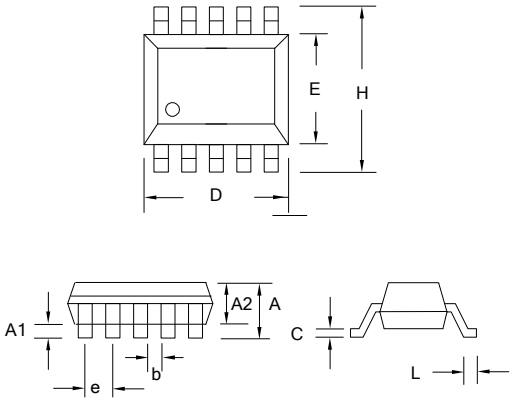
CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		50	MHz
Crystal Loading Rating		$C_{L\ (xtal)}$		15		pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

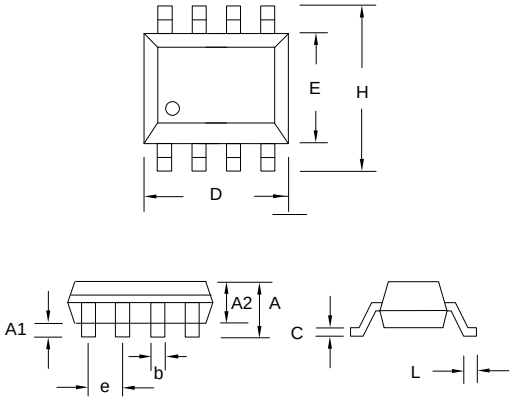
MSOP-10L

Symbol	Dimension in MM	
	Min.	Max.
A	0.86	1.06
A1	0.05	0.15
A2	0.81	0.91
b	0.17	0.25
C	0.1	0.2
D	3.00 BSC	
E	3.00 BSC	
H	--	5.08
L	0.43	0.63
e	0.50 BSC	



SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	

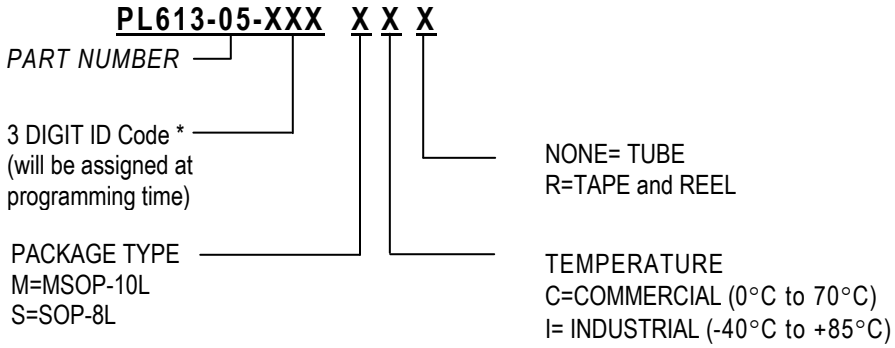


ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range



* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.

Part Number/Order Number	Marking†	Package Option
PL613-05-XXXMC	J3XXX	10-Pin MSOP (Tube)
PL613-05-XXXMC-R	J3XXX	10-Pin MSOP (Tape and Reel)
PL613-05-XXXSC	J3XXX	8-Pin SOP (Tube)
PL613-05-XXXSC-R	J3XXX	8-Pin SOP (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number.
Please consult your PhaseLink sales representative for marking information.

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf