



# PIC16C73A

## Errata Sheet for Rev. B PIC16C73A Silicon

The PIC16C73A (Rev. B) parts you have received conform functionally to the PIC16C7X data sheet (DS30390C), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of PIC16C73A silicon.

### 1. Module: USART

When the USART (SCI) is configured in asynchronous mode with the BRGH bit set, a high number of receive errors may be experienced. For asynchronous receive operations it is recommended that the USART be configured with the BRGH bit cleared.

### 2. Module: CCP

The special event trigger of the Compare mode may not occur if both of the following conditions exist:

- An instruction one cycle ( $T_{CY}$ ) prior to a Timer1/Compare register match has literal data equal to the address of a CCP register being used.\*
- An instruction in the same cycle as a Timer1/Compare register match has an MSb of '0'.

The interrupt for the compare event will still be generated, but no special event trigger will occur.

- \* 15h(CCPR1L), 16h(CCPR1H) or 17h(CCP1CON) for CCP1; 1Bh(CCPR2L), 1Ch(CCPR2H) or 1Dh(CCP2CON) for CCP2.

#### Work Around

Use the interrupt service routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

### 3. Module: Timer1

The Timer1 value may unexpectedly increment if either the TMR1H or the TMR1L register is written.

If Timer1 is ON, then turned OFF, performing any write instruction with TMR1H as the destination may cause TMR1L to increment.

#### Example 1:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = 3F:00

TMR1 value after MOVF instruction:

TMR1H:TMR1L = 3F:01

#### Example 2:

```
BSF T1CON, TMR1ON
```

:

```
BCF T1CON, TMR1ON
```

```
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after MOVF instruction:

TMR1H:TMR1L = FF:00

If Timer1 is ON, then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination may cause TMR1H to increment.

#### Example 1:

```
BSF T1CON, TMR1ON
```

:

```
BCF T1CON, TMR1ON
```

```
CLRF TMR1L
```

TMR1 value before CLRF instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after CLRF instruction:

TMR1H:TMR1L = 00:00

(TMR1IF is **not** set.)

#### Work Around

To preserve Timer1 register values:

Read Timer1 register values into "shadow" registers. Perform any write instruction(s) on the shadow registers. Write the shadow register values back into the Timer1 registers.

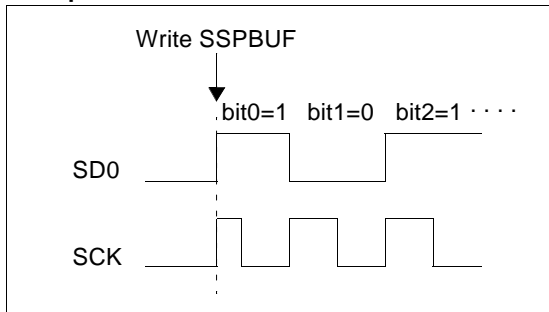
**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.

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## 4. Module: SSP

When the SPI is using Timer2/2 as the clock source, a shorter-than-expected SCK pulse may occur on the first bit of the transmitted/received data.

### Example:



### Work Around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on.

### Example Code:

```
BSF STATUS, RP0 ;Bank 1
LOOP BTFSS SSPSTAT, BF ;Data received?
; (Xmit complete?)
GOTO LOOP ;No
BCF STATUS, RP0 ;Bank 0
MOVF SSPBUF, W ;W = SSPBUF
MOVWF RXDATA ;Save in user RAM
MOVF TXDATA, W ;W = TXDATA
BCF T2CON, TMR2ON ;Timer2 off
CLR TMR2 ;Clear Timer2
MOVWF SSPBUF ;Xmit New data
BSF T2CON, TMR2ON ;Timer2 on
```

**Clarifications/Corrections to the Data Sheet:**

In the PIC16C7X Data Sheet (DS30390C), the following clarifications and corrections should be noted.

**NONE**

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## AMERICAS

### Corporate Office

Microchip Technology Inc.  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 602 786-7200 Fax: 602 786-7277  
Technical Support: 602 786-7627  
Web: <http://www.microchip.com>

### Atlanta

Microchip Technology Inc.  
500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770 640-0034 Fax: 770 640-0307

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Microchip Technology Inc.  
5 Mount Royal Avenue  
Marlborough, MA 01752  
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Miamisburg, OH 45342  
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18201 Von Karman, Suite 1090  
Irvine, CA 92612  
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### New York

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150 Motor Parkway, Suite 416  
Hauppauge, NY 11788  
Tel: 516 273-5305 Fax: 516 273-5335

### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408 436-7950 Fax: 408 436-7955

### Toronto

Microchip Technology Inc.  
5925 Airport Road, Suite 200  
Mississauga, Ontario L4V 1W1, Canada  
Tel: 905 405-6279 Fax: 905 405-6253

## ASIA/PACIFIC

### China

Microchip Technology  
Unit 406 of Shanghai Golden Bridge  
Bldg.  
2077 Yan'an Road West, Hongjiao Dis-  
trict  
Shanghai, Peoples Republic of China  
Tel: 86 21 6275 5700  
Fax: 011 86 21 6275 5060

### Hong Kong

Microchip Technology  
RM 3801B, Tower Two  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T. Hong Kong  
Tel: 852 2 401 1200 Fax: 852 2 401 3431

### India

Microchip Technology  
No. 6, Legacy, Convent Road  
Bangalore 560 025 India  
Tel: 91 80 526 3148 Fax: 91 80 559 9840

### Korea

Microchip Technology  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku,  
Seoul, Korea  
Tel: 82 2 554 7200 Fax: 82 2 558 5934

### Singapore

Microchip Technology  
200 Middle Road  
#10-03 Prime Centre  
Singapore 188980  
Tel: 65 334 8870 Fax: 65 334 8850

### Taiwan, R.O.C

Microchip Technology  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886 2 717 7175 Fax: 886 2 545 0139

## EUROPE

### United Kingdom

Arizona Microchip Technology Ltd.  
Unit 6, The Courtyard  
Meadow Bank, Furlong Road  
Bourne End, Buckinghamshire SL8 5AJ  
Tel: 44 1628 850303 Fax: 44 1628 850178

### France

Arizona Microchip Technology SARL  
Zone Industrielle de la Bonde  
2 Rue du Buisson aux Fraises  
91300 Massy - France  
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 Muenchen, Germany  
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleone Pas Taurus 1  
Viale Colleoni 1  
20041 Agrate Brianza  
Milan Italy  
Tel: 39 39 6899939 Fax: 39 39 689 9883

### JAPAN

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shin Yokohama  
Kohoku-Ku, Yokohama  
Kanagawa 222 Japan  
Tel: 81 45 471 6166 Fax: 81 45 471 6122

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