PowerMOS transistor PHT1N52S

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance. Intended for use in Compact Fluorescent Lights (CFL) and general purpose switching applications.

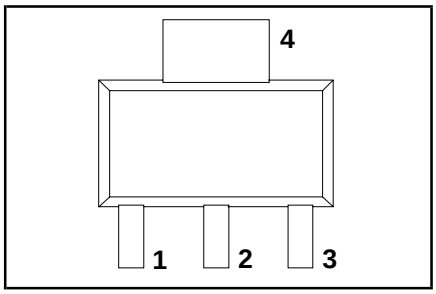
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	520	V
I_D	Drain current (DC)	0.6	A
P_{tot}	Total power dissipation	1.8	W
$R_{DS(ON)}$	Drain-source on-state resistance	10	Ω

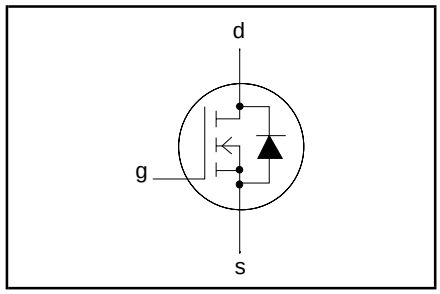
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	520	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	520	V
$\pm V_{GS}$	Gate-source voltage		-	30	V
I_D	Drain current (DC)	T_{sp} = 25 ˚C	-	0.6	A
		T_{sp} = 100 ˚C	-	0.5	A
I_{DM}	Drain current (pulse peak value)	T_{sp} = 25 ˚C	-	2.4	A
I_{DR}	Source-drain diode current (DC)	T_{sp} = 25 ˚C	-	0.6	A
I_{DRM}	Source-drain diode current (pulse peak value)	T_{sp} = 25 ˚C	-	2.4	A
P_{tot}	Total power dissipation	T_{sp} = 25 ˚C	-	1.8	W
T_{stg}	Storage temperature		-55	150	˚C
T_j	Junction temperature		-	150	˚C

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω			
		T_j = 25˚C prior to surge	-	25	mJ
		T_j = 100˚C prior to surge	-	10	mJ
W_{DSR}[1]	Drain-source repetitive unclamped inductive turn-off energy	I_D = 1 A ; $V_{DD} \leq$ 50 V ; V_{GS} = 10 V ; R_{GS} = 50 Ω ; $T_j \leq$ 150 ˚C	-	3.6	mJ

1. Pulse width and frequency limited by $T_{j(max)}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:2	-	70	-	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	520	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 ˚C	-	1	100	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	0.1	1.0	mA
I_{GSS}	Gate-source leakage current	V_{GS} = ±35 V; V_{DS} = 0 V	-	4	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1 A	-	7.9	10	Ω
V_{SD}	Source-drain diode forward voltage	I_F = 2 A ;V_{GS} = 0 V	-	0.85	1.2	V

DYNAMIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 15 V; I_D = 1 A	0.5	0.8	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	75	100	pF
C_{oss}	Output capacitance		-	10	15	pF
C_{rss}	Feedback capacitance		-	5	10	pF
$Q_{g(tot)}$	Total gate charge	V_{GS} = 10 V; I_D = 2 A; V_{DS} = 400 V	-	5	-	nC
Q_{gs}	Gate to source charge		-	.5	-	nC
Q_{gd}	Gate to drain (Miller) charge		-	3	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2 A;	-	5	10	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	15	20	ns
$t_{d\ off}$	Turn-off delay time	R_{GEN} = 50 Ω	-	15	20	ns
t_f	Turn-off fall time		-	7	15	ns
t_{rr}	Source-drain diode Reverse recovery time	I_F = 2 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Source-drain diode Reverse recovery charge	V_{GS} = 0 V; V_R = 100 V	-	1.5	-	µC

MOUNTING INSTRUCTIONS

Dimensions in mm.

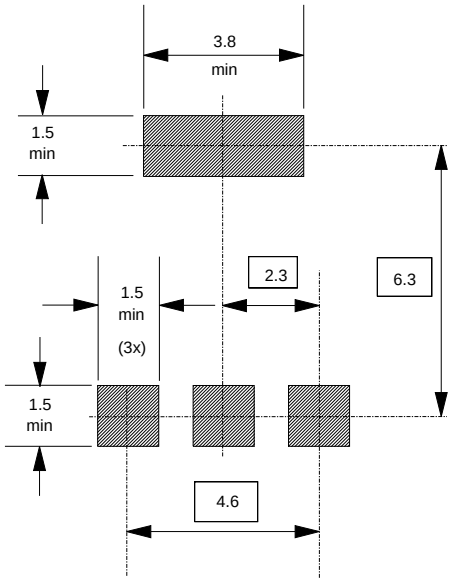


Fig.1. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

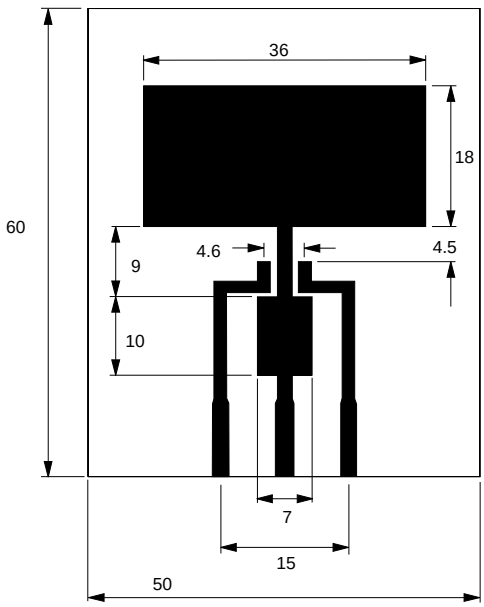


Fig.2. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

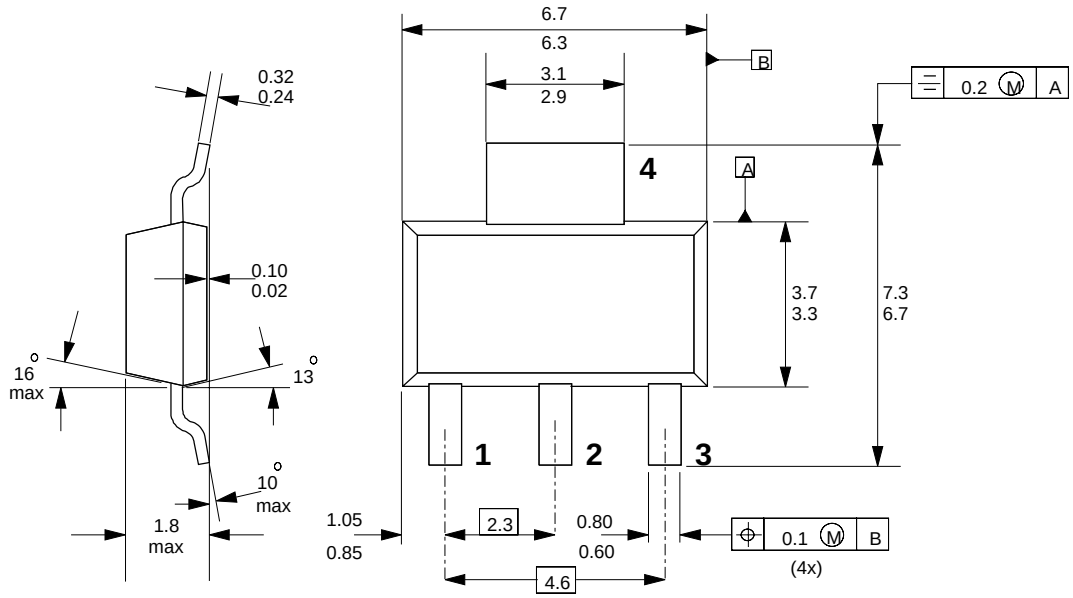


Fig.3. SOT223 surface mounting package.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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