

# PEEL™ 22LV10AZ-25 / I-35

## CMOS Programmable Electrically Erasable Logic Device

### Features

- Low Voltage, Ultra Low Power Operation**
  - $V_{CC} = 2.7$  to  $3.6$  V
  - $I_{CC} = 5 \mu A$  (typical) at standby
  - $I_{CC} = 1.5$  mA (typical) at 1 MHz
  - Meets JEDEC LV Interface Spec (JESD8-B)
  - 5 Volt tolerant inputs and I/O's
- CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- Application Versatility**
  - Replaces random logic
  - Super set of standard PLDs
  - Pin and JEDEC compatible with 22V10
  - Ideal for battery powered systems
  - Replaces expensive oscillators
- Architectural Flexibility**
  - Enhanced architecture fits in more logic
  - 133 product terms x 44 input AND array
  - 12 inputs and 10 I/O pins
  - 12 possible macrocell configurations
  - Asynchronous clear, synchronous preset
  - Independent output enables
  - Programmable clock; pin 1 or p-term
  - Programmable clock polarity
  - 24-Pin DIP/SOIC/TSSOP and 28 Pin PLCC
  - Schmitt triggers on clock and data inputs
- Schmitt Trigger Inputs**
  - Eliminates external Schmitt trigger devices
  - Ideal for encoder designs

### General Description

The PEEL22LV10AZ is a Programmable Electrically Erasable Logic (PEEL) SPLD (Simple Programmable Logic Device) that operates over the supply voltage range of 2.7V-3.6V and features ultra-low, automatic "zero" power-down operation. The PEEL22LV10AZ is logically and functionally similar to ICT's 5V PEEL22CV10A and PEEL22CV10AZ. The "zero power" ( $25 \mu A$  max.  $I_{CC}$ ) power-down mode makes the PEEL22LV10AZ ideal for a broad range of battery-powered portable equipment applications, from hand-held meters to PCMCIA modems. EE-reprogrammability provides both the convenience of product fast reprogramming for product development and quick personalization in manufacturing, including Engineering Change Orders.

The differences between the PEEL22LV10AZ and PEEL22CV10A include the addition of programmable clock polarity, p-term clock, and Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. Like the PEEL22CV10A, the PEEL22LV10AZ is a pin and JEDEC compatible, logical superset of the industry standard PAL22V10 SPLD Figure 1. The PEEL22LV10AZ provides additional architectural features that allow more logic to be incorporated into the design. The PEEL22LV10AZ architecture allows it to replace over twenty standard 24-pin DIP, SOIC, TSSOP and PLCC packages.

Figure 1 - Pin Configuration

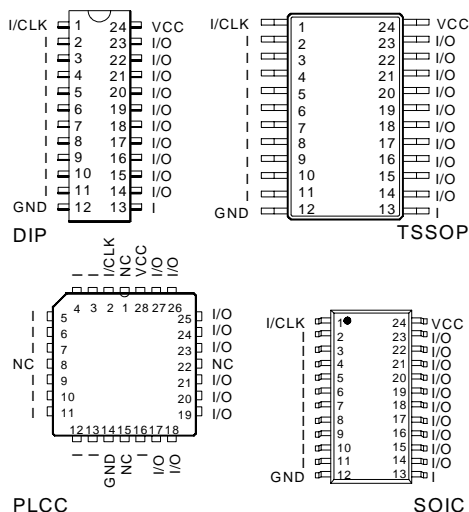
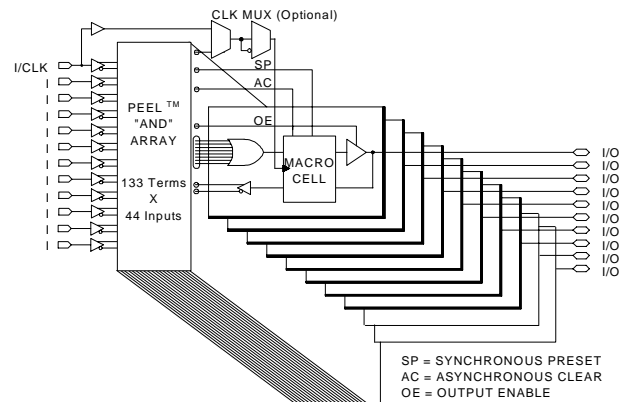


Figure 2 - Block Diagram



SP = SYNCHRONOUS PRESET  
AC = ASYNCHRONOUS CLEAR  
OE = OUTPUT ENABLE

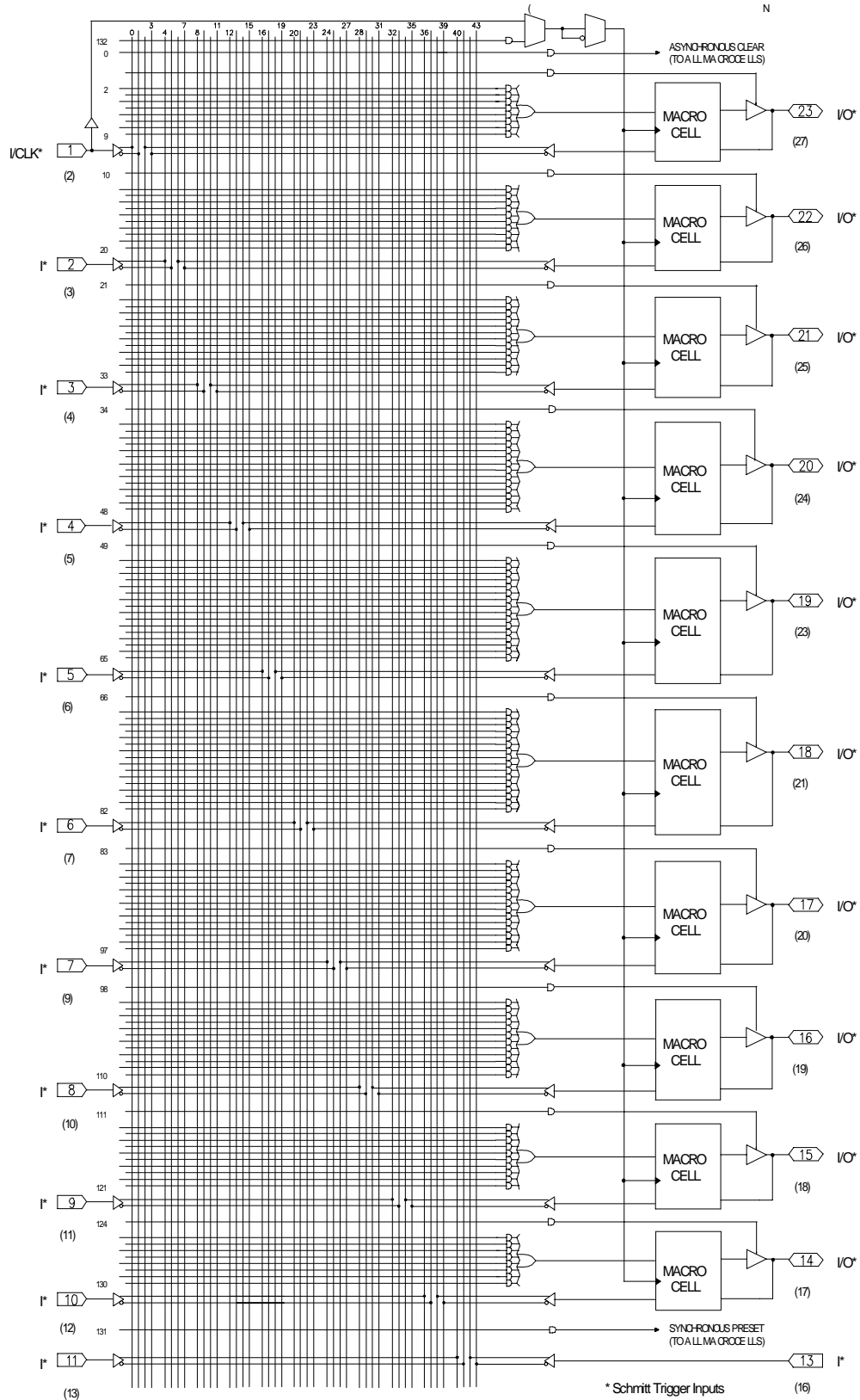


Figure 3 - PEEL22LV10AZ Logic Array Diagram



### Function Description

The PEEL22LV10AZ implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

ICT has added optional enhanced capabilities to the PEEL22CV10A family of products with additional features and added fuses to support them. Please view the comparison chart found below for the best algorithm

Algorithms	PEEL V10A Algorithm	PEEL V10A+ Algorithm	PEEL V10A++ Algorithm
Number of Fuses	5828	5873	5958
Supported Features	Standard 22V10 JEDEC Compatible  4 macrocell options	Superset of standard 22V10  12 macrocell options 3 byte signature word Security bit	Superset of standard 22V10 (recommended for new designs)  12 macrocell options 8 byte signature word Security bit Clock source selection Clock polarity selection

Table 1 - Programming Algorithm Comparison

### Architecture Overview

The PEEL22LV10AZ architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically erasable AND array that drives a fixed OR array. With this structure, the PEEL22LV10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the ten OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations, including the four standard 22V10 modes. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

### AND/OR Logic Array

The programmable AND array of the PEEL22LV10AZ (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **44 Input Lines:**
  - 24 input lines carry the true and complement of the signals applied to the 12 input pins
  - 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

### • 133 Product Terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) are used to form sum of product functions
- 10 outputs enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term
- 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL22LV10AZ, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).





**Programmable Clock Options** (see Table 1)

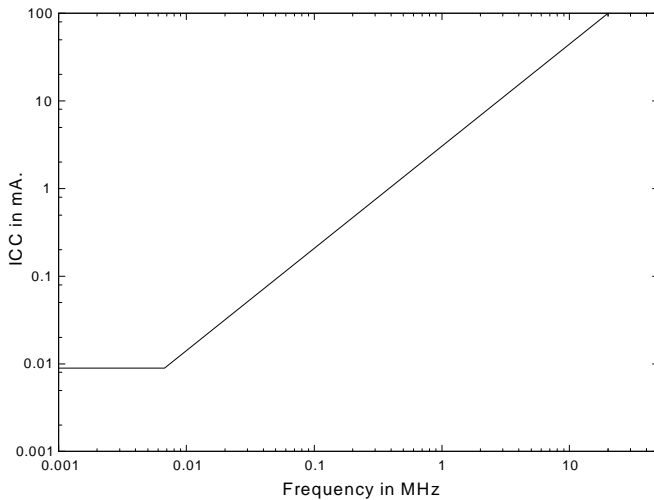
A unique feature of the PEEL22LV10AZ is a programmable clock multiplexer that allows the user to select true or complement forms of either input pin or product-term clock sources.

**Operates in both 3 Volt and 3.3 Volt Systems**

The PEEL22LV10AZ is designed to operate with a  $V_{CC}$  range of 2.7 to 3.6 Volts D.C. This allows operation in both 3 Volt 10% (battery operated) and 3.3 Volt 10% (power supply operated) systems. The propagation delay  $t_{PD}$  is 5 ns slower at the lower voltage, but this is typically not an issue in battery-operated systems (see Table 6 - A.C. Electrical Characteristics).

**Zero Power Feature**

The CMOS PEEL22LV10AZ features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately two  $t_{PD}$ 's, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down. (Note that the  $t_{PD}$  is approximately 5 ns. slower on the first transition from sleep mode.)



**Figure 5 - Typical ICC vs. Input Clock Frequency for the 22LV10AZ**

As a result of the "Zero-Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 5.

When the PEEL22LV10AZ is powered up, a built-in feature holds the outputs in tri-state until  $V_{CC}$  reaches 2.2V. This prevents output transitions during power-up.

**Schmitt Trigger Inputs**

The PEEL22LV10AZ has Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. They are also useful in cleaning up noisy signals. This makes the PEEL22LV10AZ especially desirable in portable applications where the environment is less predictable.

**Design Security**

The PEEL22LV10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

**Signature Word**

The signature word feature allows a 64-bit code to be programmed into the PEEL22LV10AZ if the PEEL V10A+ software option (see Table 1) is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

**Programming Support**

ICT's JEDEC file translator allows easy conversion of existing 24 pin PLD designs to the PEEL22LV10AZ, without the need for redesign. ICT supports a broad range of popular third party design entry systems, including Data I/O Synario and Abel, Logical Devices CUPL and others. ICT also offers its proprietary WinPLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers; Data I/O, Logical Devices, and numerous others.

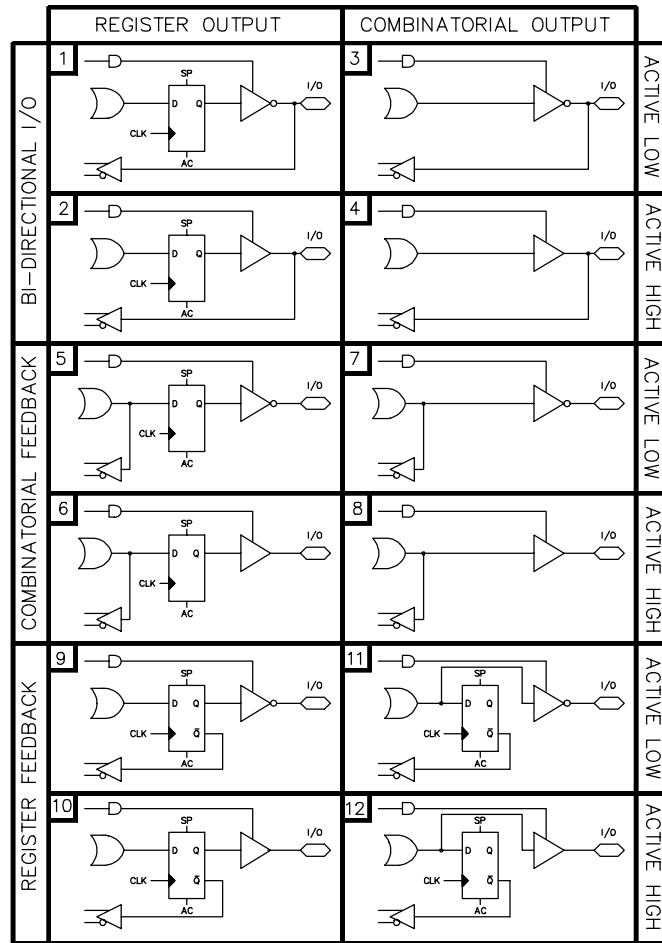


Figure 6 - Twelve Extended I/O Macrocell Configurations (see Table 1)

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-directional I/O	Register	Active Low
2	1	0	1	0		Register	Active High
3	0	1	0	0		Combinatorial	Active Low
4	1	1	0	0		Combinatorial	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1		Register	Active High
7	0	1	1	1		Combinatorial	Active Low
8	1	1	1	1		Combinatorial	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0		Register	Active High
11	0	1	1	0		Combinatorial	Active Low
12	1	1	1	0		Combinatorial	Active High

Table 2 – Extended Macrocell Configuration Bits (see Table 1)



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

**Table 3 - Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Rating	Unit
V <sub>CC</sub>	Supply Voltage	Relative to Ground	-0.5 to + 6.0	V
V <sub>I</sub> , V <sub>O</sub>	Voltage Applied to Any Pin <sup>2</sup>	Relative to Ground <sup>1</sup>	-0.5 to 5.5	V
I <sub>O</sub>	Output Current	Per Pin (I <sub>OL</sub> , I <sub>OH</sub> )	±25	mA
T <sub>ST</sub>	Storage Temperature		-65 to +150	°C
T <sub>LT</sub>	Lead Temperature	Soldering 10 Seconds	+300	°C

**Table 4 - Operating Range**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage <sup>3</sup>	Commercial/Industrial	2.7	3.6	V
T <sub>A</sub>	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T <sub>RVCC</sub>	V <sub>CC</sub> Rise Time	See Note 4.		250	ms

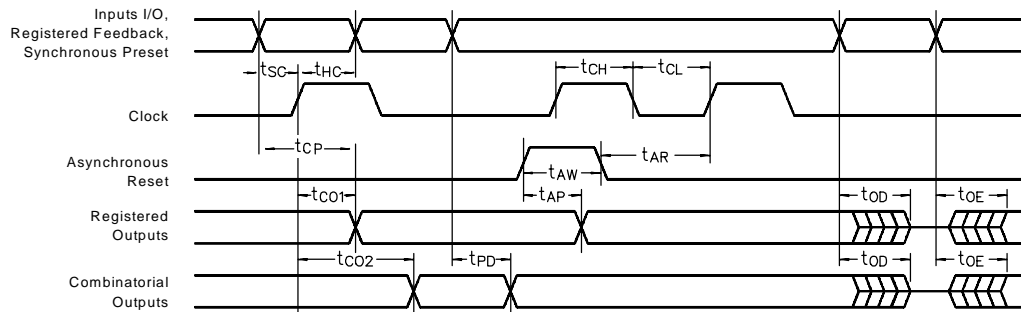
**Table 5 - D.C. Electrical Characteristics** Over the operating range (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage - TTL	V <sub>CC</sub> = Min, I <sub>OH</sub> = -2.0 mA	V <sub>CC</sub> - 0.5		V
V <sub>OHC</sub>	Output HIGH Voltage - CMOS	V <sub>CC</sub> = Min, I <sub>OH</sub> = -10 μA	V <sub>CC</sub> - 0.3		V
V <sub>OL</sub>	Output LOW Voltage - TTL	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>OLC</sub>	Output LOW Voltage - CMOS	V <sub>CC</sub> = Min, I <sub>OL</sub> = 10 μA		0.15	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 3.3 V	2.0	5.5	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 3.3 V	-0.3	0.8	V
V <sub>H</sub>	Input Voltage Hysteresis		0.2		V
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = Max, GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , I/O = High Z		+/- 1	μA
		V <sub>CC</sub> = Min, GND ≤ V <sub>IN</sub> ≤ 5.5V, I/O = High Z		25	μA
	I/O Leakage Current	V <sub>CC</sub> = Max, GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , I/O = High Z		+/- 1	μA
		V <sub>CC</sub> = Min, GND ≤ V <sub>IN</sub> ≤ 5.5V, I/O = High Z		500	μA
I <sub>CCS</sub>	VCC Current, Standby	V <sub>IN</sub> = 0V or V <sub>CC</sub> , All Outputs disabled <sup>5</sup>	5 (typ)	25	μA
I <sub>CC</sub> <sup>11</sup>	VCC Current, f=1MHz	V <sub>IN</sub> = 0V or V <sub>CC</sub> , All Outputs disabled <sup>5</sup>	1.5 (typ)	3	mA
C <sub>IN</sub> <sup>8</sup>	Input Capacitance	T <sub>A</sub> = 25°C, V <sub>CC</sub> = Max @ f = 1 MHz		6	pF
C <sub>OUT</sub> <sup>8</sup>	Output Capacitance			12	pF



**Table 6 - A.C. Electrical Characteristics**  
(Over the operating range<sup>9</sup>)

Symbol	Parameter	-25				I-35				Units
		3V±10%		3.3V±10%		3V±10%		3.3V±10%		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD</sub>	Input <sup>6</sup> to non-registered output in continuous mode <sup>13</sup>		30		25		40		35	ns
t <sub>OE</sub>	Input <sup>6</sup> to output enable <sup>7</sup>		30		25		40		35	ns
t <sub>OD</sub>	Input <sup>6</sup> to output disable <sup>7</sup>		30		25		40		35	ns
t <sub>CO1</sub>	Clock to output		20		15		28		25	ns
t <sub>CO2</sub>	Clock to comb. Output delay via internal registered feedback		40		35		56		49	ns
t <sub>CF</sub>	Clock to Feedback		14		9		20		13	ns
t <sub>SC</sub>	Input <sup>6</sup> or feedback setup to clock	20		15		28		21		ns
t <sub>HC</sub>	Input <sup>6</sup> hold after clock	0		0		0		0		ns
t <sub>CL</sub> , t <sub>CH</sub>	Clock low time, clock high time <sup>9</sup>	20		13		28		18		ns
t <sub>CP</sub>	Min clock period Ext (t <sub>SC</sub> + t <sub>CO1</sub> )	40		30		56		39		ns
f <sub>MAX1</sub>	Internal feedback 1/(t <sub>SC</sub> + t <sub>CF</sub> ) <sup>12</sup>	29.4		41.6		20.8		29.4		MHz
f <sub>MAX2</sub>	External Feedback (1/t <sub>CP</sub> ) <sup>12</sup>	25		33.3		17.9		25.6		MHz
f <sub>MAX3</sub>	No Feedback 1/(t <sub>CL</sub> + t <sub>CH</sub> ) <sup>12</sup>	25		38.4		17.9		27.7		MHz
t <sub>AW</sub>	Asynchronous Reset Pulse Width	30		25		40		35		ns
t <sub>AP</sub>	Input to Asynchronous Reset		30		25		40		35	ns
t <sub>AR</sub>	Asynchronous Reset recovery time		30		25		40		35	ns
t <sub>RESET</sub>	Power-on reset time for registers in clear state <sup>14</sup>		5		5		5		5	µs

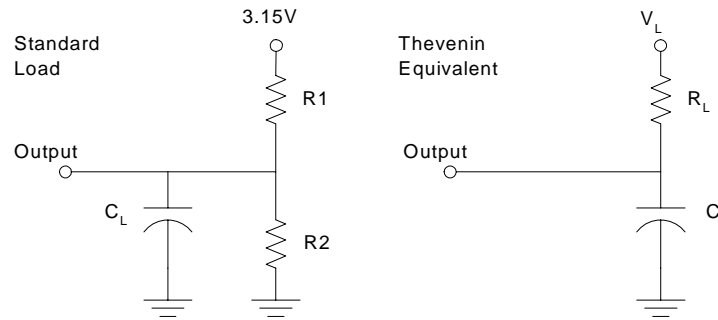


**Figure 7 - Switching Waveforms**

**Notes:**

- Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
- V<sub>I</sub> and V<sub>O</sub> are not specified for program/verify operation.
- The Supply Voltage range of 2.7 to 3.6V was chosen to allow this part to be used in both 3V 10% and 3.3V 10% applications.
- Test Points for Clock and V<sub>CC</sub> in t<sub>R</sub> and t<sub>F</sub> are referenced at the 10% and 90% levels.
- I/O pins are 0V and V<sub>CC</sub>.
- "Input" refers to an input pin signal.
- t<sub>OE</sub> is measured from input transition to V<sub>REF</sub> 0.1V, t<sub>OD</sub> is measured from input transition to V<sub>OH</sub> -0.1V or V<sub>OL</sub> +0.1V; V<sub>REF</sub> =V<sub>L</sub>
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
- Test one output at a time for duration of less than 1 second.
- ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
- t<sub>PD</sub>, t<sub>OE</sub>, t<sub>OD</sub>, t<sub>CO</sub>, t<sub>SC</sub>, and t<sub>AP</sub> are approximately 5 ns, slower on the first transaction from sleep mode.
- All inputs at GND.

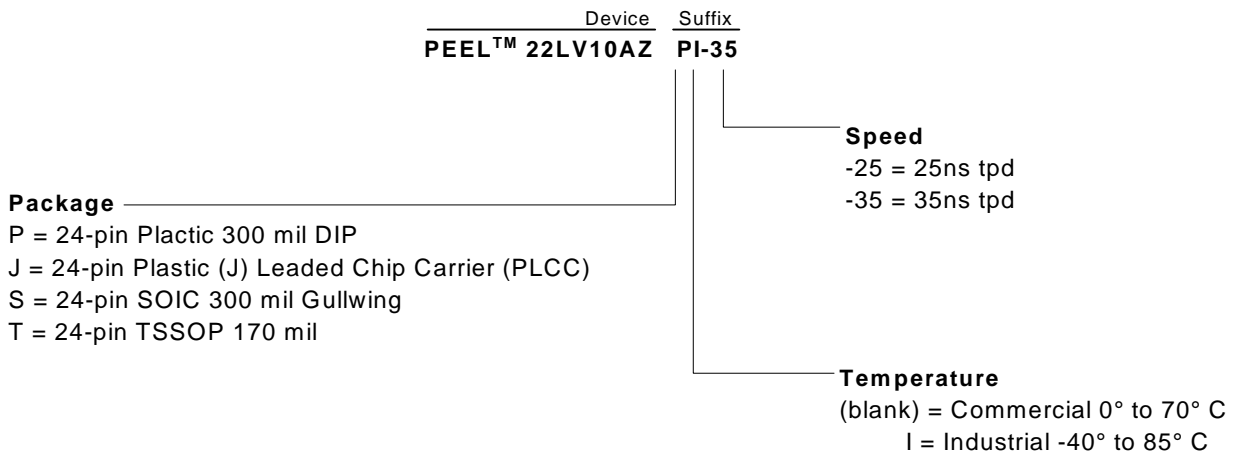



**Figure 8 - PEEL™ Device and Array Test Loads**

Technology	R1	R2	RL	VL	CL
CMOS	274kΩ	257kΩ	110kΩ	1.30V	33 pF
TTL	315Ω	548Ω	200Ω	2.00V	33 pF

**Table 7 - Ordering Information**

Part Number	Speed	Temperature	Package
PEEL22LV10AZP-25	25ns	Commercial	24-pin Plastic DIP
PEEL22LV10AZPI-35	35ns	Industrial	24-pin Plastic DIP
PEEL22LV10AZJ-25	25ns	Commercial	28-pin PLCC
PEEL22LV10AZJI-35	35ns	Industrial	28-pin PLCC
PEEL22LV10AZS-25	25ns	Commercial	24-pin SOIC
PEEL22LV10AZSI-35	35ns	Industrial	24-pin SOIC
PEEL22LV10AZT-25	25ns	Commercial	24-pin TSSOP
PEEL22LV10AZTI-35	35ns	Industrial	24-pin TSSOP


**Figure 9 - Part Number**



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