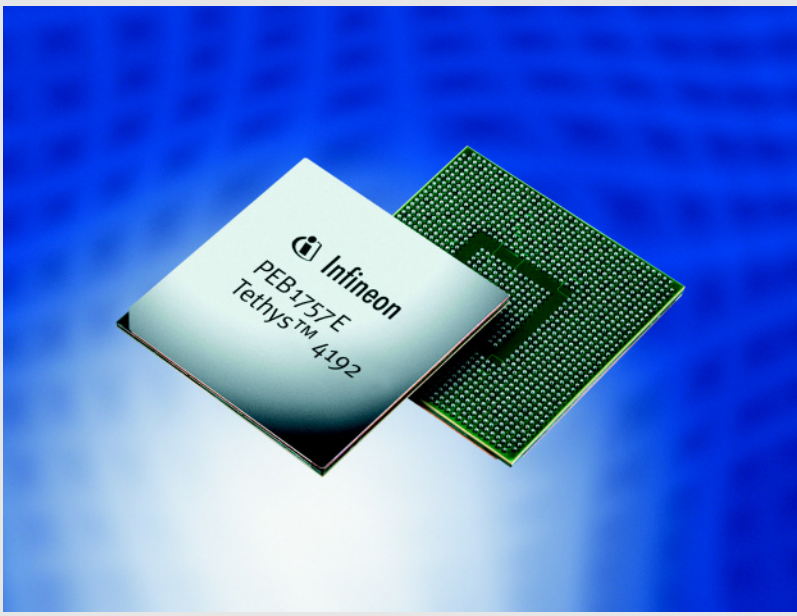
## Semiconductor Solutions for High Speed Communications and Fiber Optic Applications

**Tethys™ 4192 is optimized for SONET/SDH applications as a full-duplex four STS-192/STM-64 MUX/DEMUX with full framer functionality including pointer processing, and overhead termination; ideal for aggregation, ADM and DWDM applications. In the demultiplex ingress direction, Tethys™ 4192 accepts four STS-192/STM-64 signals in SFI-4.2/SFI-4.1 format. Tethys locates the incoming SONET/SDH frame, optionally de scrambles the data, monitors the TOH and POH, and provides STS-1 level pointer processing. In addition, Tethys supports TOH and POH overhead transparency.**

**In the multiplex direction, Tethys™ 4192 accepts four STS-192/STM-64 or sixteen STS-48/STM-16 signals in either 4 x 2.5 Gbit/s or serial 2.5 Gbit/s format. Further Tethys provides corresponding functionality in the DEMUX direction.**






### Applications

- ADM
- Metro Aggregation
- Digital Cross connects
- Repeaters
- DWDM Equipment
- Test Equipment

### Features

- Complies with OIF specifications SFI-4.2, SFI-4.1 or provides serial STS-48/STM-16 links
- Differential CML 2.5 G I/O interface to optics
- Differential CML 2.5 G I/O interface to system/backplane
- TFI-5 Support
- Processes SONET/SDH quad STS-192/STM-64 on the line side interface
- Processes SONET/SDH quad STS-192/STM-64 or sixteen STS-48/STM-16 on the system/client side serial 2.5 Gbit/s interface
- Provides line timing of all line and system side interfaces
- Processes SONET/SDH flexible concatenation streams of STS-2c, 3c, 4c, … to 192c
- Supports auto-detection of concatenation streams STS-3c/STM-1, STS-12c/STM-4,STS-48c/STM-16 and STS-192c/STM-64
- Supports STS-1 level pointer processing of STS-192/STM-64 or STS-48/STM-16 streams
- Provides interfaces for dropping alarm and status information, and for forcing alarm conditions
- Provides de skew of up to ± 250 ns for quad STS-192/STM-64
- Power dissipation of 15 W, depending on mode of operation
- Terminates and generates SONET section, line, and path layers
- Provides TOH and POH transparency
- Provides monitoring of POH bytes B3 and N1/Z5
- Provides B2 SF/SD capability for Poisson and bursty error distribution
- Provides full TOH/POH add/drop
- Provides STS-1 level POH add/drop
- Supports more than ±746 UI programmable output skew on STS-192/STM-64 or STS-48/STM-16 output links to external cross-connects
- For diagnostic purposes, Tethys provides PRBS generator/checker and loop backs
- Provides B1, B2, H1 and H2 bit error generation for both receive and transmit direction diagnostics
- Provides 1 second performance monitors

# Tethys™ 4192 PEB1757E

## Quad STS-192/STM-64 MUX/DEMUX

Infineon technologies

Never stop thinking.

**Features** (cont'd)

- Provides B1, B2, H1 and H2 bit error generation for both receive and transmit direction diagnostics
- Provides 1 second performance monitors
- 0.13 µm process, 1.2 V core, 3.3 V I/O
- Motorola 32-bit synchronous microprocessor interface for configuration, control, and status monitoring
- P-FCHBGA-1397 CBGA
- Complies with GR-253, GR-1377, ITU-T G.707, and ANSI T1.105
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes

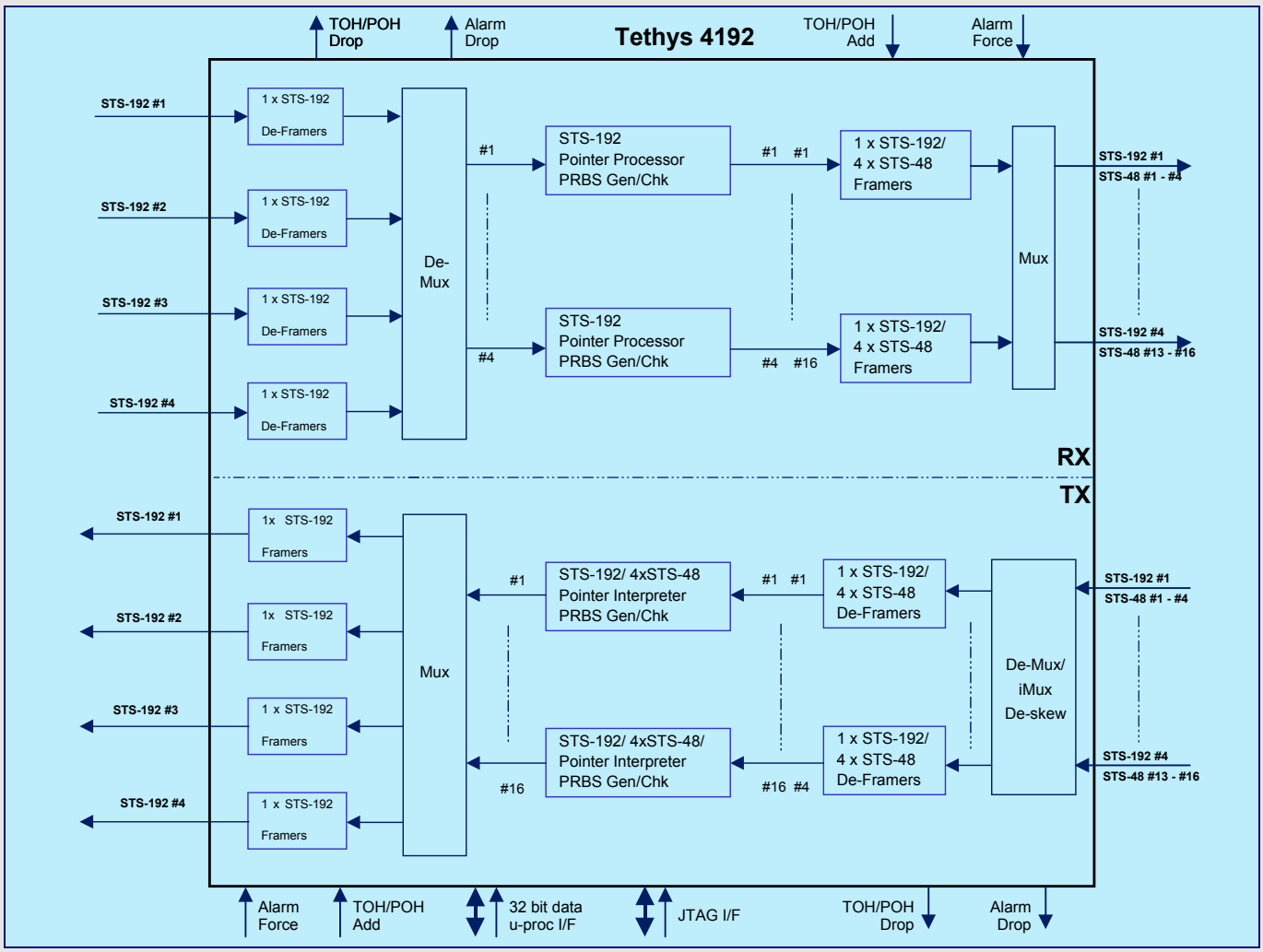
**Specifications**

- OIF SFI-4.1
- OIF SFI-4.2
- OIF TFI-5

**Standards**

- ANSI T1.105-2000-193R2 (DRAFT)
- ANSI T1.105.05-1994
- T1X1.3/93-005RI -1993 - preliminary
- GR-253-CORE Sept. 2000
- ITU-T G.707 10/2000

| Type | Sales Code | Description | Package |
|---|---|---|---|
| 1397 ball BGA | – | – | P-FCHBGA-1397 |




Tethys™ 4192 PEB1757E Block Diagram

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## Overview

Tethys™ 4192 is a highly integrated device that implements full duplex SONET/SDH processing at STS-192/STM-64 or STS-48/STM-16 rates. In the rest of this document, only SONET terminology will be stated. However, SDH terminology applies equally well unless otherwise written.

Tethys™ 4192 supports up to 40 Gbit/s bandwidth or 80 Gbit/s full-duplex. It provides section, line, and path overhead processing and supports framing, scrambling/de scrambling, alarm signal insertion/detection, bit interleaved parity (B1/B2/B3) processing, path overhead processing, pointer processing and TOH and POH transparency. It also provides substantial performance monitoring of TOH/POH overhead for the receive direction with 1 second count accumulation.

On the line side, quad STS-192 are supported. The interface utilizes SFI-4.2 or SFI-4.1. The STS-192 interfaces can be received at differing clock frequencies, depending on the SONET line clock variation of ±20 ppm. Similarly, the STS-192 outputs can be line timed to the corresponding incoming STS-192's.

On the system/client side, quad STS-192 or sixteen STS-48 can be interfaced. In this case, a 4 × 2.5 Gbit/s or serial 2.5 Gbit/s is utilized for the respective interfaces.

The System side can support 16 independent STS-48 links or four groups of STS-192 links, where each group of an STS-192 link consists of four 2.488 Gbit/s links. This means for instance that 8 STS-48's and two STS-192's can be supported at the same time. Or alternatively, three STS-192's and four STS-48's. In fact, any legal mix of interfaces can be supported. The selection/configuration of the system and line side interfaces is completely independent.

All TOH (A1 … E2) bytes can be added/dropped onto the parallel TOH/POH interfaces. This applies in both receive and transmit directions.

All POH passing through the device can be added or dropped onto the TOH/POH ports. The TOH and POH ports are physically shared.

Detected alarms like LOS, LOF, SEF, AIS-L can be dropped onto the parallel Alarm Drop Interfaces. This applies in both the receive and transmit directions. In addition, Tethys™ 4192 can drop the payload concatenation configuration onto the same interface.

In TOH Transparency mode, J0, B1, E1, F1, K1, K2, D1-D12, S1, M0/M1 and E2 bytes are transparent through the device. In POH Transparency mode, all POH bytes, including the B3 bytes, are transparent as is. TOH/POH transparency can be implemented through the TOH/POH ADD/DROP ports using the dropped overhead and bit error masks on these interfaces. This applies to both the receive and transmit directions.

Tethys™ 4192 can process any legal mix of flexible concatenated signals ranging from STS-1, STS-2c, STS-3c … up to STS-192c. Each set of concatenated signals must fit inside an STS-48 or STS-192 boundary (depending on whether the pointer processor is configured as an STS-48 or STS-192 block) and must be formatted as an STS-Nc frame as defined in GR-253-CORE.

Tethys™ 4192 provides the ability for certain frame structures to be automatically detected and configured into the device. This feature allows the user to interface to systems with unknown standard payload concatenation configurations.

Various diagnostic features are provided. Framed PRBS-32 can be generated and checked on any channel via loop backs. Errors can be inserted into B1, B2, H1 and H2 bytes on a bit-by-bit basis.

To support asynchronous timing between different physical ports, Tethys™ 4192 provides STS-1 level pointer processing for quad STS-192 interfaces in the receive direction. On the line side receive interface, all inputs can be asynchronous with frequency differences of ±20 ppm.

The pointer processor on the receive side adjusts for these differences and outputs the STS-192 or STS-48 streams based on the line timed or system frequencies selected on the system side. In the transmit direction, the system side ingress ports and line side egress ports must be locked to the same frequency.

Tethys™ 4192 aggregates all STS-48 or STS-192 ports from the system side to the line side in the transmit/multiplex direction. In the case of quad STS-192 interfaces on the line side, any one of the STS-48 ports can be aggregated into any one of the STS-192 line side ports.

To select the best timing available in the system, the S1 bytes are processed and the system has the option to select either timing from the line or timing from the local reference source. On the system side, the receive outputs can be line timed to their respective system side transmit inputs.

When interfacing the system side physical ports to different transmission paths, the ports can have skew of up to ±250 ns. This skew must be tolerated in order to support the normal multiplex of STS-48 streams to higher rate signals to the line side. For this purpose, Tethys™ 4192 includes de skew buffers for desks of up to ±250 ns between the ports on the system side.

Tethys™ 4192 generates and detects all SONET/SDH relevant alarms and defects, including LOS, LOF, RDI-L, REI-L, AIS-P, AIS-L and LOC on each line side and system side interface.

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## Applications

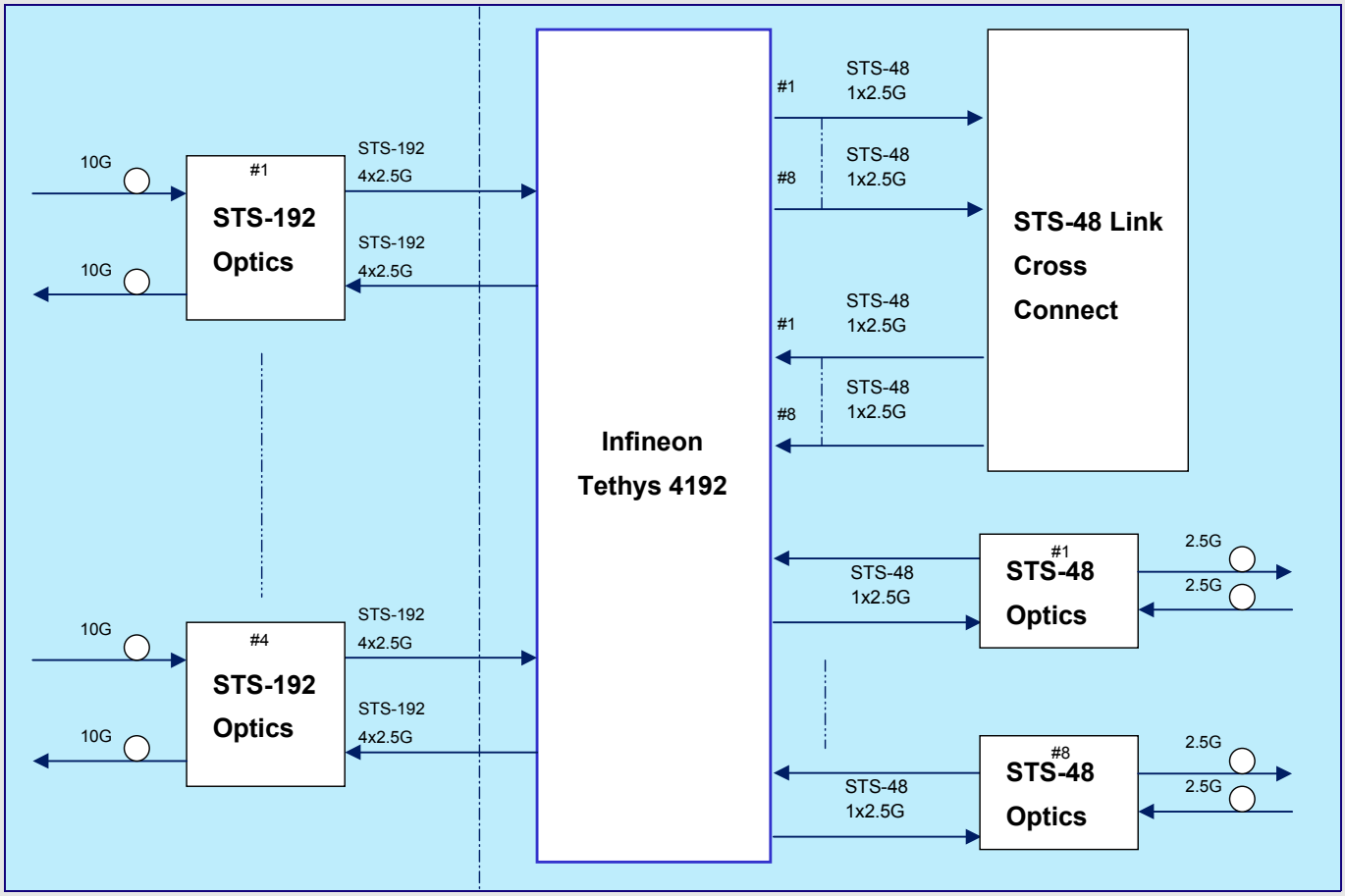
The application below shows how a quad STS-192 signal can be connected to a Tethys™ 4192 device.

Tethys™ 4192 receives an SFI-4.2's format STS-192 frame from the optical device. It then performs framing, performance monitoring, and rate adaptation in the receive direction, and finally outputs an STS-48 single 2.5 Gbit/s differential pair to the STS-48 link cross connect or the STS-48 optics transceivers.

In the transmit direction, Tethys™ 4192 performs the reverse operation.

TOH and POH interfaces may be added and dropped as required through the respective Tethys™ 4192 ports (not shown).

Many other configuration options are possible that cannot be shown in this diagram. Please refer to the data sheet for more detailed information.




40G - STS-48 Cross Connect and Aggregation

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Template: pb_tmplt.fm/4/2003-07-01

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